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Influence of annealing effects on the electrical and microstructural properties of Se Schottky contacts on n-type GaN

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Abstract The electrical and microstructural properties of Se/n-gallium nitride (GaN) Schottky diode have been investigated by current–voltage (I–V), capacitance–voltage (C–V) and transmission electron microscopy (TEM) measurements as a function of annealing temperature. The Se/n-GaN Schottky contact exhibited an excellent rectification behavior. The barrier height of the as-deposited Se/n-GaN Schottky contact is 0.94 eV (I–V) and 1.55 eV (C–V), respectively. However, the barrier height of Se/n-GaN Schottky diode decreases to 0.90 eV (I–V) and 1.33 eV (C–V) upon annealing at 200 °C. Cheung's and modified Norde functions are employed to determine the barrier height and series resistance. TEM results reveal that the Se film becomes fully crystallized for the contact annealed at 200 °C compared to the as-deposited contact without the reaction between Se film and GaN substrate. It is observed that the barrier height of Se/n-GaN Schottky diode decreases with increasing annealing temperature. This could be associated with the decrease in series resistance caused by the phase transformation from high resistance amorphous Se to low resistance crystalline Se. Further, the interface states density is found to be increased with the increasing annealing temperature. The Schottky emission mechanism is found to dominate the reverse leakage current in Se/n-GaN Schottky diodes irrespective of annealing temperatures.

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1 Introduction

Owing to the wide and direct-energy band gap, the gallium nitride (GaN) is attractive for the fabrication of microelectronic and optoelectronics devices such as light emitting diodes (LEDs) [1], lasers [2], metal–semiconductor-metal (MSM) photo detectors [3], hetero junction field effect transistors (HFETs) [4], high electron mobility transistors (HEMTs) [5], metal oxide semiconductor field effect transistors (MOSFETs) [6] and Schottky rectifiers [7]. These exciting applications present several challenges in making high performance metal contacts to GaN-based materials, which is crucial for device performance. Still, the excess reverse bias leakage current is a major impediment in GaN-based Schottky contacts even though continuous improvement in the synthesis of III-nitride materials by different growth techniques leads to increased device quality [8]. For that reason, the fabrication of high-quality Schottky contacts on GaN with high barrier height and low reverse leakage current is still up till now represents a challenge

Many researchers have explored various metal schemes for the fabrication of Schottky contacts on n-type GaN [9–17]. For example, Venugopalan et al. [9] investigated the electrical properties of Re/n-GaN Schottky contact by I–V and C–V measurements, reported that the barrier height was 0.82 and 1.06 eV after annealing at 500 °C. Auret et al. [10] reported a barrier height of 1.08 eV for Ru/n-GaN Schottky contact by I–V measurements. Fang et al. [11] found that the Al/Ni/Au contact exhibits high quality Schottky contact with a barrier height of 0.875 eV and the

lowest reverse-bias leakage current respectively after annealing at 450 °C for 12 min in N_2 ambient. Reddy et al. [12] studied the electrical and structural properties of Pt/Mo Schottky contacts to n-GaN as a function of annealing temperature. They indicated that the reason for the increase of Schottky barrier heights (SBHs) upon annealing at elevated temperatures was ascribed to the formation of gallide phases at the Pt/Mo/n-GaN interface. Menard et al. [13] prepared Ni based Schottky diodes with different metal thicknesses (20, 100 and 300 nm) on n-type GaN and reported that the Ni Schottky contact with a 300 nm thickness exhibited good rectifying behavior after annealing at 450 °C during 3 min under Ar. Jung et al. [14] investigated the effects of rapid thermal annealing (RTA) on the performance of Ni/Au Schottky devices on non-polar a-plane GaN. They showed that the SBH is improved by 43 % with annealing up to 500 °C under N_2 ambient. Dobos et al. [15] studied the thermal annealing effects on Al and Ti/Al Schottky contacts on n-GaN using XTEM, FESEM, XRD and I–V characteristics. They reported that as-deposited Al and Ti/Al contacts were rectifying, but after heat treatment at 300 and 400 °C both contacts exhibited linear current–voltage characteristics. Siva Pratap Reddy et al. [16] investigated the effect of annealing on the electrical and structural characteristics of Ni/Pd Schottky rectifiers on n-type GaN. They reported that the change in SBH and ideality factor during different annealing temperatures may be attributed to the interfacial reactions between the Ni/Pd and GaN layers. Nanda Kumar Reddy [17] studied the electrical and structural properties of Pd/Ru/n-GaN Schottky diode by I–V, C–V, XPS and XRD measurements, and reported that the barrier height increased upon annealing at 300 °C and then slightly decreased after annealing at 400 °C. Also, they found that the formation of gallide phases at the Pd/Ru and n-GaN layers could be the reason for the increase in the barrier height. Although, the extensive work is being carried out on GaN-based Schottky barrier diodes (SBDs) [9–17] for the past few years, the fabrication of Schottky contacts with high barrier height and low reverse leakage current is still a scientific challenge. It is well known that the rectifying properties of Schottky contact strongly depends on the work function of metal. Till now, platinum (Pt) is the most preferred metal in the fabrication of Schottky rectifiers because of its high work function (5.65 eV) despite its expensiveness as compared to most metals [18]. However, Se is inexpensive and can be expected to provide far superior device performance as a Schottky electrode, since it has the highest reported work function (5.9 eV) of all the chemical elements [19]. Further, the efforts for the implementation of Se into Schottky rectifier is limited at this moment and has not been explored to date as a Schottky contact to n-type GaN. For the first time, we have fabricated Se Schottky contact on n-type GaN and investigated its electrical and microstructural properties by current–voltage (I–V), capacitance–voltage (C–V) and transmission electron microscopy (TEM) techniques as a function of annealing temperature.

2 Experimental details

In this work, 2 µm-thick Si-doped GaN films ($N_d = 4.07 \times 10^{18}$ cm^{-3}) used were grown by metal organic chemical vapor deposition on c-plane sapphire substrate. First, the n-GaN wafer was ultrasonically degreased with warm trichloroethylene, acetone and methanol for 5 min in each. This degreased layer was then dipped into buffered oxide etch (BOE) solution for 10 min to remove the surface oxide and rinsed in DI water. Standard photolithography and lift-off techniques were used to define contact electrodes. After the above procedure, Ti (30 nm)/Al (60 nm) films were deposited on cleaned GaN surface to form ohmic contacts. Then, the contacts were annealed at 750 °C in N_2 for 1 min in a RTA system. A Schottky contact of Se (30 nm) films were thermally evaporated from a stainless-steel effusion cell under a base pressure of 1×10^{-6} Torr without substrate heating. The area of the circular Schottky contacts was 3.14×10^{-4} cm^2. The Se/n-GaN Schottky diodes were sequentially annealed at 100, 150 and 200 °C for 1 min under nitrogen ambient in a RTA system. The annealing temperature was limited to 200 °C since the melting point of Se is 221 °C. I–V and C–V measurements were performed at room temperature using a precision semiconductor parameter analyzer (Agilent 4156C) and precision LCR meter (Agilent 4284A), respectively. The microstructure and interfacial reactions of the Se/n-GaN Schottky contact was investigated by the TEM (Tecnai G^2 F30 S-Twin) with an acceleration voltage of 300 kV installed with energy dispersive X-ray spectroscopy (EDX) (EDAX Genesis).

3 Results and discussion

Figure 1 shows the current–voltage (I–V) characteristics of the Se/n-type GaN Schottky diode as a function of annealing temperature. The measured reverse leakage current is 9.599×10^{-10} A at −1 V for the as-deposited contact. For the contacts annealed at 100 and 150 °C, the reverse leakage current values are 1.867×10^{-9} and 2.295×10^{-9} A at −1 V, respectively. However, when the contact is annealed at 200 °C, the reverse leakage current increases to 1.092×10^{-8} A at −1 V. These results indicate that the electrical properties of Se/n-GaN Schottky

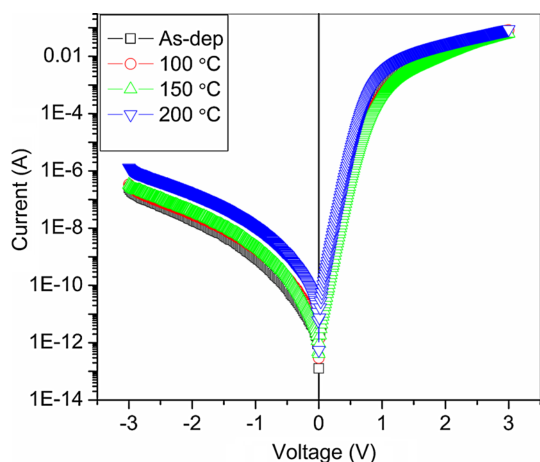

Fig. 1 The current–voltage (I–V) characteristics of the Se/n-GaN Schottky diode measured at different annealing temperatures

diode slightly degraded upon annealing at 200 °C. The Se/n-GaN Schottky diode showed a good rectification behavior for all annealing temperatures, suggests that the current transport over the top of the barrier may be described by the thermionic emission (TE) theory. The current through a SBD at a forward bias (V) according to TE theory is given by [20, 21]

$$I = I_o \exp\left(\frac{qV_d}{nkT}\right)\left[1 - \exp\left(\frac{qV_d}{kT}\right)\right] \quad (1)$$

where $V_d = (V - IR_s)$ is the diode voltage. I_o is the saturation current derived from the straight line intercept of ln(I) at zero-bias and is given by

$$I_o = AA^*T^2 \exp\left[\frac{q\phi_b}{kT}\right] \quad (2)$$

T is the absolute temperature in Kelvin, V is the applied voltage, k is the Boltzmann's constant, A is the diode area, A^* is the effective Richardson constant (26.4 A cm^{-2} K^{-2} for n-GaN) [22], ϕ_b is the zero-bias SBH and n is the ideality factor. From Eqs. (1) and (2), ideality factor n and barrier height ϕ_b can be written as

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right) \quad (3)$$

and

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_o}\right) \quad (4)$$

A plot of ln(I) versus V is a straight line with a slope of q/(nkT) and the intercept on y-axis yields I_o. Once I_o is determined, the barrier height (ϕ_b) can be estimated using Eq. (4). Calculations showed that the barrier height of as-deposited Se/n-GaN Schottky diode is 0.94 eV. However, the barrier heights slightly decrease upon annealing at 100 and 150 °C, and the values are 0.93 and 0.91 eV, respectively. When the contact is annealed at 200 °C, the barrier height further decreases to 0.90 eV. The ideality factors calculated from the slope of the linear forward I–V curves are found to be 1.10 for as-deposited, 1.19 for 100 °C, 1.26 for 150 °C and 1.38 for 200 °C respectively. All annealed Se/n-GaN Schottky diodes showed the ideality factor is greater than unity. The higher values of ideality factor are probably due to potential drop in the interface layer between Se and n-GaN and presence of excess current and the recombination current through the interfacial states between the semiconductor/insulator layers [23]. Another possibility may be due to the presence of a wide distribution of low SBH areas caused by a laterally inhomogeneous barrier, as suggested by Tung [24].

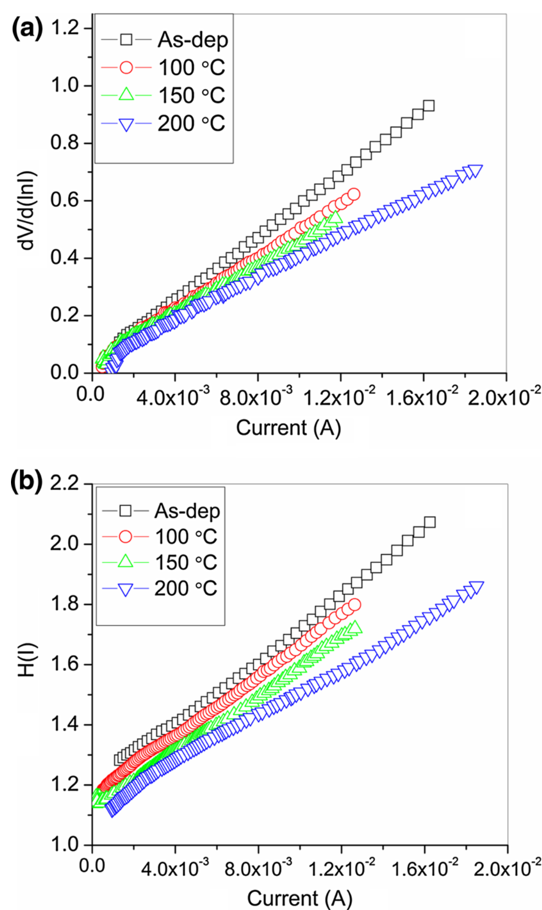

Fig. 2 **a** dV/d(lnI) versus I, and **b** H(I) versus I plot of the Se/n-GaN Schottky diode at different annealing temperatures

As can be seen from Fig. 1, the forward bias current–voltage (I–V) characteristics of the Se/n-GaN Schottky diode deviate significantly from linearity when the applied voltage is sufficiently large due to the presence of the effect of series resistance R_s. Hence, the series resistance is an important parameter for junction diodes. The R_s values are estimated using a method developed by Cheung and

Cheung [25]. Based on the Cheung and Cheung [25], the series resistance can be calculated from the following Cheung's functions

$$\frac{dV}{d(\ln I)} = \frac{nkT}{q} + IR_S \tag{5}$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \tag{6}$$

and H(I) is given as follows.

$$H(I) = n\phi_b + IR_s \tag{7}$$

A plot of *dV/d(lnI)* versus *I* will be linear and gives R_s as slope and nkT/q as the y-axis intercept from Eq. (5). Figure 2a shows a plot of *dV/d(lnI)* versus *I* for the Se/n-GaN Schottky contacts at different annealing temperatures. The values of ideality factor *n* and series resistance R_s are calculated as 1.17 and 55 Ω for as-deposited, 1.24 and 46 Ω for 100 °C, 1.31 and 42 Ω for 150 °C, and 1.40 and 37 Ω for 200 °C, respectively.

Moreover, *H(I)* versus *I* (Fig. 2b) will be linear, the slope of this plot gives a different determination of R_s. The value of the barrier height ϕ_b is estimated from the y-axis intercept of this plot, using the value of the *n* calculated from Eq. (5). The values of ϕ_b and R_s are estimated from *H(I)* versus *I* plot as 0.96 eV and 58 Ω for as-deposited, 0.94 eV and 50 Ω for 100 °C, 0.93 eV and 46 Ω for 150 °C, and 0.91 eV and 39 Ω for 200 °C, respectively. The values of R_s obtained from the plots of *dV/d(lnI)* versus *I* are in good agreement with those estimated from the plots of *H(I)* versus *I*, implying their consistency and validity.

In order to estimate the values of the barrier height ϕ_b and series resistance R_s, an alternative method was proposed by Norde method [26]. The method involves a Norde function, F(V), being plotted against V (plot not shown here). The modified Norde function is expressed as

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{8}$$

where γ is a dimensionless integer having value greater than the ideality factor, I(V) is the current obtained from the I–V curve. The effective barrier height is given by

$$\phi_b = F(V_{\min}) + \frac{V_{\min}}{\gamma} - \frac{kT}{q} \tag{9}$$

where $F(V_{min})$ is the minimum point of F(V), and V_{min} is the corresponding voltage. From the Norde's functions, the R_s is calculated using the relation

$$R_s = \frac{kT(\gamma - n)}{qI} \tag{10}$$

where I is the current in the device corresponding to voltage V_o (at which F(V) becomes minimum). From modified Norde method, the ϕ_b and R_s are found to be 1.03 eV and 70 Ω for as-deposited, 1.02 eV and 61 Ω for 100 °C, 0.98 eV and 50 Ω for 150 °C, and 0.95 eV and 46 Ω for 200 °C, respectively. It is noted that there is good agreement between the values of ϕ_b estimated from the forward bias ln I–V, the Cheung function and the Norde function. Also, the R_s obtained from the Norde function is reasonably in good agreement with those obtained from the plot of *dV/d(lnI)* versus *I* and the Cheung function. Further, it is noted that the series resistance decreases with increasing in annealing temperature. Such annealing temperature dependency of series resistance of Se/n-GaN Schottky diode could be related to the crystallinity of Se film caused by RTA process. This is confirmed by TEM results.

The C–V characteristics of Se/n-GaN Schottky diodes were measured at frequency of 1 MHz as a function of annealing temperature. Figure 3 shows a plot of $1/C^2$ as a function of bias voltage for as-deposited and annealed Se/n-GaN Schottky diodes. The C–V relationship for Schottky diode is given by [21]

$$\frac{1}{C^2} = \frac{2\left(V_{bi} - \frac{kT}{q} - V\right)}{A^2qN_d\varepsilon_s}, \tag{11}$$

where V_{bi} is the built-in-potential, N_d is the donor concentration, A is the area of the Schottky contact and ε_s is the permittivity of the semiconductor ($\varepsilon_s = 9.5\ \varepsilon_o$). The x-intercept of the plot of $(1/C^2)$ versus V gives V_o, V_o is related to the built-in-potential V_{bi} given by $V_{bi} = V_o + kT/q$, where T is the absolute temperature. The barrier height (ϕ_{cv}) is given by $\phi_{cv} = V_{bi} + V_n$, where $V_n = (kT/q)\ \ln\ (N_c/N_d)$. The density of states in the conduction band edge is given by $N_c = 2\ (2\pi m^*kT/h^2)^{3/2}$, where $m^* = 0.22\ m_o$ and its value was $2.6 \times 10^{18}\ cm^{-3}$ for GaN at room temperature [27]. The barrier height of the Se/n-GaN Schottky diode is found to be 1.55 eV. For the samples annealed at 100, 150 and 200 °C, the SBHs are 1.48, 1.41 and 1.33 eV, respectively. Table 1 show the values of barrier heights, ideality factors, series resistance and interface state density for the Se Schottky contacts to n-type GaN at different annealing temperatures. From Table 1, it is noted that there is a large difference between the barrier heights estimated by the I–V and C–V measurements. This difference may be due to the existence of barrier height inhomogeneity at the metal/semiconductor interface. The current in the I–V measurement is dominated by the current which flows through the regions of low barrier height. Consequently, the measured I–V barrier height is significantly lower than the weighted arithmetic average of the SBHs [28]. On the other hand, the C–V measured barrier height influenced by the distribution of charge at the depletion region

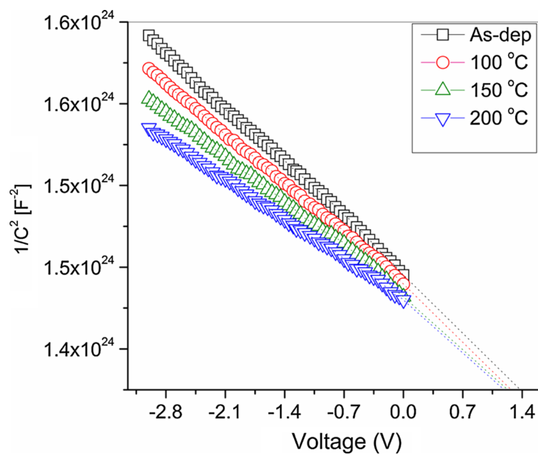

Fig. 3 Plot of $1/C^2$ versus V of the Se/n-GaN Schottky diode at different annealing temperatures

Table 1 Various electronic parameters estimated from I–V and C–V characteristics on the Se/n-GaN Schottky diode at different annealing temperatures

Parameter	As-dep.	100 °C	150 °C	200 °C
From I–V characteristics				
Barrier height [ϕ_b (eV)]	0.94	0.93	0.91	0.90
Ideality factor (n)	1.10	1.19	1.26	1.38
From Cheung's method dV/d(lnI) versus I				
Series resistance [R_s (Ω)]	55	46	42	37
Ideality factor (n)	1.17	1.24	1.31	1.40
H(I) versus I				
Series resistance [R_s (Ω)]	58	50	46	39
Barrier height [ϕ_b (eV)]	0.96	0.94	0.93	0.91
From Norde's method				
Series resistance [R_s (Ω)]	70	61	50	46
Barrier height [ϕ_b (eV)]	1.03	1.02	0.98	0.95
From C–V characteristics				
Built-in potential (V)	1.40	1.31	1.26	1.20
Barrier height [ϕ_b (eV)]	1.55	1.48	1.41	1.33
Interface state density [N_{ss} ($\times 10^{13}$ cm^{-2} eV^{-1})]	6.63	6.89	7.04	7.52

boundary and this charge distribution follows the weighted arithmetic average of the SBH inhomogeneity; as a result the barrier height measured by C–V is close to the weighted arithmetic average of the SBHs. Thus, the SBH determined from the zero-bias intercept assuming TE as current transport mechanism is well below the C–V measured BH and the weighted arithmetic average of the SBHs [29]. Geng et al. [30] reported that the pinholes come from the extended coreless dislocations, which were originating in the GaN buffer layer, resulting in a high leakage current and low BH. Conversely, much less dislocations or pinholes appear on the surface of sample, results low leakage current and high effective BH. Usually, C–V measurements are less prone to dislocations or pinholes, thus the determined barrier height is considered more reliable.

The cross-sectional bright field TEM images obtained from the Se/n-GaN Schottky contacts before and after annealed at 200 °C are shown in Fig. 4. For as-deposited Se/n-GaN Schottky contacts, Fig. 4a, it is observed that the Se film is amorphous in nature. After annealing at 200 °C, the Se film becomes fully crystallized as shown in Fig. 4b. This indicates that the increase in annealing temperature causes crystallized grains to grow toward the surface of the film. Such a crystallization progress of Se film upon RTA process is also confirmed by selected area electron diffraction (SAED) patterns (insets of Fig. 4). Specifically, for the as-deposited sample, the SAED patterns exhibited diffuse halos corresponding to the amorphous phase (indicated by arrows) (the inset of Fig. 4a). In particular, the indexing of SAED pattern (the inset of Fig. 4b) obtained from the Se/n-GaN Schottky contact upon annealing at 200 °C shown the presence of pure Se having hexagonal crystal structure. This indicates that Se film is not reacted with GaN substrate even after annealing at 200 °C.

As can be seen from Table 1, the barrier heights of Se/n-GaN Schottky diode decreased with increasing annealing temperature. Such annealing temperature dependency of the barrier height can be directly correlated with micro-structural change of Se film. With an increase in annealing temperature, it is observed the improvement in crystallinity of the Se film as evidenced from the TEM results (Fig. 4). Specifically, high resistance amorphous Se film is changed into low resistance crystalline Se film caused by annealing process [31–33]. This implies that the series resistance of Se/n-GaN Schottky diode decreases with increasing annealing temperature as shown in plots of *dV/d(lnI)* versus *I*, H(I) versus I (Fig. 2) and Norde method. In general, SBH is strongly affected by the series resistance. Wang et al. [34] demonstrated that the decrease in the barrier height could be associated with the decrease in series resistance. Also, Bhandari et al. [35] reported that the decrease in SBH could be ascribed to the decrease of series resistance. Therefore, it is concluded that the decrease in the barrier height of Se/n-GaN Schottky diode upon annealing temperature could be due to the decrease in the series resistance associated with a crystallization of Se film caused by annealing process.

Next, for Schottky diodes having interface states (N_{ss}) in equilibrium with semiconductor, the ideality factor n becomes greater than unity, as proposed by Card and Rhoderick [36] and it can be expressed as

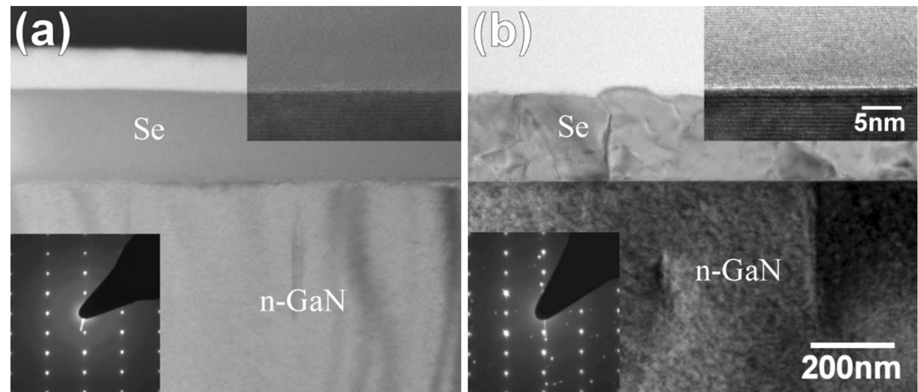

Fig. 4 Bright field TEM images taken from the Se/GaN Schottky diode (**a**) before and (**b**) after annealing at 200 °C. Corresponding TED patterns and HREM images obtained from the interface between Se and n-GaN are shown in *insets*

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}\right] \tag{12}$$

where ε_i and ε_S are the permitivities of interfacial layer and the semiconductor, W_d is the width of the space charge region $(W_D = \sqrt{2\varepsilon_s V_{bi}/qN_D})$ and δ its thickness. The voltage dependent ideality factor n(V) can be expressed as $n(V) = V/kT/q \ln(I/I_o)$ [37]. For Schottky diode having interface states in equilibrium with semiconductor, N_{ss} is given by

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \tag{13}$$

Moreover, in n-type semiconductor, the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of the semiconductor is given by [36]

$$E_C - E_{SS} = q(\phi_e - V) \tag{14}$$

where ϕ_e is the effective barrier height. The voltage dependence of the effective barrier height ϕ_e is given by [38]

$$\phi_e = \phi_b + \beta(V) \tag{15}$$

where

$$\beta = \frac{d\phi_e}{dV} = 1 - \frac{1}{n(V)} \tag{16}$$

The interface states density N_{ss} values as function of the bias are calculated using Eqs. (12) and (13). These values are converted to a function of $E_c - E_{ss}$ using Eq. (14). The bias dependence values of ideality factor and barrier height are taken into account from the forward bias current–voltage data of the Schottky diode for the calculation. The N_{ss} versus E_c-E_{ss} plots of Se/n-GaN Schottky diode as a function of annealing temperature is shown in Fig. 5. From Fig. 5, it is seen an increase in the interface state density from mid gap towards the bottom of the conduction band. The interface state density is calculated as 6.63×10^{13} eV^{-1} cm^{-2} for as-deposited,

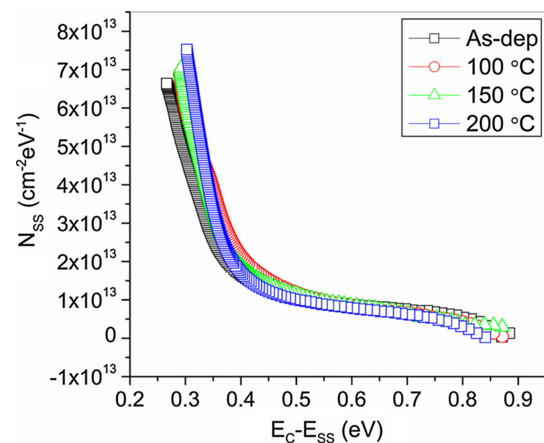

Fig. 5 Interface state density distribution profiles as a function of $E_c - E_{ss}$ for the Se/n-GaN Schottky diode at different annealing temperatures

6.89×10^{13} eV^{-1} cm^{-2} for 100 °C, 7.04×10^{13} eV^{-1} cm^{-2} for 150 °C, and 7.52×10^{13} eV^{-1} cm^{-2} for 200 °C, respectively. It is noted that the interface state density increases with increasing annealing temperature up to 200 °C. The interface states and interfacial layer between the metal and semiconductor play a significant role in the determination of Schottky barrier parameters of the devices.

Furthermore, it can be clearly seen in Fig. 1, as-deposited and annealed Se/n-GaN Schottky diodes shows the exponential dependence of reverse current (I_R) on applied reverse voltage (V_R), which strongly suggests that Poole–Frenkel or Schottky barrier lowering was operative in the Schottky junction. In other words, the plot of $\ln(I_R)$ versus $V_R^{1/2}$ (Fig. 6), for the Se/n-GaN Schottky diode shows a linear variation irrespective of annealing temperature, indicating the possibility of the existence of the domination of Poole–Frenkel emission and Schottky emission on the reverse current. The current through the diode when dominated by Schottky barrier lowering effect is given by [39, 40]

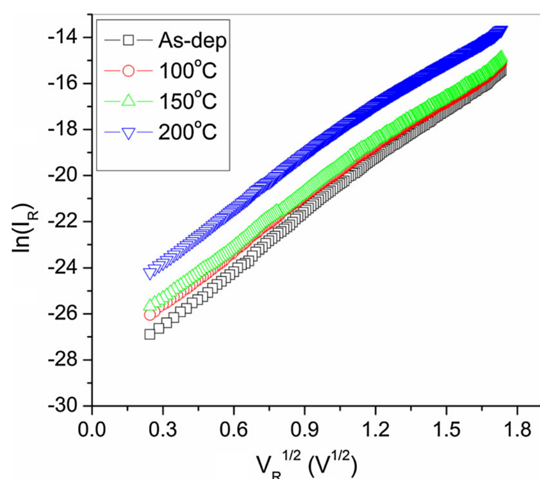

Fig. 6 Plot of $\ln(I_R)$ versus $V_R^{1/2}$ for the Se/n-GaN Schottky diode at different annealing temperatures

$$I_R = A^*AT^2 \exp\left(\frac{-\phi_S}{kT}\right) \exp\left(\frac{\beta_{SC} V^{1/2}}{kTd^{1/2}}\right) \quad (17)$$

and the Poole–Frenkel barrier lowering effect is given by

$$I_R = I_0 \exp\left(\frac{\beta_{PF} V^{1/2}}{kTd^{1/2}}\right) \quad (18)$$

where d is the depletion width, and β_{PF} and β_{SC} are the Poole–Frenkel and Schottky field lowering coefficients, respectively. The theoretical values for β_{PF} and β_{SC} are given by

$$2\beta_{SC} = \beta_{PF} = \left(\frac{q^3}{\pi\varepsilon_o\varepsilon_r}\right)^{1/2} \quad (19)$$

where q is the electric charge, ε_r the relative permittivity of the semiconductor and ε_o the permittivity of the free space. The theoretical values of Poole–Frenkel field-lowering coefficient (β_{PF}) and the Schottky field-lowering coefficients (β_{SC}) for Se/n-GaN Schottky diode are $\beta_{PF} = 2.46 \times 10^{-5}$ eV m$^{1/2}$ V$^{-1/2}$ and $\beta_{SC} = 1.23 \times 10^{-5}$ eV m$^{1/2}$ V$^{-1/2}$. A plot of $\ln(I_R)$ versus $V_R^{1/2}$ for Se/n-GaN Schottky diode at different annealing temperatures is shown in Fig. 6. The experimental values of field-lowering coefficients determined from the slope of the linear region of the plot of $\ln(I_R)$ versus $V_R^{1/2}$ are 1.55×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ for as-deposited, 1.36×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ for 100 °C, 1.34×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ for 150 °C and 1.21×10^{-5} eV m$^{1/2}$ V$^{-1/2}$ for 200 °C, respectively. The comparison of the experimental and theoretical slopes revealed that the experimental slopes determined are close to the theoretical values of β_{SC}. This suggests that irrespective of annealing temperatures, the reverse leakage current of Se/n-GaN Schottky diode is dominated by the Schottky lowering mechanism, where current conduction in reverse bias occurs through the Se/n-GaN interface rather than from the bulk material.

4 Summary

In conclusion, the electrical and microstructural properties of Se/n-GaN SBD have been investigated using I–V, C–V and TEM measurements at different annealing temperatures in the range of 100–200 °C. The Se/n-GaN Schottky contact showed a good rectification behavior at all annealing temperatures. It is observed that the SBH of the Se/n-GaN Schottky diode decreases from 0.94 eV (I–V), 1.55 eV (C–V) to 0.90 (I–V), 1.33 eV (C–V) before and after annealing at 200 °C. The Cheung's method is used to calculate the series resistance of the Se/n-GaN Schottky diodes and values are in good agreement with each other. It is observed that the series resistance decreases with the increasing annealing temperature. TEM results show that the Se film become fully crystallized after annealing at 200 °C compared to the as-deposited Se film. The decrease in the series resistance of Se/n-GaN Schottky diode with increasing annealing temperature could be related to the phase transformation from high resistance amorphous Se to low resistance crystalline Se. This could be responsible for the decrease in barrier height of Se/n-GaN Schottky diode upon annealing at 200 °C. Further, the discrepancy between SBHs obtained from I–V and C–V measurements is also explained. The interface state density is found to be increased with increasing annealing temperatures. Moreover, the Schottky conduction mechanism is found to be dominant in the reverse bias region of Se/n-GaN Schottky diode at all annealed temperatures.

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