Direct formation of AuNPs thin film using thermal evaporated zinc as sacrificial template in hydrothermal method

S. A. Ng · K. A. Razak · L. P. Goh ·
K. Y. Cheong · P. C. Ooi · K. C. Aw

Abstract This work describes the properties of gold nanoparticles (AuNPs) embedded in polymethylsilsesquioxane (PMSSQ) as an organic dielectric layer. AuNPs were grown on this dielectric layer via the sacrificial hydrothermal process using ZnO seeded template prepared by thermal evaporation. Template prepared by using the thermal evaporation method has advantages in terms of ease of fabrication and cost compared to previous work, which the template was prepared by using sputtering method. The effect of annealing temperature on the ZnO seeded template was investigated. The effect of template on structural and electrical properties of the grown AuNPs was studied by field-emission scanning electron microscope, X-ray diffraction and semiconductor characterization system. Metal–insulator-semiconductor device with embedded AuNPs was proven to exhibit memory effect. Optimum memory properties of AuNPs embedded in PMSSQ was obtained for AuNPs grown on the Zn seeds template annealed at 350 °C with the lowest threshold voltage at 3.7 V in current–voltage characteristics, and could store 49 electrons per Au nanoparticle. This indicated that uniform AuNPs in combination with the size and area density contributed to excellent memory effect.

1 Introduction

Gold nanoparticles (AuNPs) have been widely used in biosensors and electronic applications. For biosensors applications, AuNPs can be in the form of colloidal or thin film whereby AuNPs can be conjugated to biomolecules such as antibody, DNA or protein [1, 2]. For electronic applications, AuNPs has been used to enhance conductivity of devices and storage properties in organic memory devices [3, 4]. Recently, non-volatile memory devices embedded with nanoparticles materials as charge trapping layer become attractive due to its high current density, large ON/OFF current ratio and other excellent performances [4]. Among all materials, AuNPs is the most promising material due to its good trap sites as electrons acceptors [5]. In addition, the AuNPs is chemically stable and also has wide work function as it provides higher confinement barrier for the retention mode and smaller barrier for the programming and erasing modes.

There are a few methods to deposit or grow AuNPs on Si substrates. Park et al. [6] have deposited AuNPs embedded in the insulator of memory devices by spin coating technique. However, this technique caused nonuniform distribution of AuNPs due to centrifugal effect [7]. This could lead to memory device properties become inconsistent. Besides that, Leong et al. [8] have studied the controlled synthesis of various metallic nanoparticles using polystyrene-block-poly(4vinyl pyridine) (PS-P4VP) diblock copolymer micelles. This method was based on the assembling of micelle embedded metallic nanoparticles on the substrate followed by oxygen plasma treatment to

S. A. Ng · K. A. Razak (✉) · L. P. Goh · K. Y. Cheong
School of Materials and Mineral Resources Engineering,
Universiti Sains Malaysia, 14300 Nibong Tebal, Penang,
Malaysia
e-mail: khairunisak@eng.usm.my; khairunisak@usm.my

K. A. Razak
NanoBiotechnology Research and Innovation, INFORMM,
Universiti Sains Malaysia (USM), 11800 Penang, Malaysia

P. C. Ooi · K. C. Aw
Mechanical Engineering, The University of Auckland,
Auckland, New Zealand

remove the polymer template. However, contamination could occur in this treatment.

There are several works reported on the deposition of colloidal metallic nanoparticles on a substrate by electrostatic interaction between metallic nanoparticles and adhesion layer. The colloidal metallic nanoparticles were produced through chemical reduction approach prior to deposition. These colloidal metallic nanoparticles were then assembled on modified surface of the substrate (amine-terminated substrate modification) [9–12]. For example, Lee et al. utilized polyelectrolytes with positive charge poly(allyl-amine hydrochloride) (PAH) and negative charge of poly(styrenesulfonate) (PSS) with negative charge AuNPs. The PAH/PSS/PAH multilayer and AuNPs were deposited through layer-by-layer (LBL) self-assembly method [5]. Zhang et al. [11] also reported the work on fabrication and characterization of AuNPs thin film on aminosilane functionalized substrate via LBL assembly. However, this method revealed more prominent particle agglomeration with increasing number of assembly layers that could cause defect of memory device.

Other than that, a metallic nanoparticle layer can be fabricated by depositing a very thin metallic layer followed by a post-annealing process in order to obtain agglomerated metallic nanoparticles through Ostwald ripening [5]. However, contamination could occur in the stacking structure and diffusion of metallic components to the interfaces of the memory devices during synthesis of metallic nanoparticles [5]. This could affect the electrical properties of the memory devices.

Previously, in Goh et al. [13] work, AuNPs was successfully formed directly on substrates using a novel method known as a sacrificial template in hydrothermal reaction by using a ZnO seeded template. ZnO template was prepared through sputtering method followed by thermal oxidation. Through this method, uniform size and good distribution of AuNPs with a simple equipment set-up was produced. The properties of AuNPs were dependent on heat treatment temperature of ZnO seeds. The effects of AuNPs distribution embedded in PMSSQ layers in memory application showed promising result compared to other reported works. However, there is lack of study in this method especially on the effect of various approaches to deposit template.

In this study, ZnO template was prepared using thermal evaporation method followed by an annealing process to produce seeds template before subjected to hydrothermal reaction. The effect of annealing temperature on the morphology and physical properties of AuNPs were systematically studied. For memory properties study, a MIS memory device in the form of gold/insulator/AuNPs/insulator/n-type silicon/aluminum structure was fabricated. The possible conduction mechanisms through the insulators memory devices were proposed.

2 Experimental details

In this work, 1×1 cm n-type $\langle 100 \rangle$ silicon wafer was used as substrates. The substrates were cleaned by using a standard Radio Corporation of America (RCA) cleaning procedures to remove organic and inorganic contaminants. The RCA cleaning consists of the following steps: The first step involves organic cleaning with 1:1:5 ratio mixture of 37 % hydrogen peroxide: 28 % ammonium hydroxide: distilled water. Si substrates were immersed in the solution at 80 °C for 10 min. After that the substrates were rinsed in distilled water. The second step involves oxide removal on the Si substrates by soaking in 1:50 of hydrofluoric acid and distilled water in a polypropylene beaker, followed by rinsed with distilled water. Then, Si substrates were subjected to ionic cleaning in a 1:1:6 ratio mixture of 49 % hydrochloric acid: 37 % hydrogen peroxide: distilled water at 80 °C for 10 min and rinsed with distilled water. The substrates were left in distilled water for 5 min and dried using N_2 gas.

A layer of 250 nm thick polymethylsilsesquioxane (PMSSQ 1) was deposited by spin coating at 2,000 rpm for 60 s. Then, the substrates were cured at 160 °C for 1 h to crosslink the PMSSQ. Then 200 nm zinc thin film was deposited using the evaporation method on the substrates. The substrates were annealed at 200, 300, 350 and 400 °C with the ramp rate and soaking time of 5 °C/min and 10 min, respectively. The substrates were then subjected to hydrothermal reaction in a preheated oven at 80 °C for 4 h. The hydrothermal bath contained 0.1 M zinc nitrate tetrahydrate [$Zn(NO_3)_2 \cdot 4H_2O$], 0.1 M hexamethylenetetramine ($C_6H_{12}N_4$), 0.01 M gold (III) chloride trihydrate ($AuCl_4 \cdot 3H_2O$) and 10 ml acetic acid. After hydrothermal reaction, the samples were removed and rinsed with deionised water. The samples were dried in an oven at 110 °C for 12 h to ensure complete removal of water in the PMSSQ layer. The samples were then characterized using a field-emission scanning electron microscope (FESEM) model LEO Gemini equipped with energy dispersive X-ray spectrometer (EDX) with model ZEISS SUPRA^{TM} 35VP. The phases presence was analyzed using X-ray diffractometer (XRD) Bruker D8. For memory properties analysis, a 250 nm second layer of polymethylsilsesquioxane (PMSSQ 2) was spin coated and cured at 160 °C for 1 h. A gold top and aluminum bottom contacts were deposited using a thermal evaporation method with the aid of a shadow mask. The electrical characteristics capacitance–voltage (C–V) and current–voltage (I–V) of the device were measured using a semiconductor characterization system Keithley Model 4200-SCS.
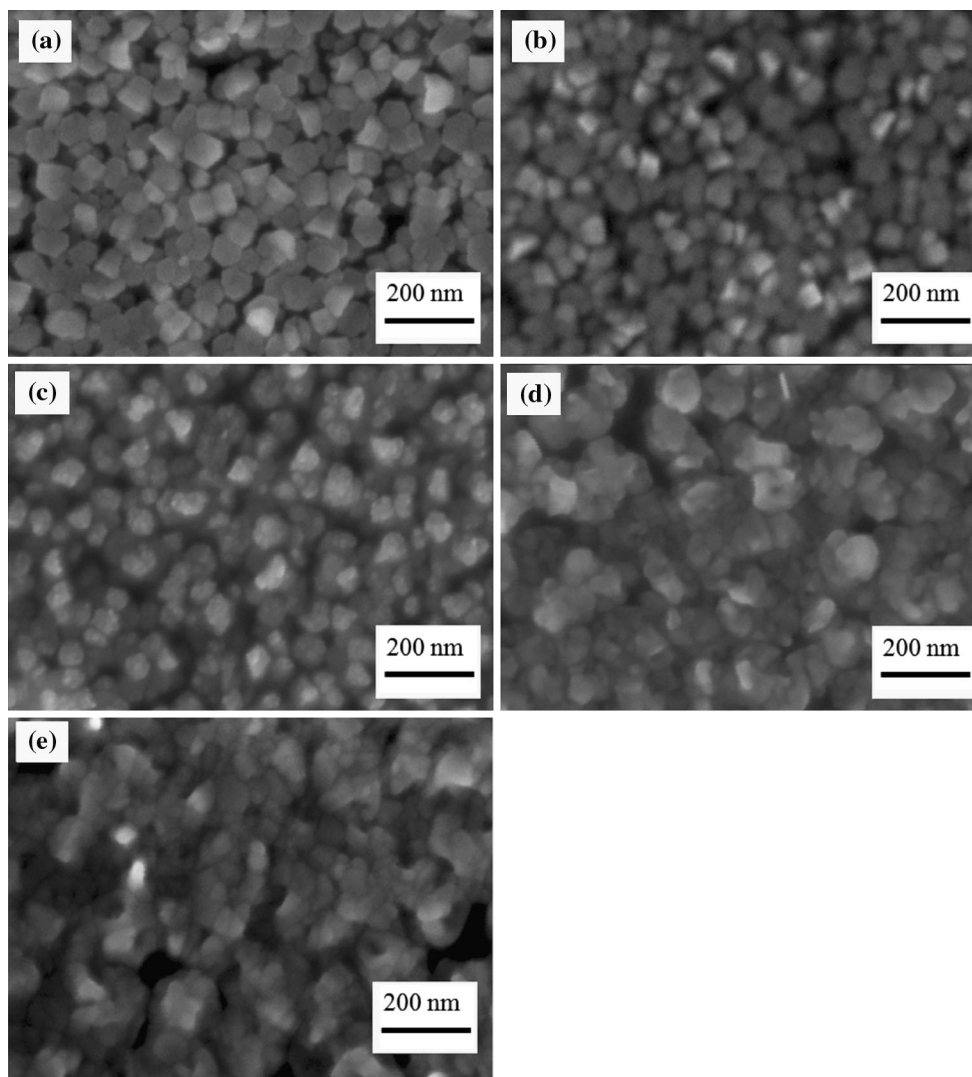
Fig. 1 SEM images of evaporated Zn seeded template with varying annealing temperature. **a** Non-annealed, **b** 200 °C, **c** 300 °C, **d** 350 °C and **e** 400 °C

3 Result and discussion

AuNPs was successfully grown on the seeded substrates using the hydrothermal method. Figure 1 shows SEM images of Zn or ZnO seeds template with varying annealing temperature. ImageJ software was used in order to measure the grain size of Zn or ZnO seeds as listed in Table 1. For the non-annealed Zn template, the grain size is 65 ± 6 nm. After annealing at 200, 300, 350, and 400 °C the grain sizes become 65 ± 9, 69 ± 9, 111 ± 13 and 135 ± 12 nm, respectively. The grain size of ZnO seeds becomes larger with increasing annealing temperature due to internal atomic diffusion, which promotes the grain growth and pore elimination. The increasing thermal energy input causes further surface texture restructuring due to grain boundary diffusion and bulk diffusion. The

Table 1 Summary of grain size for Zn or ZnO seeds

Annealing temperature (°C)	Non-annealed	200	300	350	400
Grain size for Zn or ZnO seeds (nm)	65 ± 6	65 ± 9	69 ± 9	111 ± 13	135 ± 12

high temperature can enhance the migration of grain boundaries and cause the coalescence of more grains during the annealing processes [14].

XRD spectra of Zn template with varying annealing temperature are shown in Fig. 2. Two important peaks were observed in the non-annealed Zn template at 36° and 39° indicated that Zn hexagonal structure exists as ascribed

Fig. 2 XRD spectra of evaporated Zn template with varying annealing temperature. *a* Non-annealed, *b* 200 °C, *c* 300 °C, *d* 350 °C and *e* 400 °C
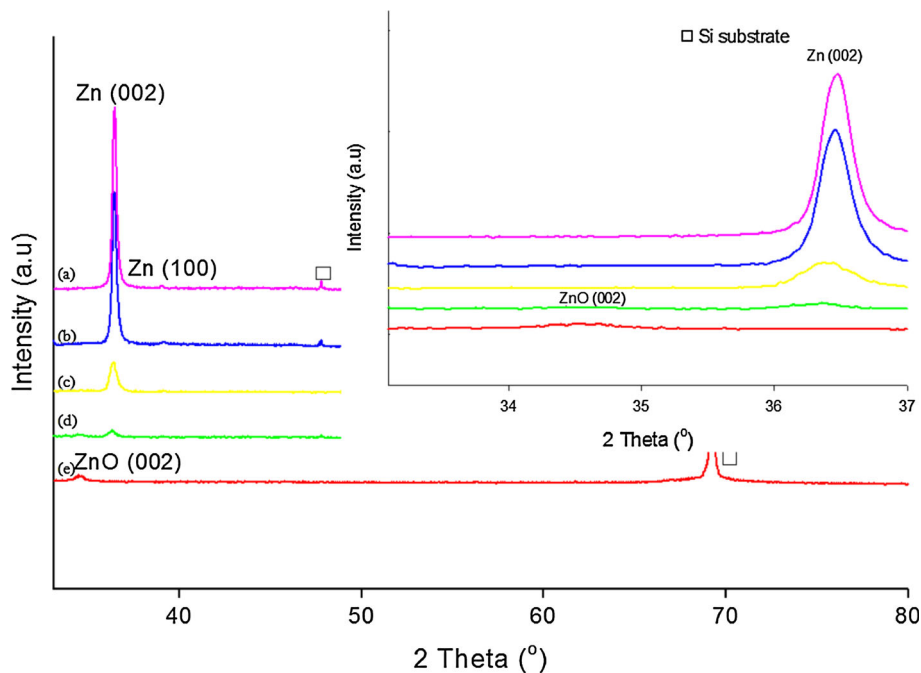
to ICDD 03-065-3358. For the Zn template annealed at 200 °C, there is no significant changes in XRD result. However, the Zn peak intensities of template annealed at 300 °C decreased drastically. For the template annealed at 350 °C, Zn peak intensities decreased and ZnO (002) peak at 34° that is ascribed to ICDD 01-080-0075 was observed. Similar finding was also discussed by Gupta et al. [15], the coexistence of Zn and ZnO peaks for Zn template annealed at 350 °C revealed incomplete oxidation of Zn thin film, which was prepared through the evaporation method. This is dependent on oxidation temperature of ZnO film. The intensity ratio of Zn to ZnO peaks in XRD changes with the oxidation temperature shows multiple mechanisms of nucleation and growth for ZnO in these films. After annealing at 400 °C, Zn peak disappeared and only ZnO phase was formed. This indicated that Zn was fully oxidized and formed more ordered structure ZnO.

After hydrothermal reaction, AuNPs thin film was formed on the substrates. The morphology of AuNPs is shown in Fig. 3. For the non-annealed Zn seeds template, rough and dense AuNPs with 117 ± 15 nm particle size was observed. For AuNPs grown on the seeds template annealed at 200 °C, the particle size of AuNPs is 117 ± 19 nm. The surface of AuNPs is smoother compared to the AuNPs grown on the non-annealed template sample. The size of AuNPs grown on the 300 °C annealed seeds template is 118 ± 20 nm. The distance between the AuNPs is farther compared to the sample grown on the 200 °C annealed seeds template. For the AuNPs grown on the 350 °C annealed seeds template, the size of AuNPs increased to 176 ± 33 nm, but the particles density

decreased and the distance between the AuNPs became larger. The AuNPs became even larger in size (320 ± 41 nm) with decreasing area density for the sample grown on the 400 °C annealed seeds template. It is known that a fully cured PMSSQ shows low moisture absorption and exhibits good thermal stability up to 500 °C [16]. A cross-section of AuNPs grown on 400 °C annealed seeds template sample is shown in Fig. 3f, proven that the first PMSSQ layer survived at a relatively high temperature annealing and moisture (hydrothermal reaction process).

The sizes of AuNPs are listed in Table 2. The effect on AuNPs growth was not observed for the non-annealed and 200 °C annealed template due to incomplete oxidation of Zn template to ZnO. However, the relationship between grain size of template and AuNPs size was indirectly proportional. The size of AuNPs growth is dependent on the formation of ZnO template. The area density of AuNPs is related to the seeded size of template annealed higher than 350 °C. Hence, the smaller the grain size of ZnO, the higher area density of AuNPs can be produced due to the presence of more grain boundaries for Au nucleation. Elemental analysis using EDX for the sample grown on 350 °C annealed template is shown in Table 3. The gold element was observed but the Zn element was absent. Therefore, it is assumed that ZnO template dissolved into the hydrothermal bath solution during hydrothermal reaction. Similar elements were observed in the samples grown on other heat treated templates.

The XRD spectra of AuNPs grown on template annealed at various temperatures are shown in Fig. 4. Figure 4a is the control sample of PMSSQ thin film whereby Si peaks

Fig. 3 SEM images of AuNPs grown on template annealed with varying temperatures. **a** Non-annealed, **b** 200 °C, **c** 300 °C, **d** 350 °C, **e** 400 °C and **f** cross-section of 400 °C
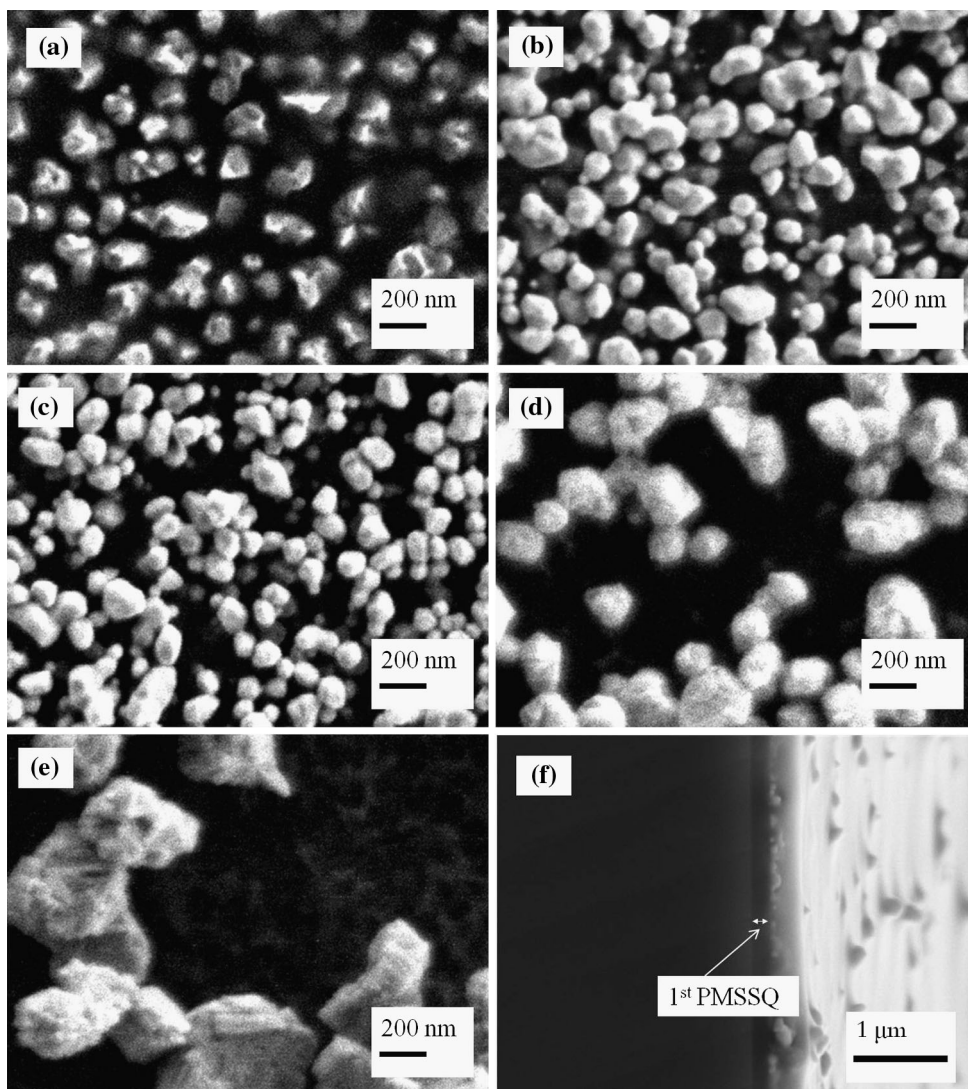

Table 2 Summary of size and area density for AuNPs

Samples	Size of AuNPs	Area density (cm^{-2})
Non-annealed	117 ± 15	2.71 × 10^9
200 °C	117 ± 19	4.06 × 10^9
300 °C	118 ± 20	3.78 × 10^9
350 °C	176 ± 33	1.17 × 10^9
400 °C	320 ± 41	4.31 × 10^8

Table 3 EDX analysis of the samples grown by using Zn template annealed at 350 °C

Element	At.%
C K	24.98
O K	10.37
Si K	58.19
Au M	06.46

were observed. For AuNPs grown on the non-annealed, 200, 300, 350 and 400 °C annealed templates gold peaks; (111), (200) and (220) were observed at 38.3°, 44.5° and 65°, respectively that could be assigned to gold with ICDD 00-001-1172. Zn or ZnO related peaks were not observed for all samples that proved that complete dissolution of template during hydrothermal reaction as determined by EDX analysis.

In order to measure the electrical properties of the sacrificial hydrothermal growth AuNPs thin film, 250 nm second layer of PMSSQ was spin coated on top of the AuNPs layer. Au top and Al bottom contacts, respectively, were evaporated with a shadow mask. The *I–V* characteristics of the AuNPs embedded in PMSSQ are shown in Fig. 5. *I–V* measurements were obtained through voltage sweep from 0 V to 10 V then back to 0 V. To explain the possible electron transport mechanisms through the insulator layers, the *I–V* curves are marked with three distinct
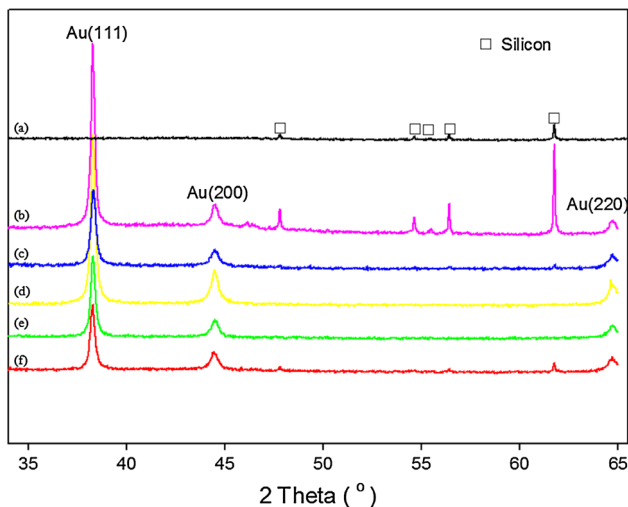
Fig. 4 XRD spectra of the samples after hydrothermal reaction on template annealed with varying temperatures. *a* PMSSQ, *b* 400 °C, *c* 350 °C, *d* 300 °C, *e* 200 °C and *f* non-annealed

regions (I, II and III). The *I–V* relationship can be expressed as $I \propto V^n$ and *n* can be determined by fitting the double log plot. The energy-band diagrams representing the transport mechanism of electron injection from Si to PMSSQ and trapped in AuNPs are shown in Fig. 6. These transport mechanisms are comparable with previous report on AuNP-memory device [17].

In Fig. 5a, the sample fabricated without AuNPs embedded in PMSSQ acted as a control sample. A negligible hysteresis window was observed when the voltage was swept from 0 to +10 V (with respect to Al bottom contact) and vice versa from the reverse swept from +10 to 0. *I–V* results in Fig. 5b–f show hysteresis windows were observed in all samples. When forward voltage was swept, an abrupt increase in current was observed at threshold voltage, V_{th}. At low voltage in region I for all cases, the thermionic emission (TE) current conduction is a common occur mechanism which is related with the thermally generated electrons due to the TE is a process of heat-induced electrons emitted across a barrier. At this low voltage region (region I), electron tunneling mechanism is unlikely to occur in the 250 nm thick PMSSQ layer. However, the electron could be transported over the metal–insulator interface via Schottky and Poole–Frenkel emissions due to the obtained experimental data in region I are well fitted to log $(I/T^2) \propto V^{0.5}$ and log $(I/V) \propto V^{0.5}$, respectively for Schottky and Poole–Frenkel emissions mechanism. However, thick PMSSQ could limit the Schottky and Poole–Frenkel emissions. Therefore, possible explanation is the electrons from Si are transported across the barrier due to thermionic effect via field-assisted lowering at Si–PMSSQ interface with the combination of Poole–Frenkel and Schottky emission effect, based on

field-enhanced thermal emission of trapped electrons in the PMSSQ into the AuNPs. Similar result was observed for AuNPs deposited using a spin coating technique [17].

As the voltage increased to V_{th}, electrons started to be trapped at the AuNPs sites until all sites are filled (region II), and this transport mechanism is believed to be trapped-charge-limited-current (TCLC) with the slope value of n is greater than 2 (n ≫ 2). This corresponds to the non-ohmic region and indicates the existence of deep traps [17]. For higher voltage in region III, further carrier injection would fill all trap centres and thus trap-free space charge limited conduction would become dominant in region III. The value of n = 2 from the *I–V* characteristic (I/V^n) suggests the onset of a trap free space-charge-limited conduction. Therefore, the *I–V* at this region represents the trap-free space-charge-limited current (SCLC) mechanism [17]. During the reverse sweep, current flows through the device is higher than when forward sweep because the traps have been filled and obeys SCLC transport mechanism. This shows that electrons can be stored and retained, thereby, proven the existence of memory effect for the embedded AuNPs memory device samples. Similar result was observed by Montero et al. [18]. The V_{th} for each samples are tabulated in Table 4. The sample grown on the ZnO template annealed at 300 °C showed the largest hysteresis. The result is attributed to uniform AuNPs distribution and size as observed in Fig. 3c. However, the sample with AuNPs grown on the template annealed at 350 °C shows an abrupt increased at 3.7 V, which is the lowest V_{th} observed among all samples. This is due to the AuNPs being more sparsely distributed that contributed to excellent memory effect.

Capacitance–voltage (*C–V*) characteristics of the AuNPs embedded in PMSSQ using ZnO template annealed at various temperatures are shown in Fig. 7. The *C–V* characteristics for all samples were obtained by sweeping voltage on the Au top contact with respect to the bottom Al contact from −10 to +10 V and then back to −10 V. The *C–V* plot of the control sample in Fig. 7a shows ignorable size of hysteresis window. The *C–V* plots in Fig. 7b–d show minor hysteresis suggesting little charge trapping. However, the *C–V* plot in Fig. 7e, f show larger hysteresis suggesting the AuNPs contributed to charge trapping. This is supported by other studies [5, 19]. This indicated as that the hysteresis observed in AuNPs–PMSSQ layer MIS structure is mainly due to the charge trapping at the AuNPs and not due to the PMSSQ layer.

For the sample prepared on the non-annealed template, the hysteresis (flat band voltage shift, ΔV_{FB}) is 0.4 V, which is the smallest hysteresis. The samples prepared on 200 °C and 300 °C annealed templates have 0.6 V hysteresis window. This similarity was due to the size of the AuNPs prepared from both temperatures are almost same. ΔV_{FB} of the
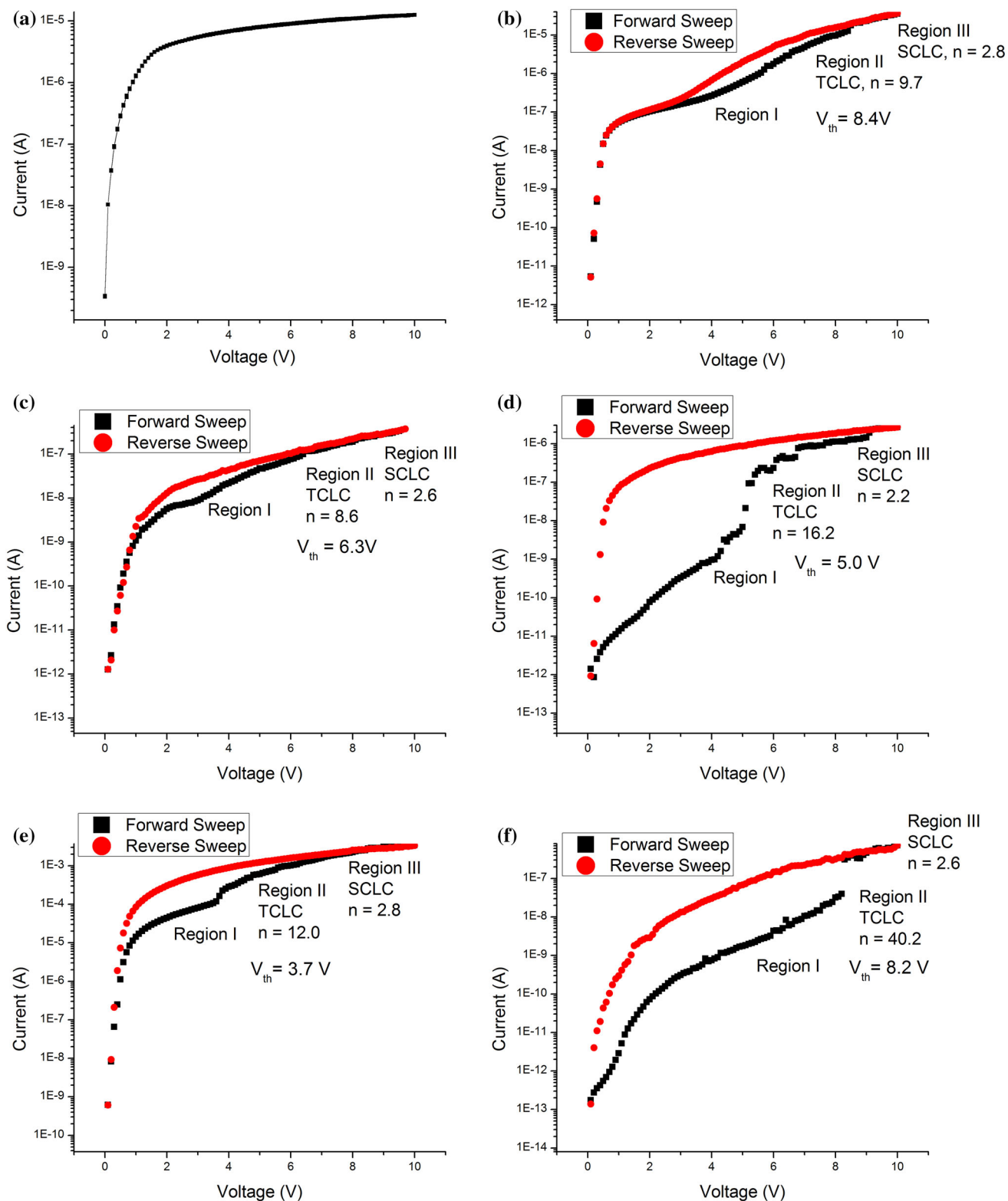
Fig. 5 *I–V* charateristics of PMSSQ without AuNPs (control sample) and AuNPs embedded in PMSSQ. AuNPs were grown on Zn template with varying annealing temperatures. **a** Control sample, **b** non-annealed, **c** 200 °C, **d** 300 °C, **e** 350 °C and **f** 400 °C. *Y scale* in log scale

Fig. 6 Energy band diagram. The band diagram describes the electron flows and trap occurs when the positive bias on the Au top electrode with respect to the Al bottom contact. **a** Forward sweep and **b** reverse sweep. Electrons are illustrated as *filled circle*
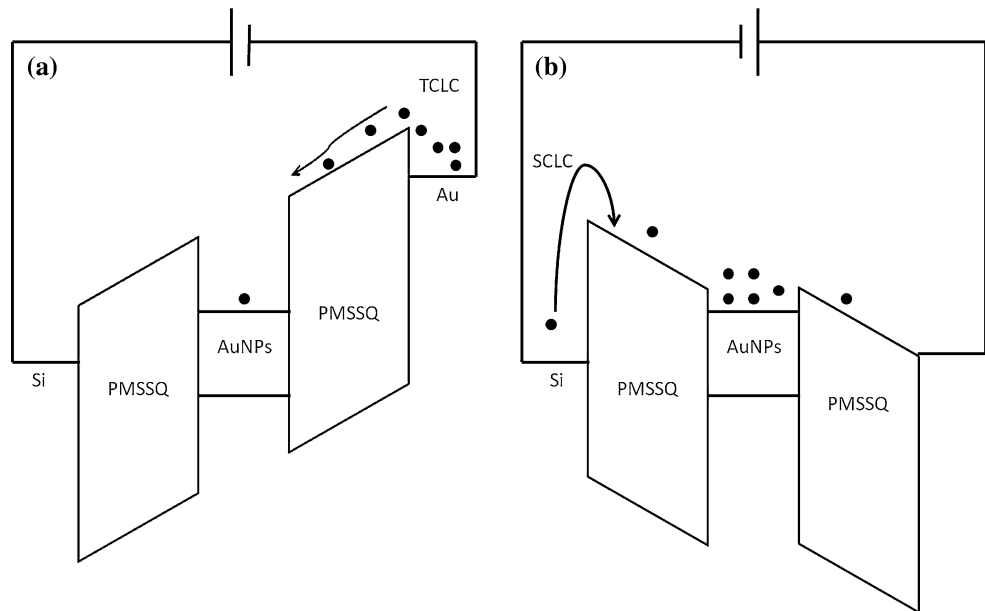
Table 4 *I–V* measurement obtained for AuNPs embedded PMSSQ with varying annealing temperature of Zn template

Samples	Region I	Region II	Region III	V_{th}	Size of AuNPs
Non annealed	Thermionic emission, Schottky emission, Poole–Frenkel emission	TCLC n = 9.7	SCLC n = 2.8	8.4 V	117 ± 15
200 °C	Thermionic emission, Schottky emission, Poole–Frenkel emission	TCLC n = 8.6	SCLC n = 2.6	6.3 V	117 ± 19
300 °C	Thermionic emission, Schottky emission, Poole–Frenkel emission	TCLC n = 16.2	SCLC n = 2.2	5.0 V	118 ± 20
350 °C	Thermionic emission, Schottky emission, Poole–Frenkel emission	TCLC n = 12.0	SCLC n = 2.8	3.7 V	176 ± 33
400 °C	Thermionic emission, Schottky emission, Poole–Frenkel emission	TCLC n = 40.2	SCLC n = 2.6	8.2 V	320 ± 41

sample grown on the 350 and 400 °C annealed template are 1.6 and 0.6 V, respectively. The sample grown on 350 °C annealed template has the largest hysteresis window due to the less agglomeration and isolated distribution (Fig. 3d).

The charge storage capacity per AuNP was calculated based on the equations that have been used by Goh et al. [13]. The charge storage of each samples is tabulated in Table 5. AuNPs grown on the non-annealed, 200 and 300 °C annealed substrates have similar charge storage capability (six electrons per Au nanoparticle). This was due to the size of AuNPs for these samples are almost similar (Fig. 3a–c) which is around 118 nm and 3.5×10^{-9} cm^{-2} of area density. Besides that, number of electrons stored per Au nanoparticle for the sample grown on 350 °C annealed template is 49. As observed in SEM image (Fig. 3d), the AuNPs are distributed quite far from each other with size 176 ± 33 nm.

It can be seen that AuNPs grown on the 400 °C annealed template (size is 320 ± 41 nm) can store 67 electrons per Au nanoparticle with a smaller hysteresis loop compared to the sample grown on 350 °C annealed template. This is due to the size and area density of AuNPs distributed in the samples. This study is in agreement with Tseng and Tao [20], whereby

particle size affects the memory window. In their study, AuNPs was embedded in the conduction channel of a pentacene film-based field-effect transistor. The AuNPs capped with organic self-assembled monolayer serves as a floating gate through trapping carrier charges into the particles. Larger particles were expected to store more charge than smaller ones [20]. The number of stored charge per single Au nanoparticle was obtained through calculation of stored charge density divided by area density, which is represented as nd$_{nanoparticle}$/d$_{nanoparticle}$. The number of stored charge per single Au nanoparticle is inversely proportional to area density of AuNPs in the sample, so, the number of stored charge is larger when area density is smaller. However, the AuNPs grown on 400 °C sample cannot be considered as the optimum memory by considering the *I–V* result and the distribution of AuNPs on the samples through SEM images. In *I–V* result of AuNPs grown on 400 °C template, very high voltage (abrupt increased current) at 8.2 V is required in order to turn on the device. Besides that, the distribution of AuNPs grown on 400 °C template is not uniform that may cause inconsistent memory properties.

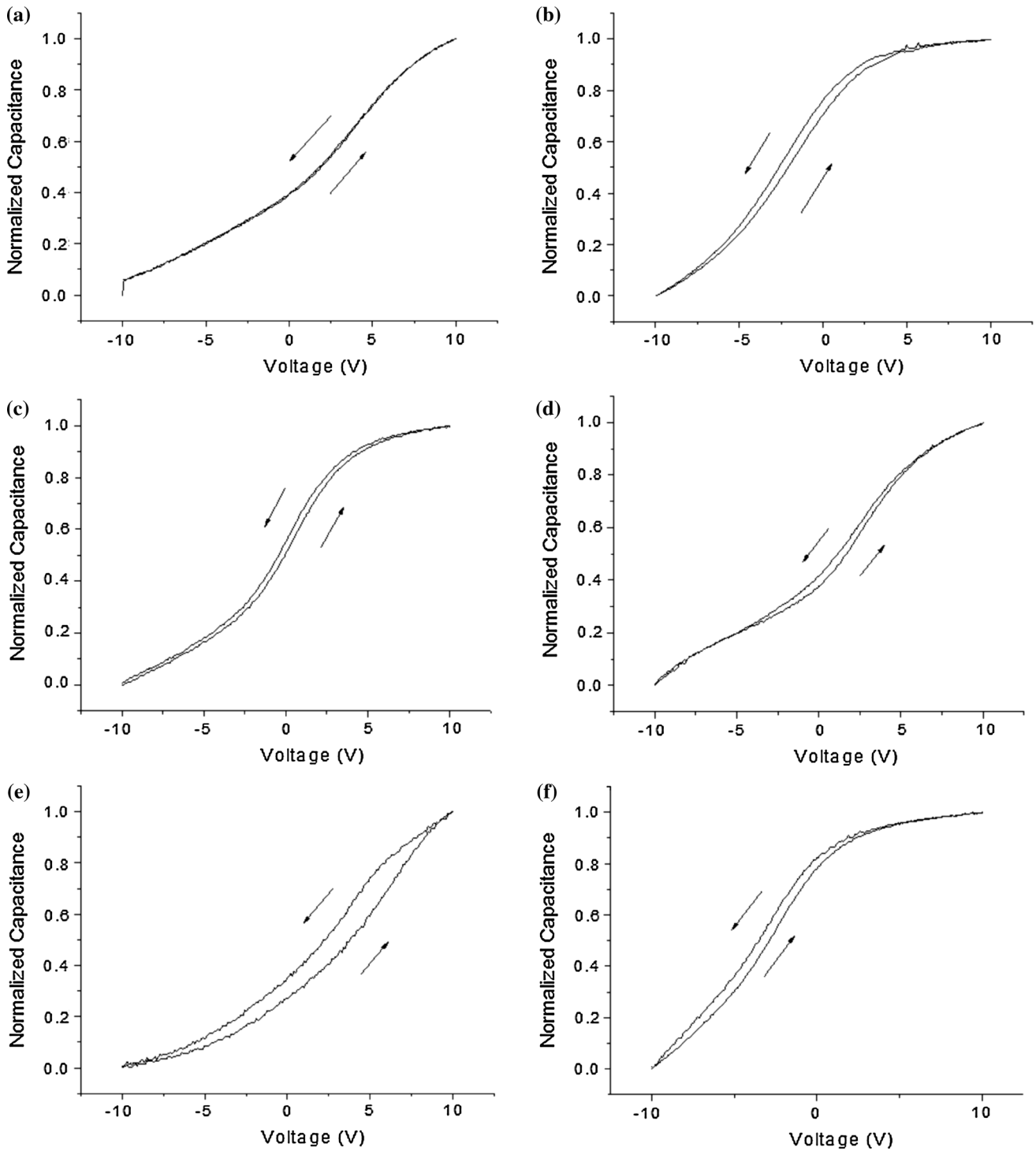In this study, optimum memory properties of AuNPs embedded PMSSQ was obtained for AuNPs grown on the

Fig. 7 C–V characteristics of PMSSQ without AuNPs (control sample) and AuNPs embedded in PMSSQ. AuNPs were grown on Zn template with varying annealing temperatures. **a** control sample, **b** non-annealed, **c** 200 °C, **d** 300 °C, **e** 350 °C and **f** 400 °C

ZnO seeds template annealed at 350 °C. This is due to the lowest turn on voltage (abrupt increased current) at 3.7 V in I–V characteristics although there are only 49 electrons stored per Au nanoparticle in C–V measurement. This indicated that uniform AuNPs in combination with the size

and area density contributed to excellent memory effect. In the work of Goh et al. [13], device with AuNPs grown on the ZnO seed template annealed at 300 °C can store 54 electrons per Au nanoparticle, which is better than the optimum result in this study which is 49 electrons per Au

Table 5 *C-V* measurement obtained for AuNPs embedded PMSSQ with varying annealing temperature of Zn template

Annealing temperature (°C)	Control sample	Non-annealed	200	300	350	400
Flat-band voltage shift, ΔV_{FB} (V)	0	0.4	0.6	0.6	1.6	0.6
Amount of electrons stored per AuNPs	0	6	6	6	49	67

nanoparticle for device with AuNPs grown on the ZnO seed template annealed at 350 °C. This is due to the distribution of AuNPs prepared through sputtering approach template is better than evaporation approach. The results proved that the presence of isolated AuNPs is important to obtain optimum memory properties. However, in terms of ease of fabrication and cost, thermal evaporation is better than sputtering method to produce ZnO template. Further work on synthesis parameters optimization such as study on the effect precursor concentration and time of hydrothermal reaction could be beneficial to tune the distribution of AuNPs that will enhance memory properties.

4 Conclusion

AuNPs were successfully grown on the Zn seeded template produced through the thermal evaporation followed by sacrificial hydrothermal process. The thermal evaporation method to prepare the template is favorable due to ease of fabrication and low cost compared to previous work that prepared through sputtering method The size and distribution of AuNPs were dependent on the annealing temperature of ZnO template due to AuNPs nucleated and grown at ZnO seeds grain boundaries. Optimum memory properties of AuNPs embedded PMSSQ was obtained for AuNPs grown on the ZnO seeds template annealed at 350 °C with the lowest turn on voltage (abrupt increased current) at 3.7 V in *I–V* characteristics and 49 electrons stored per Au nanoparticle in *C–V* measurement. This indicated that uniform AuNPs in combination with the size and area density contributed to excellent memory effect.

References

1. K. Saha, S.S. Agasti, C. Kim, X. Li, V.M. Rotello, Chem. Rev. **112**, 2739 (2012)
2. S. Su, X. Zuo, D. Pan, H. Pei, L. Wang, C. Fan, W. Huang, Nanoscale **5**, 2589 (2013)
3. D. Prime, S. Paul, P.W. Josephs-Franks, Philos. Trans. R. Soc. A **367**, 4215–4225 (2009)
4. T.W. Kim, Y. Yang, F. Li, W.L. Kwan, NPG Asia Mater. **4**, e18 (2012)
5. J.-S. Lee, Gold. Bull. **43**, 189 (2010)
6. B. Park, K. Cho, H. Kim, S. Kim, Semicond. Sci. Technol. **21**, 975 (2006)
7. A. Das, S. Das, A.K. Raychaudhuri, B Mater. Sci **31**, 277 (2008)
8. W.L. Leong, N. Mathews, S.G. Mhaisalkar, T.P. Chen, P.S. Lee, Appl. Phys. Lett. **93**, 222908 (2008)
9. W.K. Lee, H.Y. Wong, K.C. Aw, Microelectron. Eng. **88**, 2837 (2011)
10. V. Shakila, K. Pandian, J. Solid State Electrochem. **11**, 296 (2007)
11. F. Zhang, M.P. Srinivasan, J. Colloid Interface Sci. **319**, 450 (2008)
12. B. Flavel, M. Nussio, J. Quinton, J. Shapter, J. Nanopart. Res. **1**, 2013 (2009)
13. L. Goh, K. Razak, N. Ridhuan, K. Cheong, P. Ooi, K. Aw, Nanoscale Res. Lett. **7**, 1 (2012)
14. Y. Lin, J. Xie, H. Wang, Y. Li, C. Chavez, S. Lee, S.R. Foltyn, S.A. Crooker, A.K. Burrell, T.M. McCleskey, Q.X. Jia, Thin Solid Films **492**, 101 (2005)
15. R.K. Gupta, N. Shridhar, M. Katiyar, Mater. Sci. Semicond. Proc. **5**, 11 (2002)
16. C.V. Nguyen, K.R. Carter, C.J. Hawker, J.L. Hedrick, R.L. Jaffe, R.D. Miller, J.F. Remenar, H.W. Rhee, P.M. Rice, M.F. Toney, M. Trollsås, D.Y. Yoon, Chem. Mater. **11**, 3080–3085 (1999)
17. K.C. Aw, P.C. Ooi, K.A. Razak, W. Gao, J. Mater. Sci. Mater. El **24**, 3116 (2013)
18. J.M. Montero, J. Bisquert, G. Garcia-Belmonte, E.M. Barea, H.J. Bolink, Org. Electron. **10**, 305 (2009)
19. D.I. Son, D.H. Park, J.B. Kim, J.-W. Choi, T.W. Kim, B. Angadi, Y. Yi, W.K. Choi, J. Phys. Chem. C **115**, 2341 (2010)
20. C.-W. Tseng, Y.-T. Tao, J. Am. Chem. Soc. **131**, 12441 (2009)