

# Conductive filament formation in printed circuit boards: effects of reflow conditions and flame retardants

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**Abstract** Conductive filament formation, a major cause of failures in printed circuit boards, is an electrochemical process that involves the transport of a metal through or across a nonmetallic medium under the influence of an applied electric field. With an increasing potential to market “green” electronics, environmental and health legislations, and the advent of lead-free and halogen-free initiatives, newer types of printed circuit board materials are being exposed to ever higher temperatures during solder assembly. The higher temperatures can weaken the glass-fiber bonding, thus enhancing conductive filament formation. The effects of the inclusion of halogen-free flame retardants on conductive filament formation in printed circuit boards are not completely understood. Previous studies, along with analysis and examinations conducted on printed circuit boards with failure sites that were due to conductive filament formation, have shown that the conductive path is typically formed along the delaminated fiber glass and epoxy resin interfaces. This paper is a result of a year-long study on the effects of reflow temperatures, halogen-free flame retardants, glass reinforcement weave style, and conductor spacing on times to failure due to conductive filament formation.

## 1 Introduction

The spacing between plated-through-hole edges is estimated to approach 2 mil by 2014 [1]. With increases in design density and tighter spacing between conductors, the possibility of conductive filament formation (CFF) failure in printed circuit board (PCB) electronic assemblies has also increased. CFF is a failure observed within glass-reinforced epoxy PCB laminates that is caused by an electrochemical process involving the ionic transport of a metal through or across a non-metallic medium under the influence of an applied electric field [2]. The growth of the metallic filament is a function of temperature, humidity, voltage, laminate materials, manufacturing processes, and the geometry and spacing of the conductors [3]. The growth of these filaments can cause an abrupt loss of insulation resistance between the conductors under a DC voltage bias.

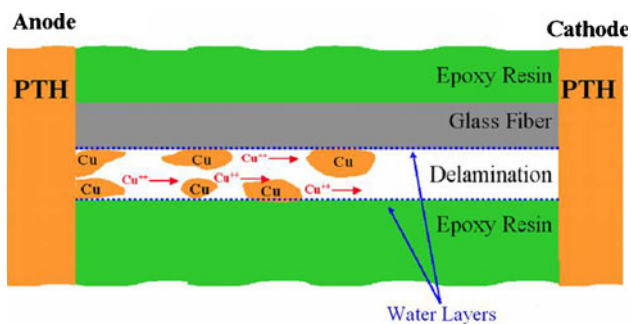
Failures in PCBs account for a significant percentage of field returns in electronic products and systems. Studies on CFF have found that path formation in a PCB is often along the glass fiber to epoxy matrix interface (Fig. 1). Delamination along the fiber/resin interface can occur as a result of stresses generated under thermal cycling due to coefficient of thermal expansion (CTE) mismatch between the glass fiber (CTE ~5.5 ppm/°C) and the epoxy resin (CTE ~65 ppm/°C) (Fig. 2). CFF can take place in the plated-through-hole to plated-through-hole (PTH-PTH), PTH-plane, and trace-trace geometries.

Tests to characterize CFF conducted by Lahti and Lando in 1979 showed that there is little or no degradation in insulation resistance up to the point of failure [2, 3]. That is, prior to failure, it is difficult to anticipate or predict failure by examining or monitoring insulation resistance. They also observed that one of the mechanisms responsible

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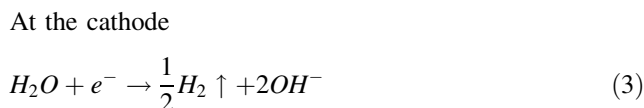
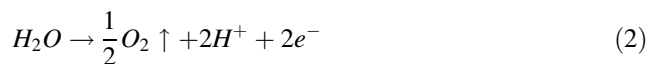
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**Fig. 1** Schematic describing CFF growth

for CFF failures involves the penetration of the glass/epoxy interface by a conductive copper compound generated by electrochemical activity at the biased conductors (at the anode). The researchers observed that failure times dropped drastically at spacings less than 5 mil.

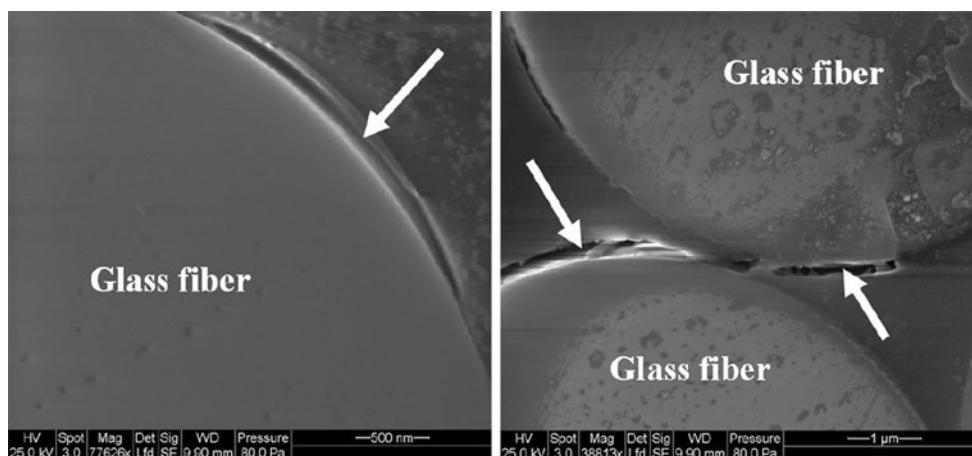
A two-step model was proposed to explain the growth of the conductive filaments occurring at the resin-glass interface in PCBs. Degradation of the resin-glass interfacial bond takes place in the first step, followed by the electrochemical reaction. According to Lando’s hypothesis, the path required for the transportation of metal ions formed by the degradation of the resin-glass interfacial bond may result from mechanical release of stresses, poor glass treatment, hydrolysis of the silane glass finish, or stresses resulting from moisture-induced swelling of the epoxy resin. The path formation was reported to be independent of bias; however, it was observed that humidity could be a contributing factor in the case of chemical degradation. After path formation, the PCB may be viewed as an electrochemical cell. In this cell, the copper conductors are the electrodes, the absorbed water is the electrolyte, and the driving potential for the electrochemistry is the operating or test potential of the circuit. The electrode reactions proposed for the metal migration were:



The electrolysis of water creates a pH gradient between the electrodes, since hydronium ions are produced at the anode while hydroxide ions are produced at the cathode. Using a simplified Pourbaix diagram for copper, a drop in pH at the anode allows copper corrosion products to be soluble until reaching a neutral region where they will be insoluble; thus, deposition along the epoxy-glass interface was explained.

The materials tested in this study [3] included standard FR-4 materials from six suppliers using barrier coatings of resin (1–4 mils thick) in addition to various glass treatments. G-10, polyimide, and triazine, all with woven glass, along with polyester (woven and chopped glass), and epoxy with woven Kevlar were tested. The parameters of the tests were a continuous DC bias ranging from 200 to 400 V, 80% RH, 85 °C, line–line, hole–hole, and hole-line conductor test patterns with and without surface coating. Lando [3] concluded that the susceptibility to CFF growth may depend on conductor configuration in decreasing order of susceptibility: hole–hole > hole-line > line–line. Mitigation strategies proposed by Lando included separating the resin/glass from the conductors by resin-rich areas, using triazine laminates, and improving the glass finish to allow stronger interfacial bonding at the glass fiber-epoxy resin interface.

Mitigation strategies proposed by researchers and laminate manufacturers include separating the resin/glass from



**Fig. 2** CFF growth along the fiber/resin interface

the conductors by resin-rich areas, using triazine laminates, and improving the glass finish to allow stronger interfacial bonding at the glass fiber-epoxy resin interface.

## 2 Conductive filament formation—literature review

The following section provides a brief review of past research in the area of CFF, including substantive findings and contributions to the understanding of CFF.

Researchers from Bell Laboratories in 1955 observed that silver in contact with insulating materials under an applied electrical bias can be ionically removed from its initial location at an anode and be re-deposited as metal at a different location at a cathode [4]. A major requirement for the process is the adsorption of water on the insulating surface to act as the electrolyte. Examination of the metal re-deposited at the cathode revealed a dendritic structure, while the deposits at the anode appeared brownish and colloidal. Since silver was the only metal at that time to cause a potential hazard, the process was called silver migration. Parameters that were identified as affecting the silver migration rate included the properties of the insulating material, the DC voltage, time of the voltage application, and the percent relative humidity. Phenol fabric—the insulating material between the metals—was found to be susceptible to silver migration. The rate of the migration was observed to increase with voltage and relative humidity. Mitigation techniques that were suggested included resin impregnation to more effectively isolate fibers, pretreatments of fibrous surfaces with water repellent agents, and the use of silver precipitating agents to capture free silver ions.

In 1979, Lahti et al. [2] conducted experiments on configurations of single-sided, double-sided, and multi-layered rigid PCBs with and without plated-through-holes (PTHs) with conductor spacings ranging from 5 to 50 mils, temperatures from 23 to 95 °C, relative humidities from 2 to 95%, and test voltages ranging from 10 to 600 V. The authors observed while monitoring CFF failures that there is little or no degradation in insulation resistance up to the point of failure. Hence, prior to failure, it is difficult to anticipate or predict failure by examining or monitoring insulation resistance. Also seen was that the mechanism responsible for CFF failures involves the penetration of the glass/epoxy interface by a conductive copper compound generated by electrochemical activity at the anodically biased conductors.

The first indication that the mechanism has initiated is the visual enhancement of the glass reinforcement around the anodes due to the physical separation at the glass/epoxy interface. Dark copper-bearing material then begins to fill the articulated regions, growing away from the anodes. The growth of the copper-bearing material follows the

reinforcement in many directions, but ultimately migrates preferentially towards the cathodically biased conductors. The researchers observed that at spacings less than 5 mils, failure times dropped drastically. Lot to lot variability in the CFF resistance of the epoxy-glass printed wiring boards was also noted; one lot may perform better at 400 V than another set at 45 V.

Among the variables observed to affect the susceptibility of a PCB to CFF, the most important appeared to be raw materials. Processing factors such as process chemistry and lamination parameters, in addition to assembly parameters such as fluxing, soldering, cleaning, and baking, were shown to influence the propensity of a PCB to CFF failure. From the tests, it was concluded that the CFF failure mechanism is voltage sensitive, but not highly so; the dependence was not found to be greater than the inverse of voltage. In this study, failures occurred first on the most deeply buried layers and later in the layers closer to the board surface.

Lando et al. [3] in 1979 proposed a two-step model to explain the growth of conductive filaments occurring at the resin-glass interface in PCBs. The first step is the degradation of the resin-glass interfacial bond followed by a second step, the electrochemical reaction. According to Lando's hypothesis, the path required for the transportation of metal ions formed by the degradation of the resin-glass interfacial bond may result from mechanical release of stresses, poor glass treatment, hydrolysis of the silane glass finish, or stresses resulting from moisture-induced swelling of the epoxy resin. The path formation was reported to be bias independent but possibly humidity sensitive in the case of chemical degradation. After path formation, the PCB may be viewed as an electrochemical cell. In this cell, the copper conductors are the electrodes, the absorbed water is the electrolyte, and the driving potential for the electrochemistry is the operating or test potential of the circuit.

In 1980, Welsher and other researchers at Bell Laboratories [5] conducted extensive tests on triazine-glass, a CFF resistant material. The test boards were fabricated with a hole-hole grid test pattern with 42 mil diameter PTHs on 75 mil centers, with a minimum conductor spacing of 35 mils. Welsher proposed a two-step model consistent with that proposed by Lando [3]. The tests showed that the exposure of a PCB to thermal transients such as thermal shock or during multiple soldering steps could significantly reduce its CFF resistance. The application of an intense thermal transient accelerates debonding of the fiber-epoxy matrix interface due to the coefficient of thermal expansion (CTE) mismatch between the fiber and epoxy. A delayed application of the DC bias test showed that delaying the application of the DC bias does not significantly affect the time to CFF failure of the boards.

This confirmed the two-step sequential process proposed for CFF formation rather than the parallel process. It was also shown that the mean time to failure due to CFF might not be sensitive to the continuous or intermittent nature of the applied DC bias. Accelerated tests comparing the resistance of FR-4 and triazine to CFF failures demonstrated that boards manufactured with triazine can exhibit a life at least 20–30 times that of the FR-4s tested.

Mitchel and Welsher [6] observed that failures due to filament formation showed an Arrhenius temperature dependence over the temperature range of 50–100 °C. Analysis of the delayed bias tests in [6] showed that CFF growth takes place in two sequential steps, where mean time to failure is equal to the time for step 1 (path formation) plus the time for step 2 (electrochemical reaction), and that the time required for path formation is much greater than that required for the electrochemical reaction.

It was also observed that during the first stage of the failure process, an applied voltage is not necessary. In another pair of experiments, the reversibility of the two sequential steps was studied. In the first experiment, two sets of FR-4 samples were exposed to 85 °C/80% RH; the first set for 240 h, the second set for 168 h. The second set was dried at 85 °C for 72 h. Both sets were then tested at 85 °C/80% RH/200V. All samples in the first set failed within 4 h, while the mean time to failure of the second set of samples was 122 h.

From this study, it was concluded that step 1, the interfacial degradation, is essentially reversible, in agreement with studies on hydrolysis of glass-polymer coupling agents. To test the reversibility of the second step, electrochemical migration, several samples after failing at 70 °C/85% RH/200V were dried at 70 °C for 330 h and then retested again at 70 °C/85% RH/200V. The MTF before the drying was 292 h while the MTF after the drying was 54 h. It was thus concluded that once a filament has formed, it is permanent. In addition, several PCB materials were studied to determine their susceptibility to CFF growth. From this study, woven glass laminates with resins of triazine, bismaleimide triazine, and polyimide were observed to offer the best hole-hole CFF resistance.

Augis et al. [7] in 1989 indicated that there is a threshold in relative humidity below which CFF would not occur. It was important to identify this threshold since linear acceleration factor models used for extrapolating reliability had broken down (i.e., a material that performed poorly under highly accelerated conditions could have acceptable characteristics under normal operating conditions). Tests showed that newly manufactured boards compared to aged boards showed no difference in CFF resistance during accelerated tests. Step stress tests run over a long period of time showed that above certain humidity levels the percentage of CFF failures increased rapidly. Hence, it was

concluded that in humidity-controlled environments, CFF failures might not be a threat. Elemental analysis of the conductive filaments in the study always showed elemental copper and sometimes either chlorine or sulfur associated with the filament. The chlorine and sulfur were believed to be from the fabrication processes.

It was speculated that the filament grows from the anode to the cathode, and the degradation mechanism most likely involves these four steps:

1. Diffusion of water into the epoxy
2. Migration of ions ( $\text{Cu}^{++}$ ,  $\text{Cl}^-$ )
3. Corrosion ( $\text{Cu} \rightarrow \text{Cu}^{++}$ )
4. Chemical reactions, such as breaking of the silane bonds at the fiber/epoxy interface (may be due to hydrolysis)

A wide variability in median time to failure under the same environments using different lots of material was also observed.

Rudra et al. [8] in 1994 conducted experiments at CALCE using three PCB materials (FR-4, bismaleimide triazine (BT) and cyanate ester (CE)), two humidity levels (70 and 85% RH), two temperatures (70 and 85 °C), and two DC voltages (300 and 800 V). Each test board had six layers, ten different spacings, and six conductor geometries. The conductor geometries were PTH-to-plane, line-to-line, line-to-PTH, corner-to-PTH, PTH-to-PTH, and non-plated through-hole-to-line. The conductor spacings varied from 5 to 65 mils. Six different surface coatings were also tested.

From this study, it was concluded that BT and CE PCB materials are more resistant to CFF than FR-4 boards. BT and CE also had lower moisture absorption percentages. The presence of a post coat (a type of conformal coating) increased the time-to-failure due to CFF, while a solder mask in addition to the post coat offered the highest resistance to filament formation. For the various conductor geometries tested, PTH-to-PTH was the most susceptible failure site, followed by line-to-PTH and then line-to-line. It was observed that geometries on the surface layer tend to fail faster than the geometries on the inner layers. An empirical model based on the failure data from the FR-4 laminates was developed to assess the time to failure due to conductive filament formation. In this model temperature and humidity were combined into a threshold moisture content based on Augis' findings.

Ready et al. [9] in 1996 postulated that elevated bromide levels detected by EDX analysis in the area of a CFF failure may not have come from the board itself, but rather from a processing step. The presence of HBr in the soldering flux used during the problematic period suggests that this may be the source of the bromide. In this case, the bromide is speculated to have diffused through several

layers of a 14-layered board during the soldering process at temperatures above 200 °C. It was observed that substrates processed with fluxes containing certain polyglycols seem to exhibit an affinity for CFF formation. It appears that these polyglycols can also increase the moisture absorption of the laminate.

Turbini et al. [10] in 2000 examined the effect of certain water-soluble flux vehicles, both with and without halide activators, at processing temperatures of 201 and 240 °C in enhancing CFF formation. These two temperatures were selected to reflect both the expected peak temperature in wave soldering for traditional eutectic solder and for a typical lead-free solder. Using standard IPC-B-24 test coupons, it was observed that at the higher processing temperature, the occurrences of CFF failures greatly increased. It was speculated that this increase in CFF failures at the higher temperature was due to the enhanced diffusion of polyglycols into the boards during the wave soldering. Since the diffusion process follows an Arrhenius behavior, the length of time during reflow that the board is above its glass transition temperature will have an effect on the amount of polyglycol absorbed into the epoxy. Higher reflow temperatures also lead to greater thermal strains due to the CTE mismatches between the glass fibers and the epoxy resin.

In 2002, Sauter [11] from Sun Microsystems described the testing parameters and design features that CFF test boards should incorporate to effectively assess CFF vulnerability in today's electronics. Some CFF test boards/coupons have been designed with only twenty PTHs and a few layers, which is not representative of today's higher layer count boards with thinner dielectrics. Sun Microsystems developed a ten-layer board with 168 potential in-line PTH–PTH failures per spacing/test daisy chain and 312 potential diagonal PTH–PTH failures per spacing/test daisy chain. The data analysis techniques require 25 or more boards to be run per sample lot per bias level, giving 4,200 potential in-line hole–hole failure sites and 7,800 potential diagonal hole–hole failure sites per sample lot. This design has been made available to IPC (Institute for Interconnecting and Packaging Electronic Circuits) for industry use. Telcordia uses a 1,000-hour test while Sun uses a 500-hour duration period.

Sauter also recommends that a temperature of 65 °C be used instead of 85 °C to reduce the risk of sublimation, which can artificially reduce the activity of flux residues or other residues that may remain when certain board finishes are used, resulting in an erroneous assessment of CFF reliability risk. Sauter has found that some laminates that offer significantly more CFF resistance at larger spacings could perform poorly at smaller spacings. It was shown that although the Bell Labs and CALCE CFF prediction models appear to be quite different, the Bell Labs model and the

adjusted CALCE model both predict a similar  $8\times$  increase in CFF failure risk for the same decrease in conductor spacing. The modification to the CALCE model was made to include the readily conductive region around the PTHs. From test failure data, Sauter concluded that some high  $T_g$  (glass transition temperature) FR-4 laminate materials for some PCB manufacturers show less resistance to CFF than standard  $T_g$  FR-4 materials. Since the combination of the PCB board finish and glass weave direction has a significant impact on CFF testing results, the most vulnerable combination, HASL-finished boards tested in the machine direction, is recommended for evaluating the CFF susceptibility of a PCB.

In 2004, research scientists at the National Physical Laboratory [11] conducted two phases of accelerated tests to characterize conductive anodic filamentation. The first phase was aimed at understanding the effects of PTH geometries, voltage levels, and thermal effects, such as thermal shock and lead-free reflow, on a typical FR-4 laminate. Phase 2 incorporated improvements of the test board design based on lessons learned from phase 1. Phase 2 also compared different laminate types, glass reinforcements, drill feed speeds, and other laminate manufacturing variables.

In phase 1, standard  $T_g$  non-CAF resistant FR-4 boards with an electroless nickel immersion gold finish and no solder mask were tested. Each board had ten layers and more than 6,000 PTHs. The test voltages used ranged from 5 to 500 V, while the conductor spacings ranged from 300 to 800  $\mu\text{m}$  (in-line and staggered PTHs), and from 100 to 200  $\mu\text{m}$  (anti-pad annulus). The parameters of the thermal shock were  $-15$  to  $+120$  °C and a cycle time of 14 min with a 5-minute dwell in each bath. Selected samples were exposed to 250 thermal shock cycles. The peak temperature used for the lead-free reflow was 250 °C, and the boards were exposed three times. The testing was conducted at 85 °C/85% RH for a duration of 1000 h.

The findings from phase 1 were as follows: lead-free reflow increased CFF susceptibility while thermal shock had a negligible effect; MTF for in-line PTHs < staggered PTHs  $\approx$  anti-pad; CFF occurs faster at higher voltages; CFF occurs faster at smaller spacings; and MTF is not strongly dependent on anti-pad gap spacing. NPL also determined that the relatively fast initial filament growth slows as it moves further away from the anode.

Phase 2 compared the CFF resistance of two manufacturers, both with CFF resistance and non-CAF resistance, and high and low  $T_g$  laminates. The effect of different drill feed speeds and surface finishes (electroless nickel immersion gold, silver, hot air solder level, and organic solderability preservative) on the time to failure for CFF were also examined. Two reflow peak temperatures were used: 210 and 250 °C.

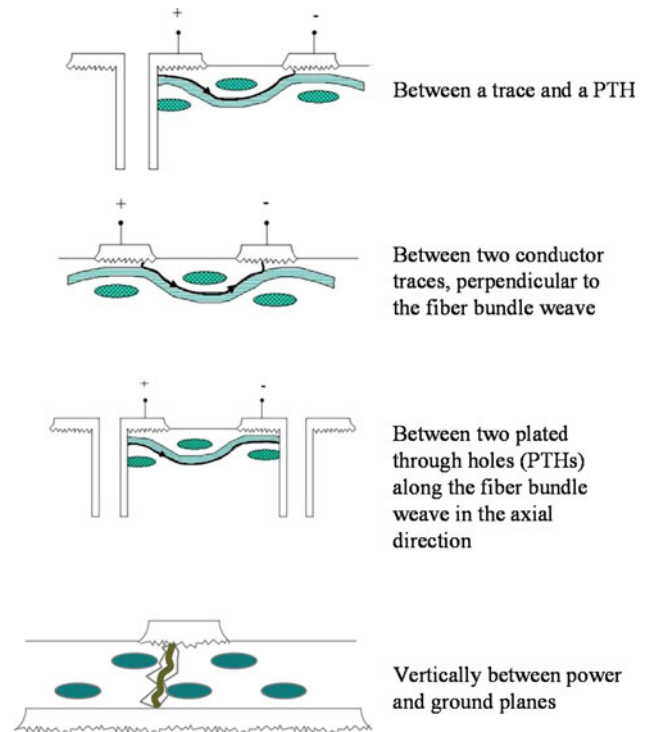
The test results from phase 2 indicated that a higher reflow temperature promotes faster CFF growth. This, in conjunction with the negligible thermal shock effect, implies that perhaps the mechanism for damage in the laminate is not based on CTE mismatches between the materials, but rather a chemical or physical breakdown above a certain critical temperature. It was observed that in the anti-pads, failure occurs faster if the PTH is positively biased and the plane is negatively biased, and slower if the PTH is negatively biased and the plane is positively biased. It was also observed that PTHs closer together fail faster, even for the same electric field. In all laminates tested, the CFF resistant laminates offered extended life of different percentages compared to their non-CAF resistant counterparts. The CFF resistant laminates delayed the time to failure due to CFF, but did not prevent it. CFF failures occur faster along the fabric weave in the machine direction. Identical laminates from different board manufacturers can have significantly different resistances to CFF. The tendency for failure to occur in a specific fabric glass style within the laminate weave-stack-up can vary from manufacturer to manufacturer. The parameters that had the most significant impact on CFF resistance were firstly the manufacturer (manufacturing process) and secondly the materials. The parameters that had negligible effects on the time to failure due to CFF were surface finishes, high or low  $T_g$  designation, and drill feed speed.

Rogers et al. [12, 13] showed that laminates containing hollow fibers posed a threat to the reliability of electronic systems in that they provided a convenient open path for CFF. A method to detect hollow fibers in PCB laminates is discussed in detail. Based on CALCE’s recommendations, hollow fiber assessment has now become a standard screen by which hollow fiber content ratios may be determined. This screen allows board fabricators and contract assemblers to qualify suppliers and discard lots with hollow fiber concentrations above specifications.

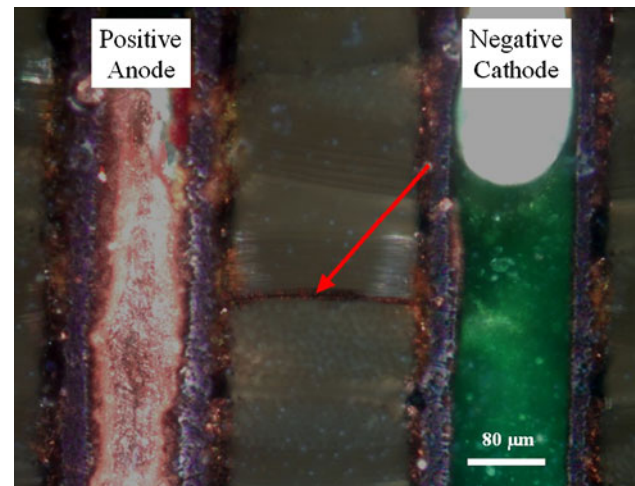
### 3 Path formation in CFF

A pathway connecting oppositely biased conductors must be formed for CFF to occur. The common pathways are shown in Fig. 3. Other path configurations include formation between PTHs and power/ground planes, between internal traces, between an internal trace and a PTH, and between internal and surface traces. Fig. 4 shows an actual CFF failure between two adjacent PTHs.

It is hypothesized that path formation, proposed to be voltage independent, is the rate-limiting step in CFF. In other words, it takes a significantly longer time for the pathway to be formed than for the metal migration and



**Fig. 3** Common CFF pathway configurations are shown. Hollow fibers can also contribute to CFF by allowing an open pathway



**Fig. 4** This optical *darkfield* photo shows a conductive filament close to but under the polished cross-sectional resin plane, connecting and electrically shorting two adjacent PTHs

formation of the conductive filament bridging and the shorting of the two conductors.

### 4 Path caused by mechanical degradation

Mechanical degradation or physical delamination can occur at the interfaces of the glass fibers and epoxy resin

matrix (see Fig. 5). Mechanical stress can arise due to the coefficient of thermal expansion (CTE) mismatches in the properties of the epoxy resin and the glass fibers. CTE values for cured un-reinforced epoxy resin can range from 50 to 65 ppm/°C (depending on the amount of diluents), while that of the glass fibers in the radial direction is approximately 5 ppm/°C [14]. Studies by Li et al. [15] show that this mismatch can lead to interfacial stresses and de-bonding at the fiber-resin interface during thermal cycling. Manufacturing defects can accelerate and help to initiate the formation of this pathway.

The difference in the moisture absorption of glass fibers and epoxy resin can also lead to interfacial stresses. During thermal-humidity cycling, the swelling and shrinking of the epoxy has been shown to induce physical de-bonding at the fiber glass/epoxy resin interface, in addition to micro-cracking in the resin [15]. The absorption of moisture can also reduce the  $T_g$  of the laminate, allowing excess thermal stress to cause more damage [16, 17]. Path formation, where there is a physical, mechanical separation at the fiber glass/epoxy resin interface or micro-cracking due to thermal cycling and thermal-humidity cycling, may not be reversible.

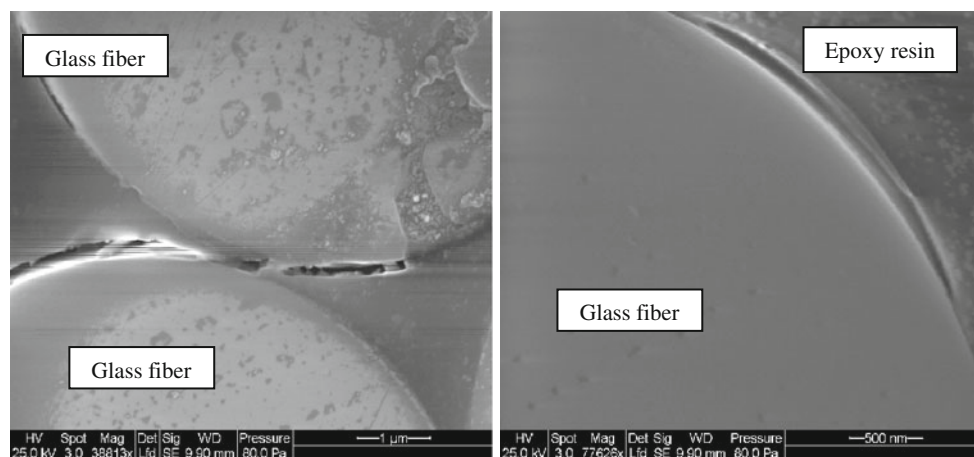
### 5 Path caused by chemical degradation

A pathway between conductors may also be formed by chemical hydrolysis of the silane glass finish or coupling agent. Studies indicate that the glass epoxy interface absorbs 5–7 times more moisture than the bulk epoxy [18]. The most common cross-linking agent used in FR-4 and many other epoxy-based laminated systems is dic-yandiamide (dicy). Dicy is hydrophilic and, to some extent, so is the glass surface. This combination of a

hydrophilic surface and a hydrophilic cross-linking agent appears to be one of the factors responsible for the mechanism whereby chemical degradation of the glass fiber/epoxy resin interface due to hydrolysis occurs. William et al. [17] have shown that PCBs manufactured with non-dicy cross-linked epoxy resins exhibit much more resistance to CFF failures compared to PCBs manufactured with dicy cross-linked epoxy resins. Research by Mitchell et al. [6] demonstrated that this type of chemical degradation may be reversible.

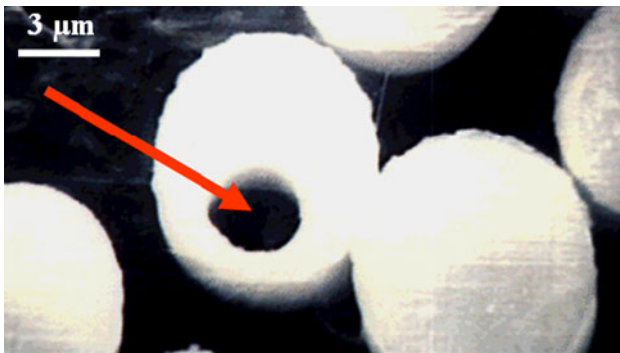
### 6 Path caused by hollow fibers

During the manufacture of glass fibers, a homogeneous melt composition with negligible impurities is necessary to prevent the decomposition of raw materials. The sublimation of these organics can lead to trapped gases. Depending on the viscosity of the glass mixture and various manufacturing processes, these gases can get trapped as bubbles, called seeds. Seeds are a naturally occurring part of the process and thus methods to remove them are necessary. If the molten glass contains a sufficient level of impurities, air bubbles may become trapped inside the fibers while being drawn through the bushing. These air bubbles, unless very large, do not cause fiber breakage but end up as capillaries in the glass fibers, otherwise known as hollow fibers (see Fig. 6). These hollow glass fibers increase the opportunity for failure between close conductors because the capillary provides a convenient path for the formation of conductive filaments [19–22]. Hollow fibers pose a serious reliability threat because with hollow fibers the rate limiting step,  $T_1$ , is eliminated from the two-step sequential process.  $T_1$  consists of path formation, followed by  $T_2$ , which is the electrochemical reaction, where  $T_1 \gg T_2$  [6].

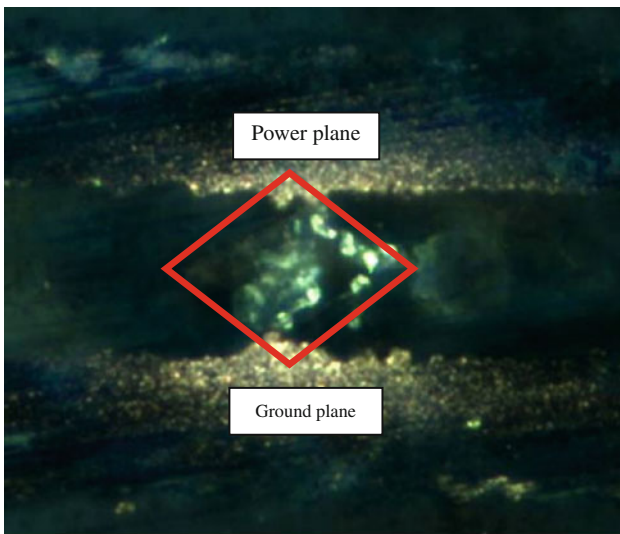


**Fig. 5** These E-SEM photos show physical delamination at the interfaces of the glass fibers and epoxy resin matrix. De-bonding can occur due to mechanical stresses arising due to the coefficient of

thermal expansion (CTE) mismatches in the properties of the epoxy resin and the glass fibers during thermal cycling



**Fig. 6** Image of a hollow fiber (*red arrow*)



**Fig. 7** Optical *photo* of conductive filament formed in the *vertical direction* between cracked Cabosil filler particles

**7 Path caused by cracks in resin filler particles**

In a set of PCBs failing by shorted internal planes, the root cause was determined to be conductive filament formation in the vertical direction via cracked Cabosil (fused silica)

particles. This determination required actual physical identification of a hydrolyzed Cabosil particle at a failure site (see Figs. 7 and 8). Unfortunately, this was made difficult by the large area covered by the power and ground planes, which made identification of the failure site using functional or parametric testing impossible.

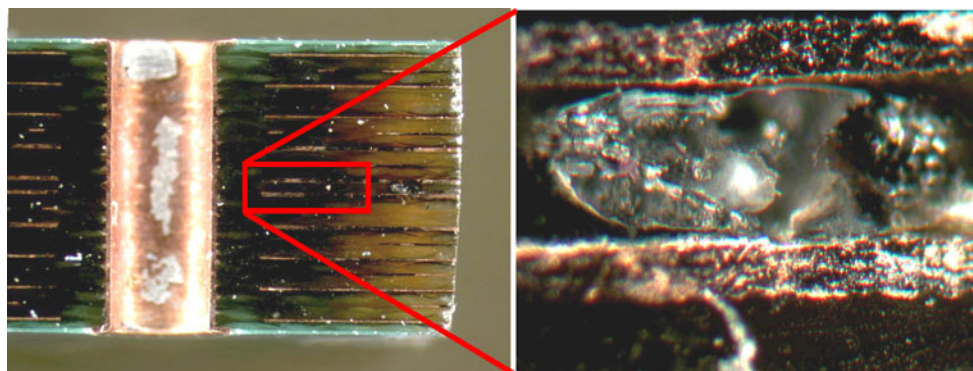
Due to the particles being larger than the vertical spacing between the power and ground planes, during lamination of the boards, larger particles are trapped in the vertical gap between the power and ground planes and cracking. In humid environments during testing and operation, these internal cracks in the Cabosil allow moisture to ingress into the existing path, leading to conductive filament growths.

**8 Influence of path formation on CFF time-to-failure**

Prior to formation of the filament, consistent with the published literature, a pathway connecting the oppositely biased conductors must be formed. It is hypothesized that path formation, which is proposed to be voltage independent, is the rate-limiting step in conductive filament formation. In other words, it takes a much longer time for the pathway to be formed than for the metal migration and formation of the conductive filament bridging and shorting the two conductors.

Hence, to deter failures due to the growth of conductive filaments, it is necessary to control the rate limiting step (path formation) by characterizing the different path formation modes and mechanisms. Attempts to mitigate CFF failures include:

- Offering of CFF resistant laminates by PC fabricators (Matsushita)
- Use of low moisture absorption (non-hydrophilic) materials
- Reduce the CTE mismatch between the epoxy resin and the glass fibers



**Fig. 8** Optical *photos* show a charred burnt area between the power and ground plane in a printed wiring board due to vertical filament formation



- Use of moisture barriers to retard moisture ingress
- Enhance the adhesion between the glass and resin
- Use of non-woven fibers
- Use of staggered (non-inline) PTHs
- PTHs drilled at 45° to the weave of the glass fabric.

## 9 Halogen-free and lead-free

Flame-retardant (FR) chemicals are added to PCBs during or after manufacture to inhibit or suppress combustion. FRs interfere with combustion at various stages of the process, such as during heating, decomposition, ignition, or flame spread. One goal is to prevent the spread of fires or delay the time of flashover.

There are various kinds of FRs, such as halogenated, chlorinated, phosphorous-based, nitrogen-based, and inorganic. Different types of FRs are better suited for different applications. Their suitability depends on compatibility with the material to be flame-retarded, the fire safety standards with which the product must comply, reliability, and cost considerations. Halogens are the chemical elements fluorine, chlorine, bromine, iodine, and astatine. For plastic PCBs, brominated flame-retardants (BFRs) are the most effective flame retardant when both performance and cost are considered. BFRs have a unique chemical interaction with the combustion process because bromine is more effective than most of the alternatives, meaning that a much lower quantity of flame retardant achieves the highest fire resistance.

There are different types of BFRs [23], such as PBBs (polybrominated biphenyls), PBDEs (polybrominated diphenyl ethers), TBBPA (tetrabromobisphenol-A), and HBCD (hexabromocyclododecane). Each of these BFRs has very different properties.

Humans and the environment can be exposed to PBBs released during recycling of materials or after disposal in landfills. BFRs, and especially PBBs and PBDEs, are considered hazardous due to the formation of polybrominated dibenzodioxins and furans (PBDD/F) during combustion of both the BFRs themselves and flame-retarded materials such as PCBs. Analyses of the principal halogen-containing component of printed circuit boards, TBBPA, have not shown that TBBPA is a source of human dioxin exposure [24]. According to an IPC white paper, the major driver for halogen-free flame substitutes for TBBPA in printed circuit boards is marketing, and there are no significant health concerns.

The main applications of lead in electrical and electronic equipment (EEE) include the solder joints of components mounted onto PCBs and board finishes [25, 26]. Typically, reflow and wave soldering involve exposing the components

and circuit boards to processing conditions sufficiently hot to melt the soldering alloys, which then form acceptable solder joints. The drive towards lead-free electronics has resulted in the use of lead-free solders in PCB assemblies. Common lead-free solder alloys such as Sn/Ag/Cu and Sn/Ag typically require a peak reflow temperature increase of approximately 40 °C compared to traditional eutectic Sn/Pb reflow soldering conditions [25]. The temperature and process time required to flow the lead-free solders have posed a significant issue in tin-lead replacement. The melting point of tin-lead solder is 183 °C, which typically corresponds to maximum reflow temperatures in the region of 220–230 °C. The primary lead-free alloys have melting points in the 217–220 °C range with corresponding processing temperatures of approximately 240–260 °C. Such an increase in processing temperature raises concerns for boards and components initially designed for tin-lead processing, but which now must withstand a 34 °C heating differential.

A particular concern is the reaction of components and PCBs that may crack or delaminate due to trapped moisture or board warpage. Significant deformation of moisture-laden packages versus dry packages starts to increase at around 90 °C. Increased rates of deformation occur beyond 138 °C [27, 28].

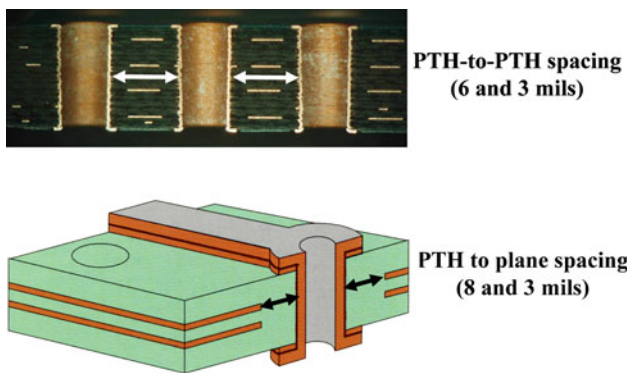
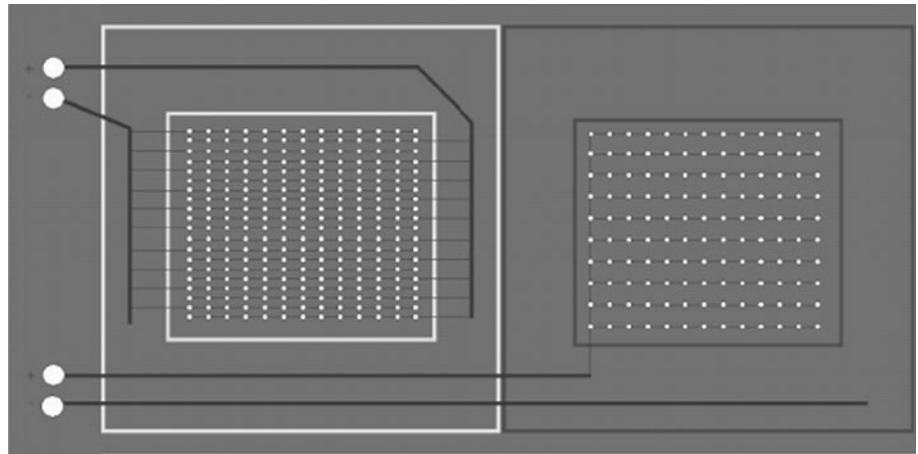
## 10 Experimental section

### 10.1 Test set-up

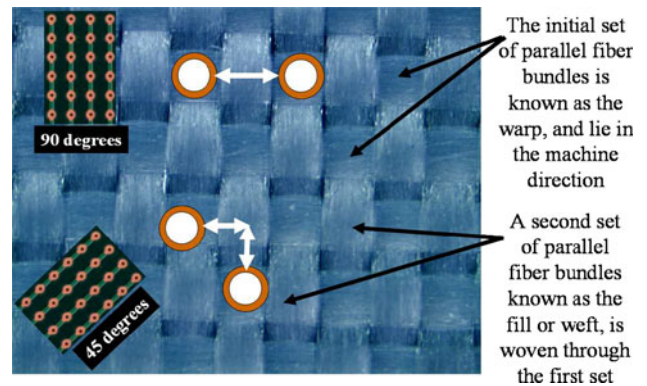
In order to characterize the CFF failure behavior in laminated PCBs, accelerated tests were conducted under high temperature and high humidity environments. Four laminate types, three conductor spacings, and voltages ranging from 1 to 100VDC were included in the design of experiments. The tests were conducted by researchers at the Center for Advanced Life Cycle Engineering (CALCE) at the University of Maryland. The test boards were manufactured by Gold Circuit Electronics in Taiwan.

The test board designs and parameters for the test coupons were selected based on IPC-TM-650 2.6.25 (2003), Telcordia GR-78 (GR-78-CORE, 13.1.4, Electro-migration Resistance Test) and Sun Microsystems [11] CFF Test Board Specifications. The design of the test boards, as shown in Fig. 9, contained 600 in-line PTH-PTH and 100 PTH-plane conductors, with PTH-PTH spacings and PTH-internal plane spacings based on current technology and manufacturing limitations using mechanical drilling (Fig. 10). The three feature sizes in both PTH-PTH and PTH-plane conductor geometries were selected to be representative of nominal, advanced, and next generation (XG) feature sizes in electronics. The nomenclature of the three designs and conductor feature sizes were:

**Fig. 9** Test board design



**Fig. 10** Conductor spacing



**Fig. 11** Fabric weave orientations

1. Nominal feature (NF): PTH-to-PTH: 6 mil; PTH-plane: 8 mil
2. Advanced feature (AF): PTH-to-PTH: 4 mil; PTH-plane: 6 mil
3. XG: PTH-to-PTH: 3 mil; PTH-plane: 3 mil

The allowed drill wander for all features was  $\pm 1$  mil.

Four different laminate types from two laminate suppliers were used for the fabrication of the 71-mil thick, 8-layer board (six internal planes). Since CFF susceptibility can be affected by fabric weave direction, features were placed on the board in such a way that the failure site opportunity with respect to weave orientation was either parallel to machine direction (warp direction) or at  $45^\circ$  to machine direction. Fig. 11 shows the placement of the features with respect to the fabric weaves.

The four laminate types from the two suppliers, along with the glass transition temperatures ( $T_g$ ) were:

- 1 Supplier A,  $T_g$  180 °C
- 2 Supplier A,  $T_g$  170 °C
- 3 Supplier B,  $T_g$  170 °C
- 4 Supplier B (Halogen-free),  $T_g$  150 °C

Five samples were tested for each spacing design and laminate type for a total of 20 samples per test.

Cross-sectional measurements of the internal conductor spacings and optical inspection revealed that the conductor spacing were within the specified tolerances. Copper wicking was found to be less than 1 mil (5, 4, and 3 mil are acceptable per IPC A-600F for class 1, 2, and 3 electronic assemblies, respectively). No plating voids or plating cracks were observed in the cross-sections. The average solder mask thickness was 0.5 and 0.2 mil measured over a masked trace and the edge of a masked trace, respectively. The maximum measured misregistration was less than 0.5 mil. Ion chromatography analysis of the boards revealed that the ionic contamination was less than 1 mg of NaCl per square inch (IPC recommends no more than 10 mg of total ionics per square inch).

The boards were tested in accordance with IPC-TM-650 2.6.25, Conductive Anodic Filament (CAF) Resistance Test: X–Y Axis [29]. Each board was uniquely identified. The test boards were handled by the edges only using non-contaminating gloves. Each of the two circuits in each test

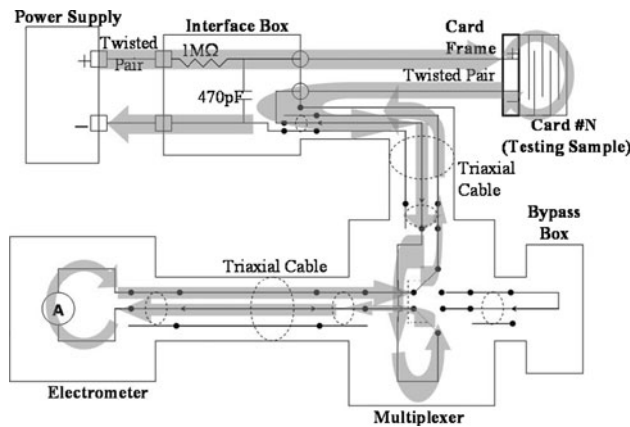


Fig. 12 Schematic of setup used for measuring insulation resistance

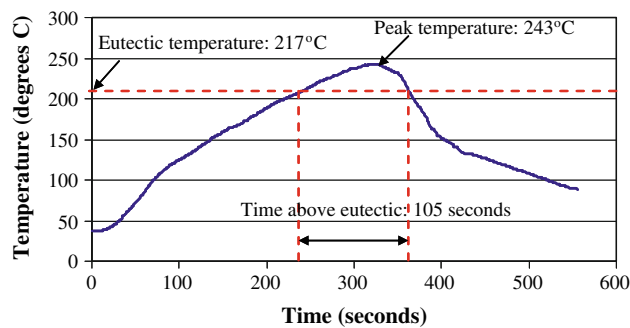


Fig. 13 A typical lead-free reflow profile

board was prescreened for short circuits by performing an as-received insulation resistance measurement check.

The boards were baked for 6 h at 105 °C prior to each test to dry out the samples. After baking, the samples were preconditioned for 24 h at 23 °C and 50% RH. The insulation resistances were again measured prior to a 96-h stabilization period with no applied bias at 85 °C/85% RH. After this stabilization period, a bias was applied and insulation resistance measurements were started. An Agilent 4349B high resistance meter was used to monitor the insulation resistance of the 20 boards as they were subjected to humidity/temperature/bias testing. The insulation resistance monitoring setup is shown in Fig. 12. A 1 MΩ

current limiting resistor was placed in series with the current path to prevent “blow-out” of the fragile filaments when shorting occurred. Prior to the biased test, insulation resistance readings for each of the circuits were measured to be greater than 500 MΩ. Every channel used for resistance monitoring was scanned once every 48 s. This monitoring regime was more stringent than the IPC requirements of 24–100 h.

One set of 20 boards were subjected to reflow conditions prior to the test exposures. In test 4, from each of the four groups of five samples each, two samples (a total of 8) were exposed to 3× eutectic reflow and three samples (a total of 12) to 3× lead-free reflow. A typical lead-free reflow profile is shown in Fig. 13. All samples were exposed to 3× reflow cycles. The samples were subsequently exposed to 85 °C and 85% RH conditions at 10V DC bias conditions as outlined in the test matrix. A summary of the test conditions is shown in Table 1.

### 11 Results and discussion

For the largest spacing (PTH-to-PTH 6 mil and PTH-plane 8 mil), a typical plot of the insulation resistance changes for three samples (two Supplier B 170 °C  $T_g$  and one Supplier B halogen-free 150 °C  $T_g$ ) monitored over the 500-h duration of the test for the PTH–PTH conductor geometry is shown in Fig. 14.

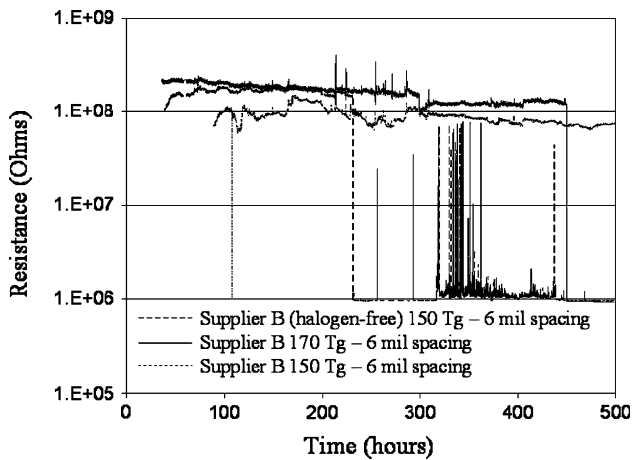
Figure 14 shows the intermittent nature of the CFF failures. Here, the insulation resistance value instantaneously drops to  $1 \times 10^6 \Omega$ , which is the value of the in-series protection resistor, and then recovers back to normal. At the 10 V bias level in test 1, there were seventeen failures in the PTH–PTH geometries and no failures in the PTH-plane geometries. After the duration of the 500-h test, some of the samples had not failed.

When the AF spacing (PTH-to-PTH 3 mil, PTH-plane 3 mil) was subjected to the same environmental test conditions after the application of the voltage bias (10 V) and after the required presoak (96 h at 85 °C/85% RH per IPC-TM-650 2.6.25, CFF Resistance Test: X–Y Axis Specifications), all PTH–PTH insulation resistances immediately

Table 1 Test conditions

Test	Number of boards	Spacing (mil)		Pre-exposure	Test environment (°C, %RH)	Voltage bias (VDC)
		PTH–PTH	PTH–Plane			
1	20	6	8	None	85, 85	10
2	20	3	3	None	85, 85	2
3	20	3	3	None	65, 85	2
4	8	6	8	Eutectic reflow *	85, 85	10
	12	6	8	Lead-free reflow *	85, 85	
5	20	6	8	None	85, 85	10

\* From each of the four groups of five samples each, two samples were exposed to eutectic reflow and three to lead-free reflow



**Fig. 14** Plot showing PTH–PTH insulation resistance monitored at 10V for three of the supplier B samples

dropped to 1 MΩ, which was the resistance of the in-series protection resistor. This suggests that there were locations where the insulation resistance significantly decreased (by two orders of magnitude) in these samples prior to the biased exposure. All of the samples failed prior to 40 h, some within 1 min. There were also four PTH-plane failures in test 2. Similar behavior was observed for test 3 where the spacing was the same (PTH-to-PTH: 3 mil; PTH-plane: 3 mil), but the exposure conditions were 65 °C/85% RH at 2 V bias. All the PTH–PTH geometries failed during the 500-h test. No failures were observed in the PTH-plane geometries.

There were failures in the test samples exposed to eutectic and lead-free reflow conditions. For PTH–PTH geometries with 6 mil spacing exposed to eutectic reflow conditions, five out of the eight boards failed. On the other hand, for PTH–PTH geometries (6 mil spacing) exposed to lead-free reflow conditions, nine of the twelve boards failed. Slightly higher failures were seen in the test samples exposed to 3× lead-free conditions as compared to samples

exposed to 3× eutectic reflow conditions. There were no failures observed in the PTH-plane geometries with 8 mil spacings exposed to eutectic reflow conditions, but the test samples that were exposed to lead-free reflow conditions had three failures out of the eight samples.

In the 6 mil spacing PTH–PTH test samples exposed to 85 °C and 85% RH, where features were placed at a 45° angle to the machine direction, there was only one failure. There were no failures in the 8 mil spacing PTH-plane geometries. A compilation of the experimental results is shown in Table 2.

The result of reflow exposure to CFF formation also varied with the laminate material type. The effect of reflow was seen clearly in the case of Supplier B  $T_g$  170 °C and Supplier B halogen-free materials where all of the samples exposed to any kind of reflow (both eutectic and lead-free) failed during testing. Test samples that were constructed out of the same two laminate materials but were not exposed to any soldering showed a fewer number of failures after testing. All the test samples constructed with Supplier B halogen-free material and tested after no reflow, eutectic reflow, or lead-free conditions failed. Test samples constructed with the halogen-free flame retarding material were the only cases where all samples had failed during testing. The test samples from Supplier A that were exposed to lead-free or eutectic reflow conditions showed a lower number of failures compared to samples that were not exposed to any reflow conditions. A summary of the effect of reflow on various laminate materials is provided in Table 3.

After the insulation resistance dropped to 1 MΩ (the resistance of the in-series protection resistor), selected samples were removed from the test chamber and analyzed with a scanning quantum interference device (SQUID). SQUID-based microscopy is able to image buried current-carrying wires by sensing and measuring magnetic fields produced by the currents. By mapping the current, short circuits can be localized and failure sites determined.

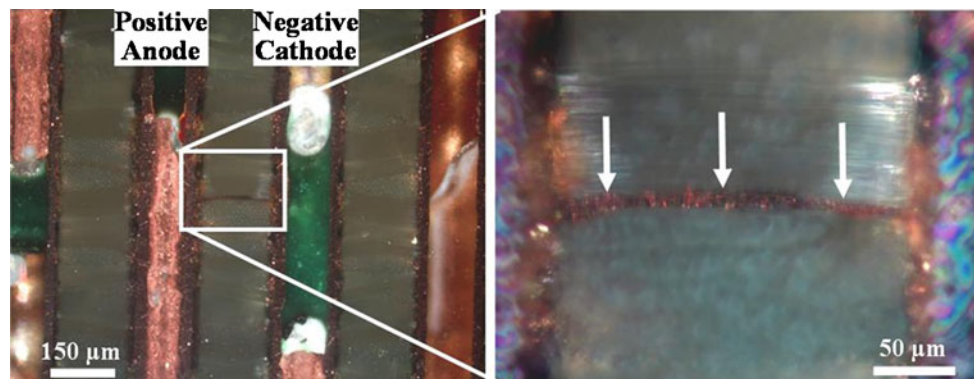
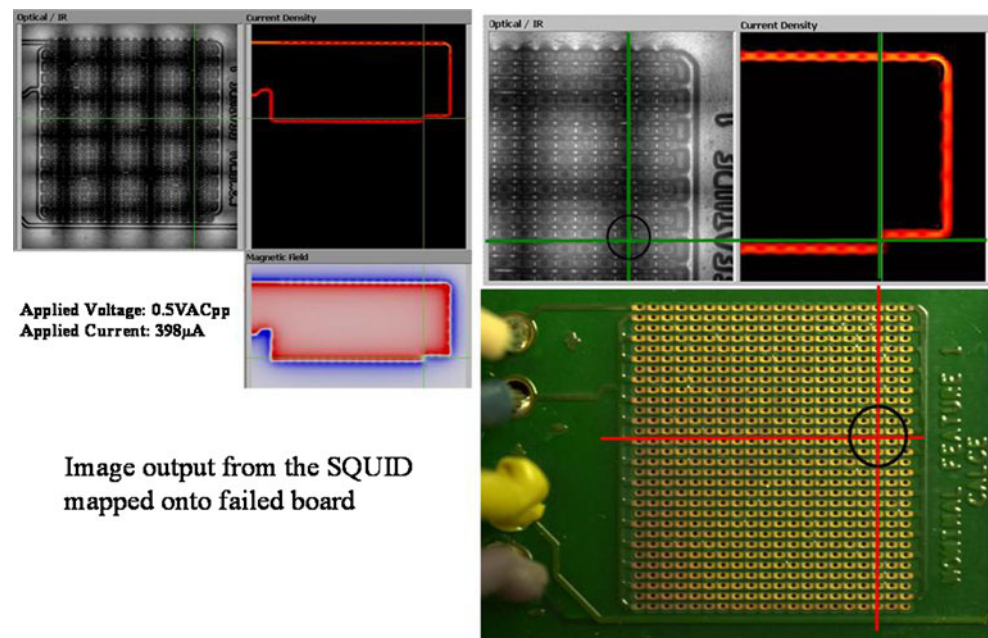
**Table 2** Experimental results

Test	Weave	Spacing (mil)		Pre-exposure	Voltage Bias (VDC)	Test environment (°C, %RH)	Number of boards showing failures/ total boards	
		PTH–PTH	PTH-Plane				PTH–PTH	PTH-Plane
1	90°	6	8	None	10	85, 85	17/20	0/20
2	90°	3	3	None	2	85, 85	20/20	4/20
3	90°	3	3	None	2	65, 85	20/20	0/20
4	90°	6	8	Eutectic reflow	10	85, 85	5/8	0/8
		6	8				Lead-free reflow	9/12
5	45°	6	8	None	10	85, 85	1/20	0/20

**Table 3** Effect of reflow on CFF failures in PTH–PTH geometries for various laminate types

Laminates	Number of boards showing failures		
	No reflow	Eutectic reflow	Lead-free reflow
Supplier A, $T_g$ 180 °C	5/5	0/2	2/3
Supplier A, $T_g$ 170 °C	5/5	1/2	1/3
Supplier B, $T_g$ 170 °C	3/5	2/2	3/3
Supplier B (Halogen Free), $T_g$ 150 °C	4/5	2/2	3/3

**Fig. 15** Overlaying the shorted site as predicted by the SQUID current mapping images, the respective conductor locations on the test boards were identified for cross-sectioning



**Fig. 16** Filament formation in the PTH–PTH geometry

Figure 15 shows the SQUID output for the selected failed samples, locating the shorted sites in the board in a PTH–PTH conductor geometry.

Cross-sectioning in the failed areas that were identified by the SQUID revealed conductive filaments in PTH–PTH conductor geometry when optically examined. Figure 16 shows optical images of a filament formed between two PTHs.

## 12 Conclusions

The drive to increase circuit density with smaller printed circuit board geometries, higher layer counts, and the increasing use of electronics in environmentally uncontrolled applications, have made short circuiting due to conductive filaments between biased conductors a major concern. In addition, higher temperatures in lead-free

processing and new flame retardant materials affect laminate stability and increase the potential for conductive filament formation failures. This study has shown that smaller conductor spacing reduces the time to failure due to conductive filament formation and that the plated-through-hole to plated-through-hole (PTH–PTH) conductor geometry is more susceptible to conductive filament-induced failures than PTH-plane geometries. The results also show that laminates with similar materials and geometries with a 45-degree angle of weave demonstrate a higher resistance to conductive filament formation compared with a 90-degree angle of weave.

To mitigate catastrophic failures, it is necessary to understand the roles and synergistic effects of environmental conditions, material properties, and manufacturing quality in accelerating the pathways necessary for the initiation of conductive filament formation. Some proactive companies have already begun to invest in this area and are funding research to deter conductive filament formation-related failures.

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