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Effects of post-deposition annealing temperature and ambient on RF magnetron sputtered Sm_2O_3 gate on n-type silicon substrate

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Abstract Samarium oxide (Sm_2O_3) thin films with thicknesses in the range of 15–30 nm are deposited on n-type silicon (100) substrate via radio frequency magnetron sputtering. Effects of post-deposition annealing ambient [argon and forming gas (FG) (90% N_2 + 10% H_2)] and temperatures (500, 600, 700, and 800 °C) on the structural and electrical properties of deposited films are investigated and reported. X-ray diffraction revealed that all of the annealed samples possessed polycrystalline structure with C-type cubic phase. Atomic force microscope results indicated root-mean-square surface roughness of the oxide film being annealed in argon ambient are lower than that of FG annealed samples, but they are comparable at the annealing temperature of 700 °C (Argon—0.378 nm, FG—0.395 nm). High frequency capacitance–voltage measurements are carried out to determine effective oxide charge, dielectric constant and semiconductor-oxide interface trap density of the annealed oxide films. Sm_2O_3 thin films annealed in FG have smaller amount of effective oxide charge and semiconductor-oxide interface trap density than those oxide films annealed in argon. Current–voltage measurements are conducted to obtain barrier heights of the annealed oxide films during Fowler–Nordheim tunneling.

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1 Introduction

Due to the aggressive downscaling in silicon (Si)-based technology of metal–oxide–semiconductor (MOS) transistors, alternative high dielectric constant (κ) materials have excessively been investigated to replace the conventional SiO_2-based gate dielectric films. In sub-100 nm Si-based MOS devices, thickness of SiO_2 should be made thinner than 1.5 nm [1–3]. Shrinkage of the physical thickness of SiO_2 films below 1.5 nm resulted in direct tunneling of charges through the dielectric films and led to large leakage current [3]. Many candidates such as Ta_2O_5 [4–6], TiO_2 [7–9], ZrO_2 [3, 10, 11], HfO_2 [9, 10, 12, 13], La_2O_3 [14–16] and CeO_2 [17–19] have been introduced as alternative dielectric material to substitute SiO_2. Recently, rare earth oxides (REOs) [14–42] have emerged as promising candidates for next generation dielectrics. Of these REOs, La_2O_3 was reported as one of the most promising candidate that has been investigated to replace SiO_2. La_2O_3 has the highest dielectric constant in the group of REOs [27]. However, it demonstrates the most hydroscopic property in the group [41], which may degrade electrical properties of the dielectric film. Thus, researchers have started to search for alternative REOs with similar dielectric features but less hydroscopic as a replacement. Sm_2O_3 is an attractive REO material to achieve the comparable dielectric properties as La_2O_3. κ values of the Sm_2O_3 thin film reported are in the range of 9–14 [21, 29, 32, 36, 40, 42], depending on the physical film thickness and deposition methods. Besides, Sm_2O_3 thin film has a wide band gap [31, 43], large conduction band offsets [33] and, thermodynamically stable on the underlying Si surface [34–36, 39, 40].

Previously, Sm_2O_3 films had been grown by different physical vapor deposition (PVD) [24, 25, 29–31, 34–36, 39, 40, 42] and chemical vapor deposition (CVD) [21, 26,

32] methods on Si. The reported chemical vapor deposited dielectric films were contained large amount of carbon due to incomplete decomposition of metal–organic precursor at low processing temperature and produced excess of carbon in the dielectric film [21]. As a result, PVD methods have an advantage compared to the CVD methods in producing a higher purity of the dielectric film. Recently, the oxide films are mostly deposited by radio frequency (RF) magnetron sputtering [34, 36, 39, 40, 42]. It is found that leakage current densities of the dielectric films deposited by this method with smaller κ values [36] are lower than the films produced by electron beam evaporation [25].

From literatures [17, 34, 36, 39, 42, 44], electrical properties of REOs dielectric films could be improved by employing post-deposition annealing (PDA). Temperature, ambient, and duration play an important role in PDA [17, 34, 36, 42, 44, 45]. It is reported that for RF-magnetron sputtered Sm_2O_3 films, PDA in N_2 ambient showed better improvement of root-mean square (RMS) surface roughness [36] than in O_2 ambient [39]. The PDA temperatures used are ranged from 600 to 800 °C [36, 39, 40, 42] as this is the range of phase transformation temperature of Sm_2O_3 from cubic C to monoclinic B [46]. Cubic C is the most stable phase of Sm_2O_3 at room temperature and it is preferably to produce the thin film in this phase [36, 40, 42, 46]. The PDA temperatures in this range was being selected in order to avoid the transformation of Sm_2O_3 into undesired monoclinic B phase at elevated temperature (>800 °C), and at the same time remains the optimum PDA performance of the Sm_2O_3 thin films [40, 42]. However, PDA of RF magnetron sputtered Sm_2O_3 films in argon (Ar) (inert gas) and forming gas (FG) (reducing gas) ambient within this range of temperatures have not been reported. Generally, FG annealing is employed to passivate Si dangling bonds at oxide–semiconductor interface by supplying electrons to reduce the Si cations [47]. These electrons also have been used to neutralize positive effective oxide charge existing in the film and thus, improving the negative flatband voltage shift (ΔV_{FB}) [47, 48]. In this study, physical and electrical characteristics of the Sm_2O_3 thin films deposited on n-type Si (100) substrate by means of RF-magnetron sputtering, followed by PDA process in Ar or FG (90% N_2 + 10% H_2) atmospheres at varies temperatures were investigated. The PDA temperatures are ranged from 500 to 800 with 100 °C interval. This interval is selected due to successful investigations from recent literatures for post deposition annealed Sm_2O_3 thin films in N_2 ambient [36, 39, 40, 42].

2 Experimental procedure

Sm_2O_3 thin films were deposited on an n-type 3-in Si (100) substrate by RF magnetron sputtering. The substrate thickness used was in the range of 525 ± 25 μm with a resistivity of approximately 30 Ω-cm. Before the sputtering, Si substrate was cleaned by a standard Radio Corporation of America (RCA) cleaning method. 99.9% pure Sm_2O_3 sputtering target with a diameter of 3 in and a thickness of 0.125 in (manufactured by ACI, USA) was used as a sputtering target to deposit the Sm_2O_3 thin film on Si. During the sputtering process, Ar flow rate of 19.05 $cm^3\ min^{-1}$ was used. The sputtering power was 150 W and the total pressure was 1.3×10^{-2} Torr. The sputtered samples were annealed in a horizontal tube at four different temperatures of 500, 600, 700, and 800 °C. They were held separately at each temperature for 30 min in Ar and FG (90% N_2 + 10% H_2) ambient. The heating rate was 10 °C min^{-1}. After PDA, the samples were slowly cooled to room temperature in the tube with a cooling rate of approximately 5 °C/min. Thicknesses of the deposited films were in the range of 15–30 nm, measured by an ellipsometer (L 116S) that used a laser light source of 632.8 nm. Surface topography and RMS surface roughness of the annealed thin films were analyzed by a non-contact mode atomic force microscope (AFM) (Nano Navi SPI3800N). X-ray diffraction (XRD) (P8 Advan–Bruker) equipped with Cu-Kα radiation with the wavelength of 1.5406 Å operated under a voltage of 40 kV and a current of 40 mA was used to examine the phases and orientations of the oxide films on Si. The scan range was carried out from $2\theta = 20°–80°$ with a step size and step time of 0.034208° and 71.599998s, respectively. In order to evaluate electrical characteristics of the investigated samples, MOS-capacitor test structure was fabricated. A layer of aluminium (Al) with thickness of 100 nm was coated on top of the oxide by a thermal evaporator (EMI TECH K950X). Then, an array of Al gate electrode with an area of $2.5 \times 10^{-3}\ cm^2$ was patterned by photolithography process. Lastly, a layer of Al electrode was coated at the back of the substrate to form MOS capacitor structures. High frequency (1 MHz) capacitance–voltage (C–V) characteristics of the MOS capacitors were measured by a LCR meter (Agilent 4284) with an applied dc voltage of 24 mV and current–voltage (I–V) measurements were conducted by a semiconductor parameter analyzer (Agilent 4156C).

3 Results and discussion

3.1 Structural properties

Figure 1 shows the XRD pattern of as deposited Sm_2O_3 thin film on Si substrate with the scanning range of $2\theta = 20°–80°$. The strong peak detected at $2\theta = 69.18°$ is consistent with the International Conference for Diffraction Data (ICDD) file no. 01-089-2749, which is corresponded

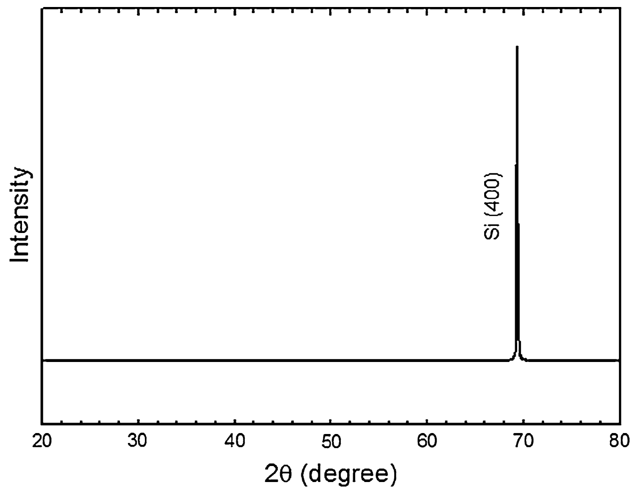

Fig. 1 XRD pattern ($2\theta = 20°–80°$) of as-deposited Sm_2O_3 thin film on Si

to cubic Si with (400) plane and is paralleled to the Si (100) plane. Intensity of the Si (400) peak is extremely higher than the oxide diffraction peaks. In order to analyze the plane orientation of annealed oxide films, Fig. 1 has been zoomed into the range of 2θ in where the oxide peaks existed ($2\theta = 20°–60°$).

Figure 2 shows the refined XRD patterns of Sm_2O_3 thin films annealed at various temperatures (500, 600, 700, and 800 °C) in Ar and FG atmospheres. All of the investigated samples are polycrystalline in nature. Four diffraction peaks are detected at $2\theta = 32.8°$, 47.9°, 54.5°, and 56.2°, which corresponded to Sm_2O_3 (400), (433), (541), and (622) planes, respectively. These diffraction peaks are well matched with the ICDD files no. 00-042-1461, which is denoted as C-type cubic phase of Sm_2O_3. The (400) peak has a stronger intensity than the other minor peaks and it is detected as a preferred oriented plane for all investigated samples. This suggests a preferential growth of the crystallites with the (400) plane of cubic Sm_2O_3 parallel to the Si (100) substrate. Previously, Pan et al. [36, 40] also had reported the same diffraction peaks in their investigation of RF-magnetron sputtered Sm_2O_3 on p-type Si (100) substrate annealed at 600, 700, and 800 °C. In our work, all of the diffraction peaks of samples being annealed in Ar ambient are growing stronger as the annealing temperatures is increased from 500 to 700 °C and dropped slightly at the annealing temperature of 800 °C. Increase of the intensities of diffraction peaks is attributed to the crystallization of Sm_2O_3 at elevated temperatures [49]. For FG annealed samples, no significant changes in the intensities of the diffraction peaks are observed as increased the annealing temperatures. This suggests FG annealing suppressed the crystallization of Sm_2O_3 thin films at high annealing temperatures.

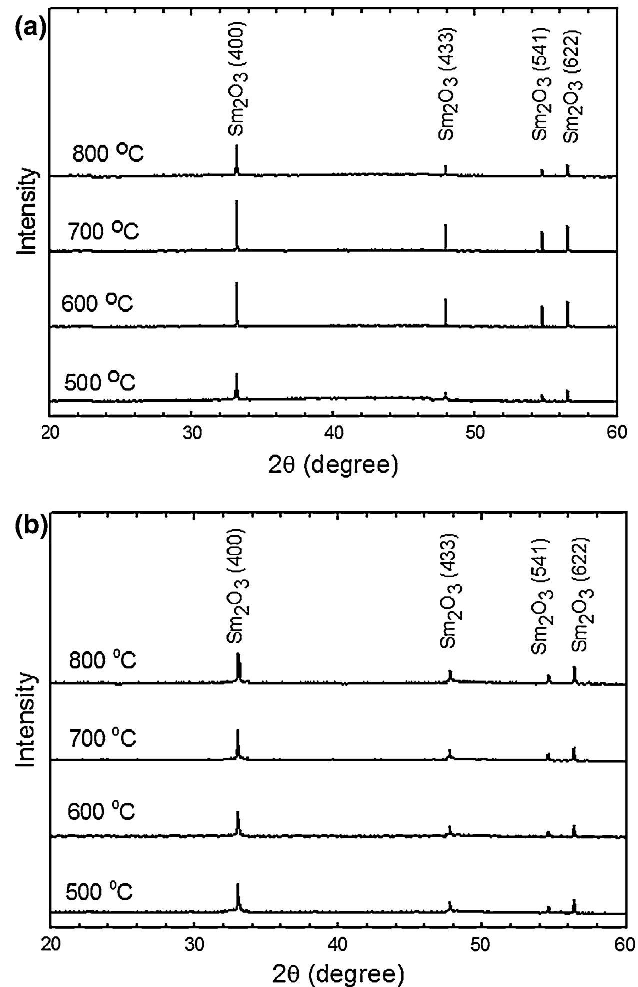

Fig. 2 XRD patterns ($2\theta = 20°–60°$) of Sm_2O_3 dielectric films prepared at various annealing temperatures (500, 600, 700, and 800 °C) in **a** Ar and **b** FG ambient

Three-dimensional surface topographies of Ar and FG annealed Sm_2O_3 dielectric films were characterized by AFM with scanning area of 1 µm × 1 µm (Figs. 3, 4). Triangular-like protrusions are observed on the surface of all annealed oxide films. For Ar annealed oxide films, coarser protrusions are observed at annealing temperature of 500 °C and they are aligned in random orientations. As the annealing temperature is increased from 500 to 800 °C, they are getting finer in shape and their alignments have improved significantly. However, blunter shapes of protrusions are revealed in the FG annealed samples. They are randomly oriented throughout all of the annealing temperatures. The finest protrusions are observed for the samples annealed at 700 °C.

Typical two-dimensional sketch of the protrusion is illustrated in Fig. 5. The average peak-valley (P–V) length and average horizontal width were determined from 20 protrusions for each specific annealing ambient and temperatures. Relationships of these two parameters as a

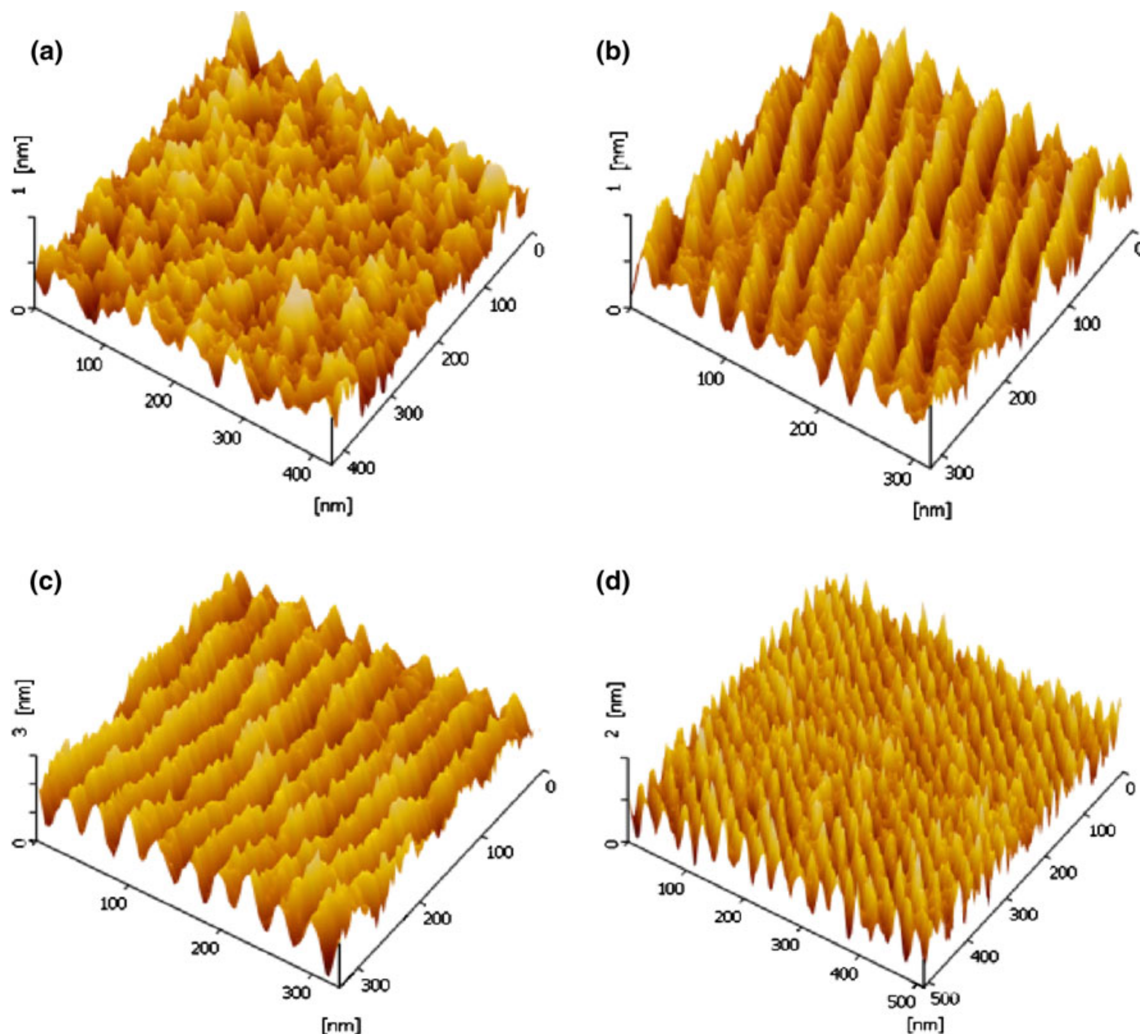

Fig. 3 Typical three dimensional images of surface morphologies of the Sm_2O_3 dielectric films annealed in Ar atmosphere at **a** 500, **b** 600, **c** 700, and **d** 800 °C

function of annealing temperatures for two different annealing ambient are plotted in error bars to show the maximum, mean and minimum values as shown in Fig. 6. Ar annealed samples behaved differently when compared with the FG annealed samples throughout the investigated annealing temperature range. As the annealing temperature increases from 500 °C to 600 °C, the protrusions grown in both horizontal and vertical directions for Ar annealed samples. These two parameters are reduced when further annealed the samples to 700 and 800 °C. As differ from Ar annealing atmosphere, reduction of the average P–V length and average horizontal width for FG annealed samples are observed from the annealing temperatures of 500 to 700 °C and increased slightly at 800 °C.

Figure 7 compares the RMS surface roughness of Sm_2O_3 films at various annealing temperatures in Ar and FG atmospheres. Five different points were taken in a particular sample from each PDA temperature to test for surface roughness and presented in error bars. Maximum, mean and minimum RMS roughness of each tested sample is shown in the error bars. The overall RMS roughness of Ar annealed thin films is smaller than the FG annealed thin films, but they showed a comparable value at the annealing temperature of 700 °C (Ar—0.378 nm, FG—0.395 nm). Both, the Ar and FG annealed samples, demonstrated different trends throughout the annealing temperatures, but they are in an agreement with the trend of average P–V length and average horizontal width measurements as presented in the earlier section. RMS surface roughness of the Ar annealed samples is increased as increasing the annealing temperatures to 600 °C, and it started to reduce when annealed at 700 and 800 °C. The increment of RMS surface roughness upon PDA is due to crystallization or grain growth mechanism of the oxide films during annealing [50]. For FG annealed samples, RMS surface roughness decreased as the annealing temperature is

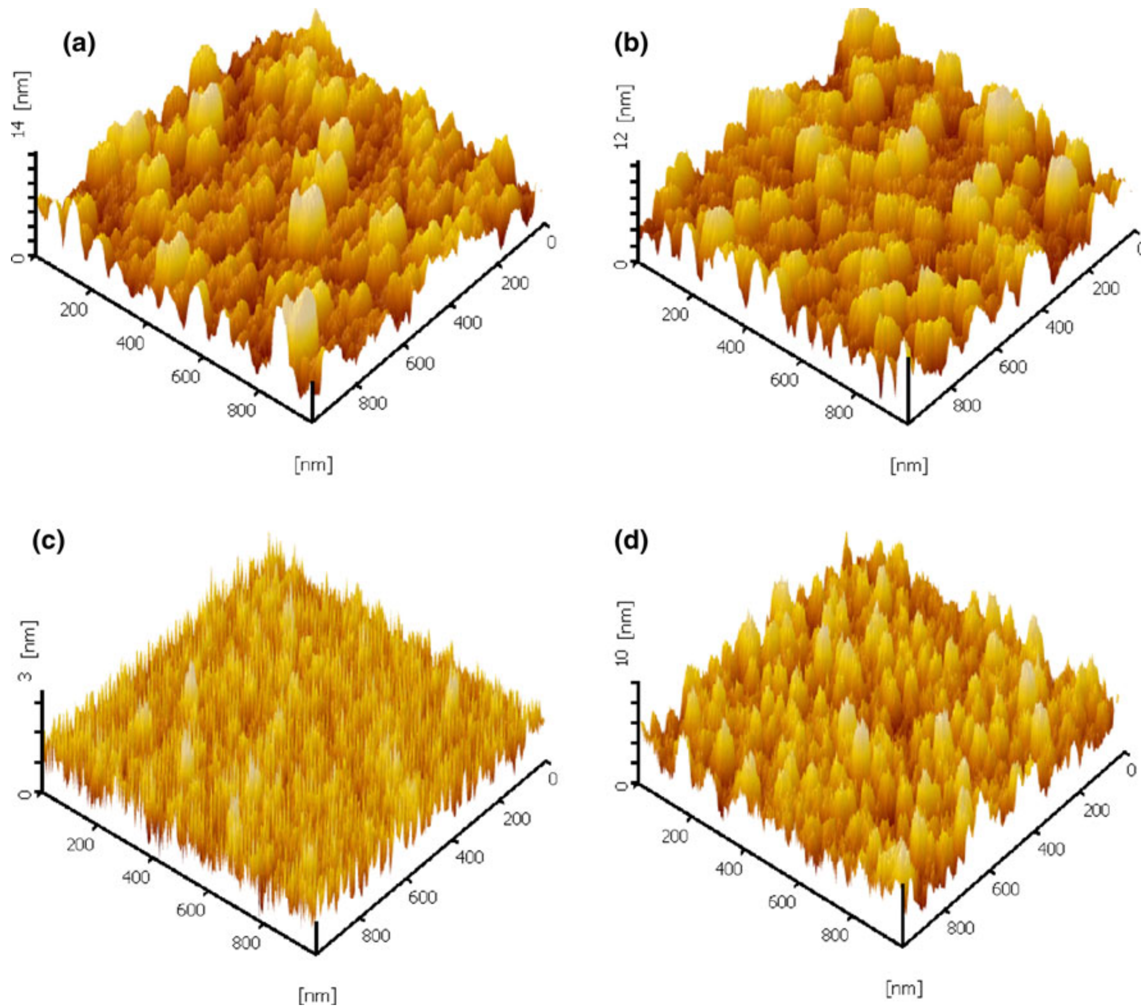

Fig. 4 Typical three-dimensional images of surface topographies of the Sm_2O_3 dielectric films annealed in FG atmosphere at **a** 500, **b** 600, **c** 700, and **d** 800 °C

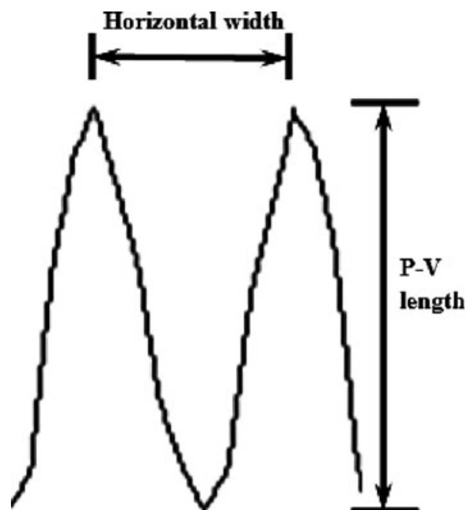

Fig. 5 Two-dimensional sketch of the protrusion present on the surface of Sm_2O_3 dielectric film

increased to 700 °C and roughened after annealed at 800 °C. Reduction of RMS surface roughness is attributed to the densification of the dielectric films upon PDA [49]. The trend of RMS surface roughness variation as a function of annealing temperature for FG annealed samples is consistent to the investigation reported by Pan et al. [36].

3.2 Electrical properties

Three samples from each specific PDA temperatures were tested electrically under LCR meter for C–V measurement. Figure 8 shows the typical average normalized capacitance (C/C_o) versus gate voltage curves of three $Al/Sm_2O_3/Si$ MOS capacitors annealed at each specific temperatures in Ar and FG atmospheres, where C_o is the capacitance at $V_g = 0$ V. The gate bias was applied in a forward direction and swept from −4 to 2 V. No constant saturation at the accumulation is observed for 500 °C annealed sample in

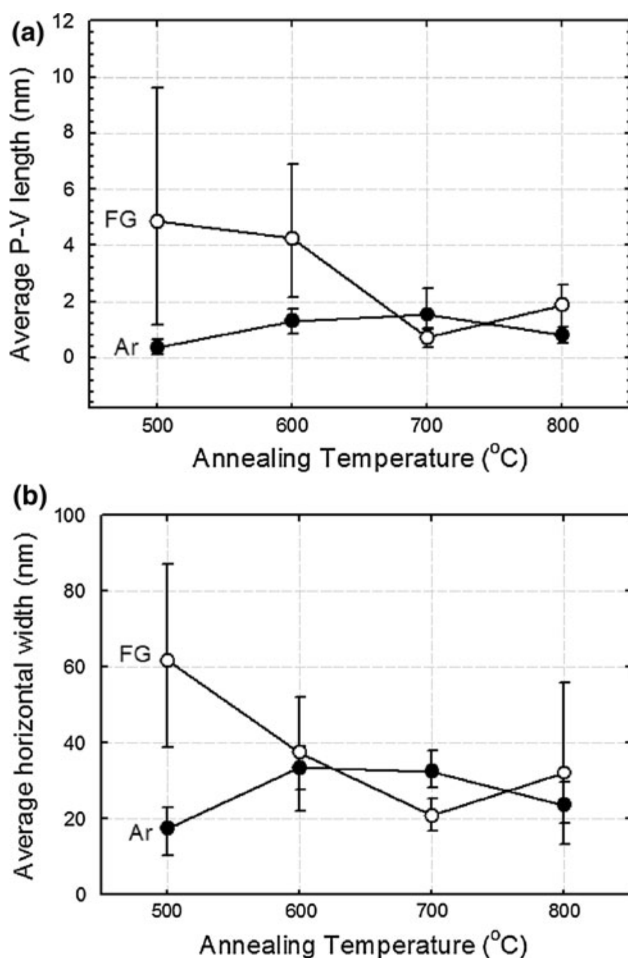

Fig. 6 The relationships of **a** average P–V length, and **b** horizontal width as a function of annealing temperatures for the Ar and FG annealed samples in error bars to show the maximum, mean and minimum values

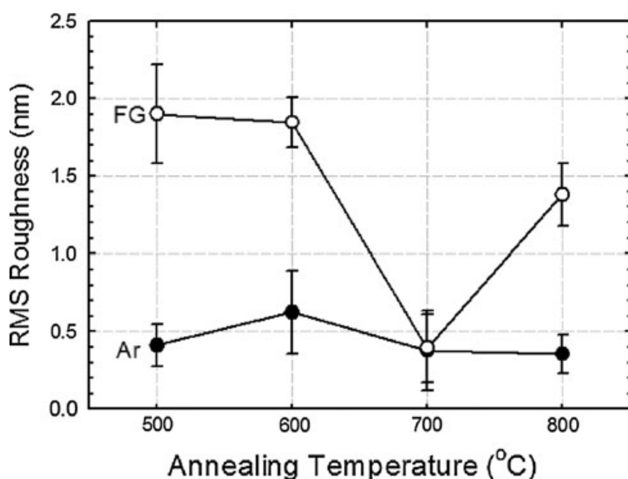

Fig. 7 *Error bars* showing the average RMS surface roughness of three Sm_2O_3 dielectric films from each specific annealing temperature in Ar and FG atmosphere

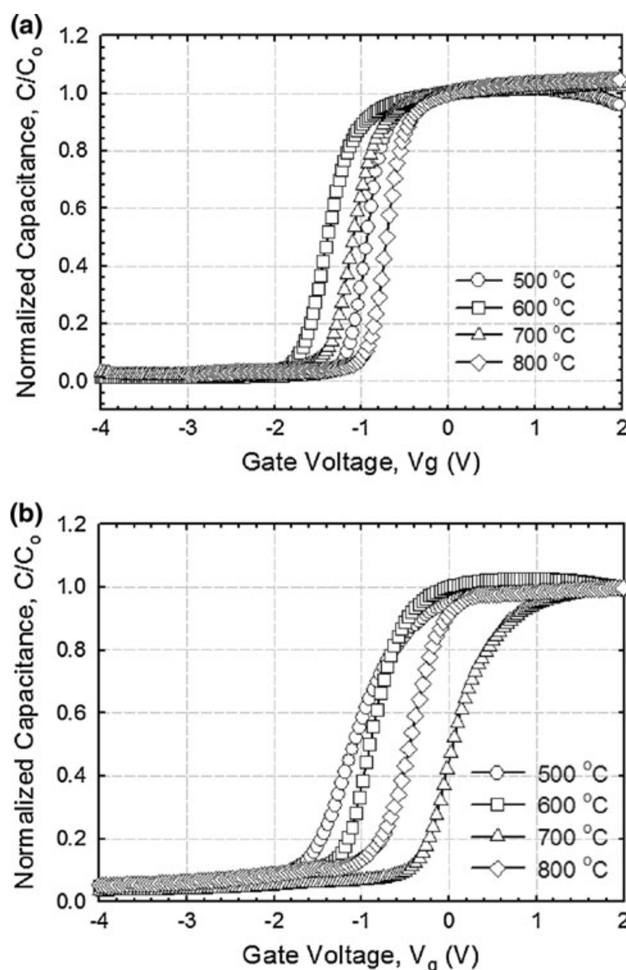

Fig. 8 Plot of normalized average capacitance (C/C_o) versus gate voltage bias for the Sm_2O_3 dielectric films annealed at various temperatures in **a** Ar, and **b** FG atmospheres

Ar ambient. This is due to the relatively high amount of trap charges in oxide film [17]. From high-frequency C–V curve, accumulation capacitances are extracted and they are used to determine κ values of oxide films based on the following equation [17]:

$$\kappa = (C_{ox}t_{ox})/(\varepsilon_0 A_{ox}) \quad (1)$$

where C_{ox} is oxide capacitance obtained from C–V curve, t_{ox} is gate oxide thickness, ε_0 is permittivity of free space, and A_{ox} is gate area.

Figure 9 displays the average κ values (maximum, mean and minimum) of Sm_2O_3 dielectric films annealed at different temperatures in Ar and FG ambient. The average κ values obtained for samples annealed in Ar ambient (6.6–9.5) and FG ambient (5.4–7.2) are comparable to the results reported by Pan et al. [36]. It is observed that κ values of Ar annealed samples are decreased upon increasing the annealing temperatures, whereas the FG annealed samples

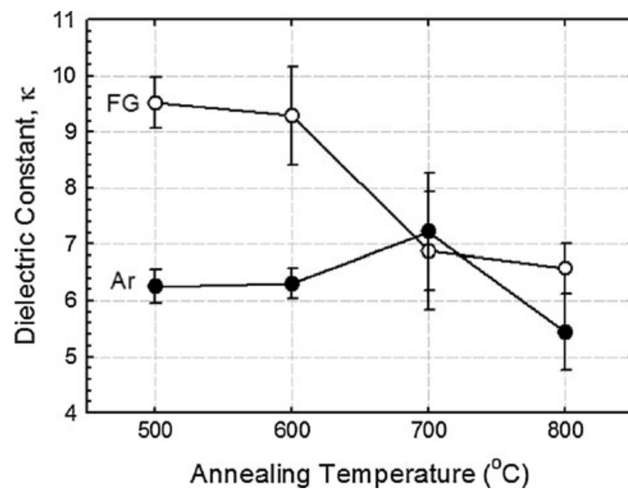

Fig. 9 Maximum, mean and minimum values of dielectric constant (κ) from three Sm_2O_3 dielectric films annealed at each specific annealing temperatures in Ar and FG ambient

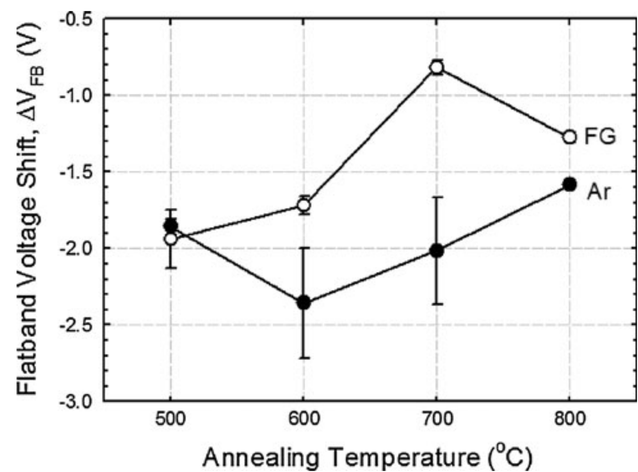

Fig. 10 Plot of error bars to show the average ΔV_{FB} of the investigated samples annealed in Ar and FG ambient as a function of annealing temperatures

show an opposite observation throughout the annealing temperatures, except for 800 °C. Reduction of average κ values of the samples annealed in Ar ambient may due to the growth of lower κ interfacial layer sandwiched between the Sm_2O_3 dielectric film and Si substrate during PDA [50], in which it reduces the total capacitance of MOS capacitor. Amount of the total capacitance (C_{Total}) of a capacitor containing interfacial layer is modeled by a series of capacitances as shown in (2) [17]

$$1/C_{Total} = 1/C_1 + 1/C_2 \quad (2)$$

where C_1 is the oxide film capacitance and, C_2 is the interfacial layer capacitance that proportional to its physical thickness. Thus, as the interfacial layer grows thicker at higher annealing temperature, the total capacitance of MOS capacitor will be reduced. However, increase of the κ value for FG annealed samples is due to densification of the Sm_2O_3 dielectric films upon PDA [49]. This justification is supported by the results of RMS surface roughness shown in the earlier section in which denser oxide films possessed smoother surface.

All of the investigated samples showed a negative shift of ΔV_{FB} as presented in Fig. 10. This indicates the presence of positive effective oxide charges (Q_{eff}) accumulated in the oxide films during PDA [17, 45, 50]. Q_{eff} is calculated based on Eq. 3 [17].

$$Q_{eff} = (\Delta V_{FB} C_{ox})/(qA_G) \quad (3)$$

where C_{ox} is the oxide capacitance and q is the electronic charge. Figure 11 compares the Q_{eff} determined from three investigated Sm_2O_3 dielectric films at each PDA temperatures in Ar and FG atmospheres, and they are presented in error bars. The overall ΔV_{FB} and Q_{eff} of FG annealed samples are smaller than Ar annealed samples. FG is a reducing gas and it tends to decompose to produce electrons at elevated temperatures [47]. During PDA, excess of electrons were supplied by the FG to neutralize the existing positive oxide charges in oxide films and thus, improving the ΔV_{FB} of the samples.

Another important parameter that can be extracted from the C–V measurement is interface trap density (D_{it}) (Fig. 12). D_{it} was determined by using Terman method (Eq. 4) [17].

$$D_{it} = [C_{ox} d(\Delta V_g)]/[qA_G d(\Phi_s)] \quad (4)$$

where ΔV_g is the difference of gate voltage in experiment and gate voltage of ideal curve and Φ_s is the surface potential of Si at a specific gate voltage.

The calculated amounts of D_{it} of FG annealed samples are smaller than the Ar annealed samples. For the samples being annealed in Ar ambient, the highest and the lowest D_{it} values are recorded at the annealing temperatures of 600 and 800 °C, respectively. D_{it} is influenced by the surface roughness of dielectric films. A rougher thin film surface contributed to a higher D_{it} as the charges are being trapped easily and vice versa [50]. The same justification is applied to the FG annealed samples. The variations of D_{it} and surface roughness as a function of annealing temperatures are demonstrated the same trend. The lowest D_{it} obtained in this study (Ar annealing: $\sim 3.8 \times 10^{12}$ eV^{-1} cm^{-2} and FG annealing: $\sim 1.1 \times 10^{12}$ eV^{-1} cm^{-2}) is lower than the results reported by Jeon et al. ($\sim 2.0 \times 10^{13}$ eV^{-1} cm^{-2}) at the surface potential of -0.1 eV [25].

Figure 13 displays the average total interface trap density (D_{Total}) of the Sm_2O_3 thin films annealed in Ar and FG ambient at various temperatures. D_{Total} was calculated from the area under the curve of D_{it} versus (E_c–E) [17]. The numbers of total interface trap density of FG annealed

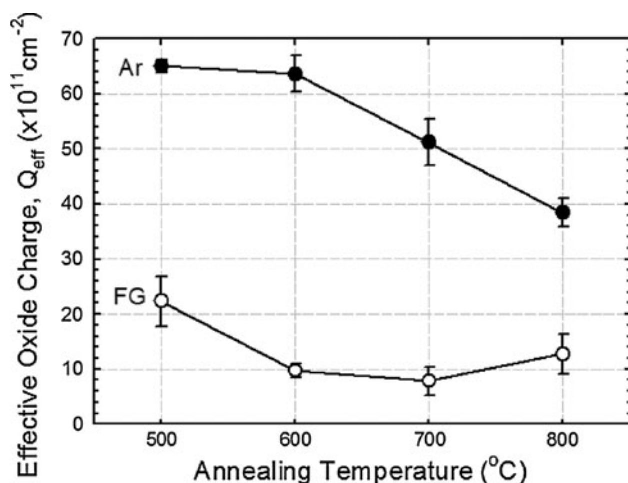

Fig. 11 Comparison of the maximum, mean and minimum effective oxide charge of Sm_2O_3 dielectric films annealed at two different atmospheres in *error bars*

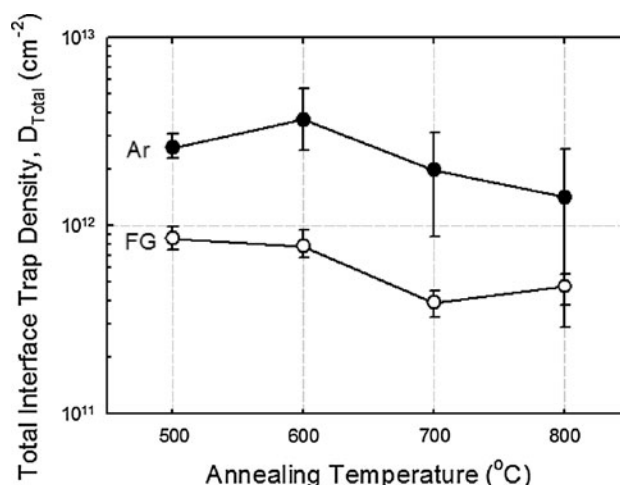

Fig. 13 Average total interface trap density of the Ar and FG annealed Sm_2O_3 dielectric films at various temperatures

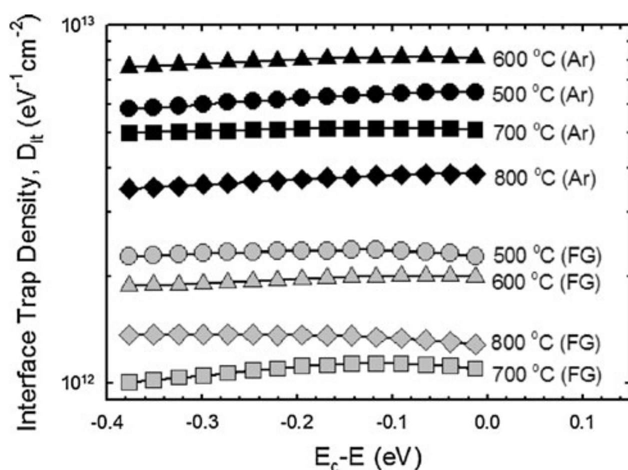

Fig. 12 Interface trap density versus surface potential of the Sm2O3 dielectric films annealed at different temperatures in Ar and FG atmospheres

samples are lower than the Ar annealed samples. The lowest D_{Total} obtained in this work are shown by the sample annealed at 700 °C in FG ambient (3.9626×10^{11} cm^{-2}).

As the same with C–V measurement, three samples from each specific PDA temperatures were tested with SPA to examine the I–V behavior. The average current density versus breakdown field characteristics of the $Al/Sm_2O_3/Si$ MOS capacitors at different annealing temperatures in Ar and FG atmospheres are illustrated in Fig. 14. The capacitor with dielectric films annealed in both different ambient showed an increasing trend of the average breakdown field as a function of annealing temperatures, except for the 800 °C annealed samples in FG ambient (Fig. 15). In overall, electric breakdown fields of all samples annealed in FG ambient are higher than the Ar ambient. The highest dielectric breakdown field ($\sim$6.76 MV cm^{-1}) is attained by the samples annealed at 700 °C in FG ambient as it has the lowest Q_{eff}, D_{it}, and D_{Total} when compared to the other samples [17, 45, 50].

In order to compute the barrier height (Φ_B) between conduction band edge of Sm_2O_3 film and of Si, Fowler–Nordheim (FN) tunneling model (Eq. 5) [17, 51] is employed. FN tunneling is a tunneling process whereby the electron passes through a triangular potential barrier into the conduction band of the oxide film [51].

$$J_{FN} = AE^2 \exp(-B/E) \quad (5)$$

where

$$A = \left(q^8 m_e\right) / (8\pi h m \Phi_B) \quad (6)$$

and

$$B = \left[4(2m)^{1/2}(\Phi_B)^{3/2}\right] / [(8qh)/(2\pi)] \quad (7)$$

where m_e is the free electron mass, m is the effective electron mass in the oxide and h is Planck's constant. The effective electron mass of 0.13 m_e was used as it had been determined previously for the Sm_2O_3 film on Si [34]. By plotting ln (J/E^2) vs 1/E (FN plot) (Fig. 16), Φ_B could be extracted from the slope (B) of the linear region of the graph.

In this study, all of the 500 °C annealed samples (both in Ar and FG ambient) did not show FN tunneling behavior as their electric breakdown field occurred before FN tunneling [17]. Figure 17 presents the relationship of average Φ_B of Sm_2O_3 dielectric films annealed at various temperatures in Ar and FG ambient. The overall Φ_B of FG annealed dielectric films is higher than the Ar annealed samples. As increasing the annealing temperatures, Φ_B of all investigated samples are increased, except for samples annealed at 800 °C in FG ambient. The highest Φ_B is attained by

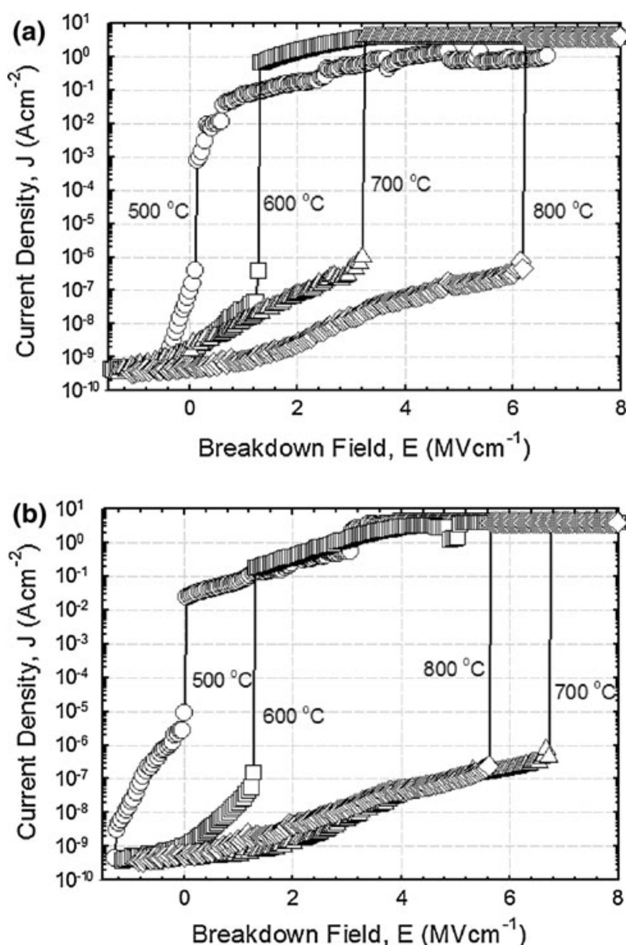

Fig. 14 Average J–V curves of Sm_2O_3 dielectric films annealed at different temperatures in **a** Ar, and **b** FG atmospheres

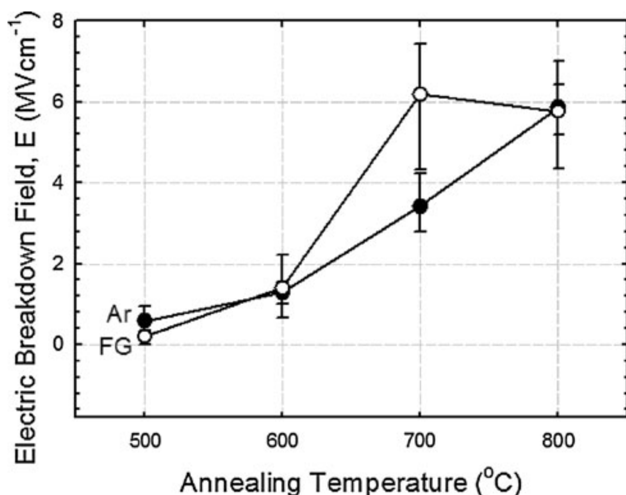

Fig. 15 Maximum, mean and minimum breakdown field of the investigated samples as a function of annealing temperatures in *error bars*

700 °C annealed sample in FG ambient (1.03 eV), which is higher than the values reported by Dahkel (0.85 eV) [31] and Ingram et al. (0.82 eV) [34]. Φ_B plays an important

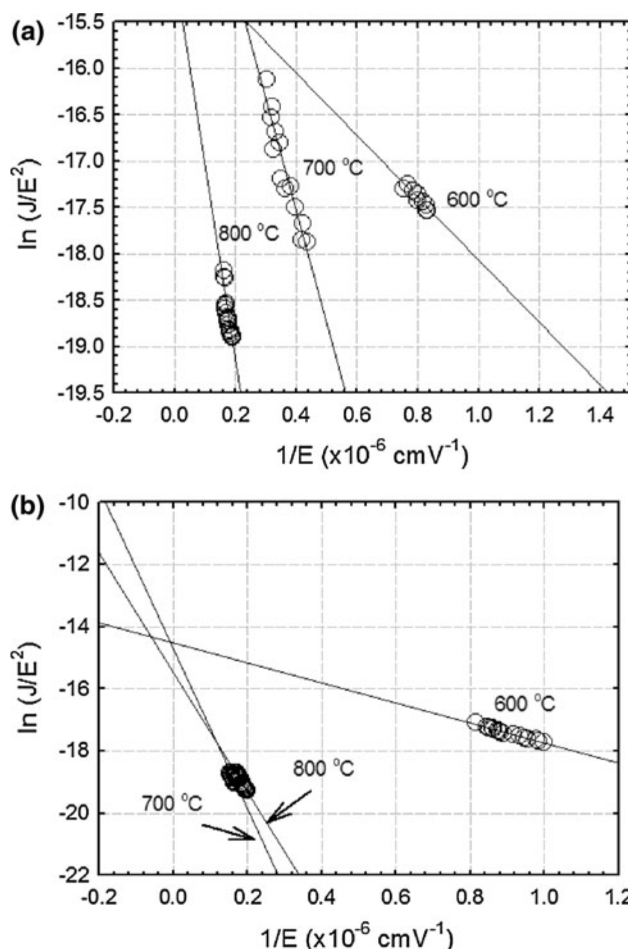

Fig. 16 FN tunneling plot (ln (J/E^2) vs. 1/E) of the Al/Sm_2O_3/Si MOS capacitor annealed in **a** Ar, and **b** FG atmospheres

role to the leakage current density of dielectric films [31]. As increased the Φ_B, probability of the charges (electrons) passes through the oxide film will be reduced and therefore, contributes to a lower leakage current density.

4 Conclusions

Sm_2O_3 thin films were deposited on n-type Si (100) substrate via RF-magnetron sputtering. PDA was carried out separately on the deposited thin films in Ar and FG (90% N_2 + 10% H_2) ambient at different temperatures (500, 600, 700, and 800 °C) for 30 min. X-ray diffraction revealed that all the annealed samples possessed polycrystalline structure with C-type cubic phase. FG annealing ambient had suppressed crystallization of the oxide films upon PDA. Atomic force microscope results indicated RMS surface roughness of the samples being annealed in Ar ambient were lower than FG annealed samples, but they were comparable at the annealing temperature of 700 °C (Ar—0.378 nm,

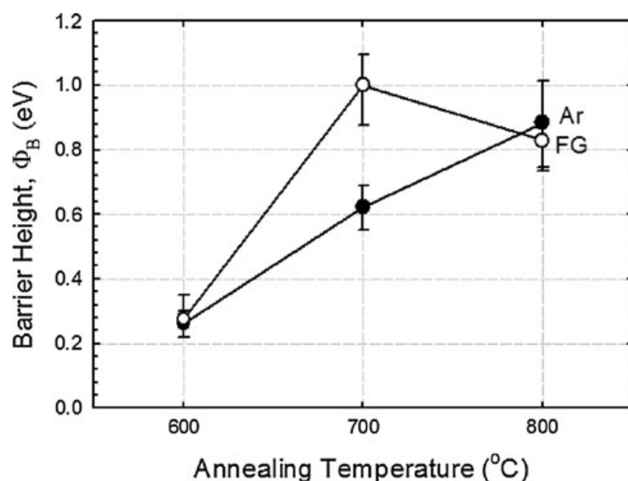

Fig. 17 Φ_B of the investigated samples at different annealing temperatures including maximum, mean and minimum values

FG—0.395 nm). For electrical characterization, FG annealing had successfully improved the ΔV_{FB} of MOS capacitor by supplying excess to electrons to neutralize the existing positive oxide charges in oxide film. Besides, the Sm_2O_3 thin films annealed in FG ambient showed smaller number of Q_{eff}, D_{it}, and D_{Total} than the oxide films annealed in Ar ambient. The highest dielectric breakdown field ($\sim$6.76 MV cm^{-1}) was attained by the samples annealed at 700 °C in FG ambient as it has the lowest Q_{eff}, D_{it}, and D_{Total}.

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