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# Study of the effect of thermal annealing on high *k* hafnium oxide thin film structure and electrical properties of MOS and MIM devices

**A. Srivastava · R. K. Nahar · C. K. Sarkar**

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**Abstract** The effect of rapid thermal annealing on structural and electrical properties of high *k* $HfO_2$ thin films is investigated. The films were initially deposited at pre-optimized sputtering voltage of 0.8 kV and substrate bias of 80 V in order to get optimized results for oxide charges and leakage current as a MOS device. The film properties were investigated for optimum annealing temperature in oxygen and optimum rapid thermal annealing temperature in nitrogen respectively to get the best electrical results as a MOS device structure. The film thickness, composition and microstructure is studied by Laser Ellipsometry, XRD and AFM and the effect of thermal annealing is shown. The electrical I–V and C–V characteristics of the annealed dielectric film were investigated employing Al-$HfO_2$-Si MOS capacitor structure. The flat-band voltage ($V_{fb}$) and oxide-charge density ($Q_{ox}$) were extracted from the high-frequency C–V curve. Dielectric study were further carried out on $HfO_2$ thin films having metal–insulator–metal (MIM) configuration over a wide temperature (300–500 K) and frequency (100 Hz to 1 MHz) range.

A. Srivastava (✉)
Electronics and Communication Engineering, Indian Institute for Information Technology Design and Manufacturing, PDPM-IIITD&M Jabalpur, Jabalpur, Madhya Pradesh 482005, India
e-mail: ashudel07@gmail.com

A. Srivastava · C. K. Sarkar
Department of Electronics & Telecommunication Engineering, Jadavpur University, Kolkata, India

R. K. Nahar
Sensors and Nanotechnology Group, Central Electronics Engineering Research Institute (CSIR, New Delhi), Pilani, Rajasthan 333031, India

## 1 Introduction

According to the ITRS roadmap, CMOS with gate length below 100 nm will require an oxide thickness of less than 2.0 nm, which corresponds to just few layers of silicon dioxide atoms. With such an ultra thin gate oxide, direct tunneling occurs resulting in an exponential increase of gate leakage current [1–7]. The increase in gate leakage current will increase the power dissipation leading to deterioration of device performance and circuit stability for ULSI circuits. High-*k* dielectric material is needed to overcome the problem [1, 2].

There are many high-*k* dielectric materials that are investigated to replace $SiO_2$ namely SiN, $TiO_2$, $Ta_2O_5$, $Al_2O_3$, $HfO_2$, $ZrO_2$. Unfortunately many of these materials are thermodynamically unstable on silicon. $HfO_2$ has emerged as one of the most promising high-*k* gate dielectric material, as it has relatively high dielectric permittivity value (25), high heat of formation (271 K cal/mol), high band gap (5.8 eV), compatibility with poly-silicon gate process, large conduction band offsets with Si, and solid-state thermodynamic stability on Si [1, 2]. There has been a lot of study already on different aspects of $HfO_2$ thin films as the As-deposited films have large oxide charge and leakage current. The technique used in deposition of $HfO_2$ thin film and post-deposition annealing plays a very important role in making good thin films with lesser leakage current and oxide charge density. High-*k* dielectric material are also drawing increasing attention as MIM capacitor for analog/mixed signal and rf integrated circuit application due to their higher capacitance density with the downward scaling of the capacitor area [8–12].

This paper investigates electrical and morphological effect of post deposition annealing (TA) in oxygen and post deposition rapid thermal annealing (RTA) in nitrogen at

different temperature for pre-optimized sputtered thin film as a MOS capacitor structure. The sputtering voltage and bias sputtering of the deposition machine has been pre-optimized at 0.8 kV and 80 V, respectively [11]. This paper further investigates dielectric behavior as a function of temperature and frequency ranging 300–600 K to from 100 Hz to 1 MHz respectively for pre-optimized sputtered thin film annealed in oxygen at 700 °C in oxygen as a MOS capacitor structure.

## 2 Experimental details

Five inch sputtering target of $HfO_2$ with high purity (99.9% purity) supplied by M/s Semiconductor technology was used to deposit the thin films using MRC RF sputtering machine. P-type silicon substrate were used to deposit $HfO_2$ which had 1–10 ohm-cm resistivity and (100) orientation. The wafers were cleaned using the standard pirana cleaning procedure in order to remove organic and inorganic contaminations. The wafers were etched in dilute HF (1: 20), rinsed in DI water and dried in dry $N_2$ immediately before loading in the vacuum chamber. The background pressure of the vacuum chamber was evacuated to $1.2 \times 10^{-6}$ torr and the sputtering was done in high purity argon ambient gas. The gas pressure was maintained at about 6 milli torr and the film deposited at 0.8 kV sputtering voltage and 80 V substrate bias for getting optimum results for oxide charges and leakage current keeping film thickness around 20 nm corresponding to equivalent oxide thickness of $SiO_2$ about 4.5 nm. The As-deposited films were further treated in two different manners. The first batch of As-deposited films was treated at three different temperatures in Oxygen for 15 min each. The second batch of As-deposited films was treated at three different temperatures in Nitrogen for 30 s (RTA) each. The top electrodes were Al dots deposited by thermal evaporator using shadow mask technique having diameter of around 500 microns and film thickness of about 200 nm while back contact was again deposited by thermal evaporator to get planar Al thin film having thickness of about 200 nm.

The thin film deposition for MIM configuration (Pt/$HfO_2$/Pt/Si) was done using a sputtering system with the gas pressure maintained at around 6 milli torr, 0.8 kV sputtering voltage and 80 V substrate bias in order to get optimum results for the oxide charges and the leakage current. The sputtered film thickness of $HfO_2$ was around 200 nm. The As-deposited films were further treated at 700 °C in Oxygen for 15 min. The top electrodes were Al dots deposited by the thermal evaporator using shadow mask technique having diameter of around 500 µm and film thickness of about 200 nm while back contact was again deposited by thermal evaporator to get planar Al thin film having thickness of about 200 nm. The physical thickness $T_{ox}$ of the high-$k$ gate dielectric is measured to be around 22 nm for MOS capacitor and 200 nm for MIM capacitor; measured using Laser Ellipsometer (Sentech Instruments Laser-Pro). The nanostructure was examined by VEECO-CPII Atomic Force Microscope. The refractive index of as deposited film as well as post annealing film was measured by Matricon 2010 system. We observed an increasing trend from 1.632 for as deposited films to 1.772, 1.868, 1.912 for post annealed films from 600 to 800 °C. The X-ray diffraction was carried out using D8 Discover with GADDS. The capacitance voltage characteristics were measured on Agilent (HP) mode 4284A LCR meter and semiconductor parameter analyzer 4145A was used for current voltage characteristics. Electrical parameters like flat-band voltage ($V_{fb}$), and oxide-charge density ($Q_{ox}$) for different types of samples were extracted using the HF C–V curves and listed in Table 1. The dielectric properties of $HfO_2$ films were studied as a MIM capacitor configuration using an impedance analyzer HP 4294A in the frequency range of 100 Hz to 1 MHz.

**Table 1** Electrical property of the post deposited annealed sputtered samples

| | TA600 °C | TA700 °C | TA800 °C |
|---|---|---|---|
| $V_{fb}$ (V) | −4.27 | −1.08 | −2.87 |
| $Q_{ox}$ ($10^{11}$ cm$^{-2}$) | 23.43 | 5.39 | 16.54 |
| | RTA600 °C | RTA700 °C | RTA800 °C |
| $V_{fb}$ (V) | −4.56 | −3.24 | −2.07 |
| $Q_{ox}$ ($10^{11}$ cm$^{-2}$) | 48.83 | 34.36 | 12.54 |

## 3 Results and discussions

### 3.1 Thermal annealing in oxygen for 15 min

Gate leakage current is an important device parameter. To evaluate the gate leakage performance of the devices, the I–V characteristics is measured both in accumulation and inversion region. The I–V characteristics of sputtered $HfO_2$ MOS capacitor deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed under different temperature in oxygen is shown in Fig. 1. It is observed that the leakage current increases with the increase in annealing temperature from 600 to 700 °C but declines gradually from 700 to 800 °C. These leakage current have opposite trends and therefore demands a trade off when designing a good gate dielectric film.

The high frequency (1 MHz) C–V curves of sputtered $HfO_2$ thin film as MOS capacitor, deposited at sputtering

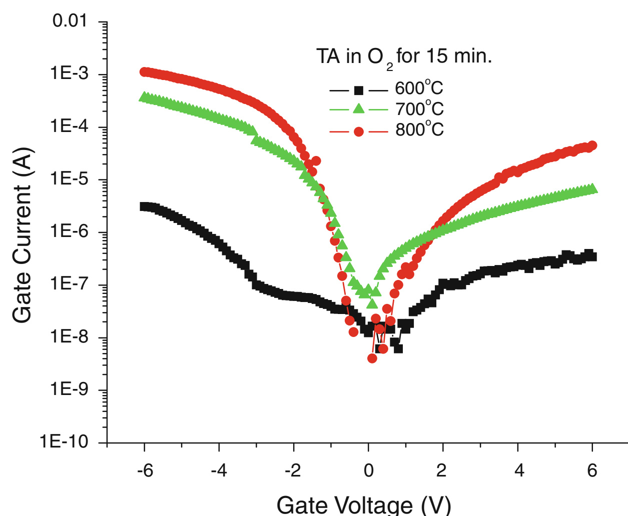


**Fig. 1** I–V characteristics of sputtered $HfO_2$ thin film MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed under different temperature in oxygen

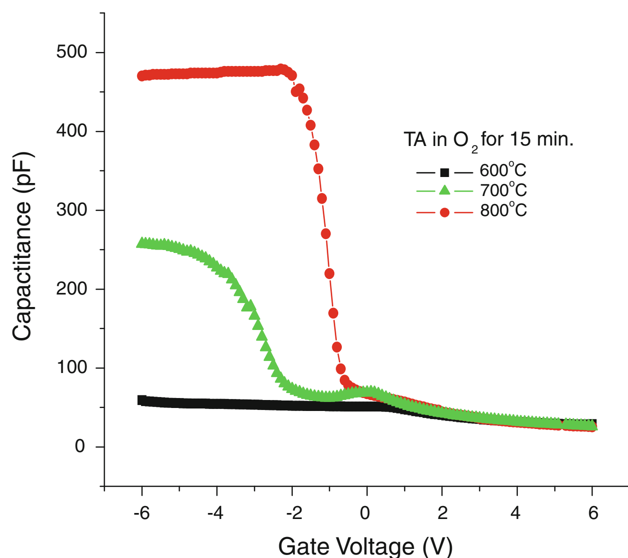


**Fig. 2** Comparison of C–V characteristics of sputtered $HfO_2$ thin film MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed under different temperature in oxygen

voltage of 0.8 kV and substrate bias of 80 V annealed under different temperature in oxygen is shown in Fig. 2. It may be noted that the oxide capacitance ($C_{ox}$) is found to rise with annealing temperature going from 600 to 700 °C, indicating improvement in oxide stoichiometry with annealing. Since higher annealing temperature or longer duration stimulates the local crystallization of $HfO_2$ and with it the growth of low-*k* interface layer between silicon and the bulk $HfO_2$, the effective oxide capacitance falls as can be seen for temperature at 800 °C in Fig. 2. These effects have opposite trends and therefore demands a trade off when designing a good gate dielectric film. In depletion region, a smear out effect is noted mainly for samples annealed at low temperature whereas the C–V characteristic of the sample annealed at the 700 °C exhibits the least stretch out implying the reduction of the interface states at this temperature revealing that the annealing temperature should be chosen around 700 °C.

The flat band voltage shift for sputtered films deposited and annealed in oxygen at different temperature is compared in Table 1. The oxide charges and interface states are the main factors that govern the shift in flat band voltage. It is observed that oxide charges is minimum for 700 °C, increases at 800 °C and maximum for 600 °C which is due to maximum stretch out in the depletion region.

The breakdown characteristics of sputtered $HfO_2$ thin film as MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed under different temperature in oxygen is shown in Fig. 3. It is observed that breakdown voltage for the post deposited sputtered film as a MOS capacitors annealed in oxygen at 600 °C has the maximum value of 40 V while at 700 °C has least value of 5 V and at 800 °C has around 12 V.

Figure 4a shows the XRD measurements of sputtered 20 nm $HfO_2$ thin film deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed in oxygen at 600, 700 and 800 °C. Hafnium oxide shows amorphous structure but starts to crystallize at 600 °C and the crystalline behavior increases with the increase in temperature. Surface morphology of the thin film affects the electrical properties of the MOS capacitor structure and the

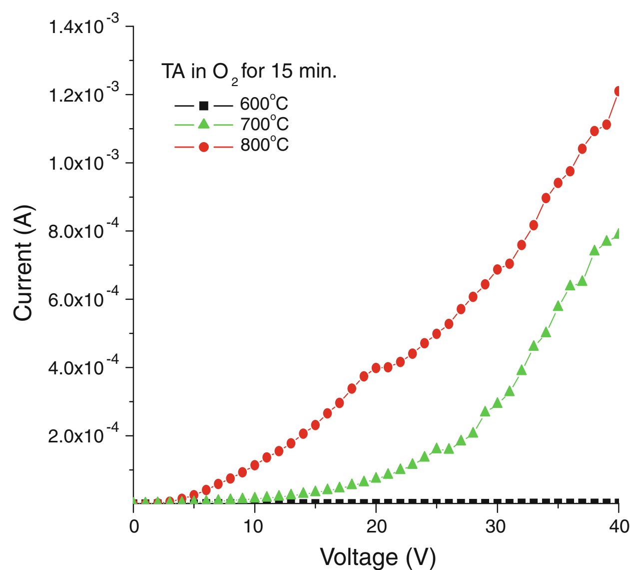


**Fig. 3** Breakdown characteristics of sputtered $HfO_2$ thin film MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed under different temperature in oxygen

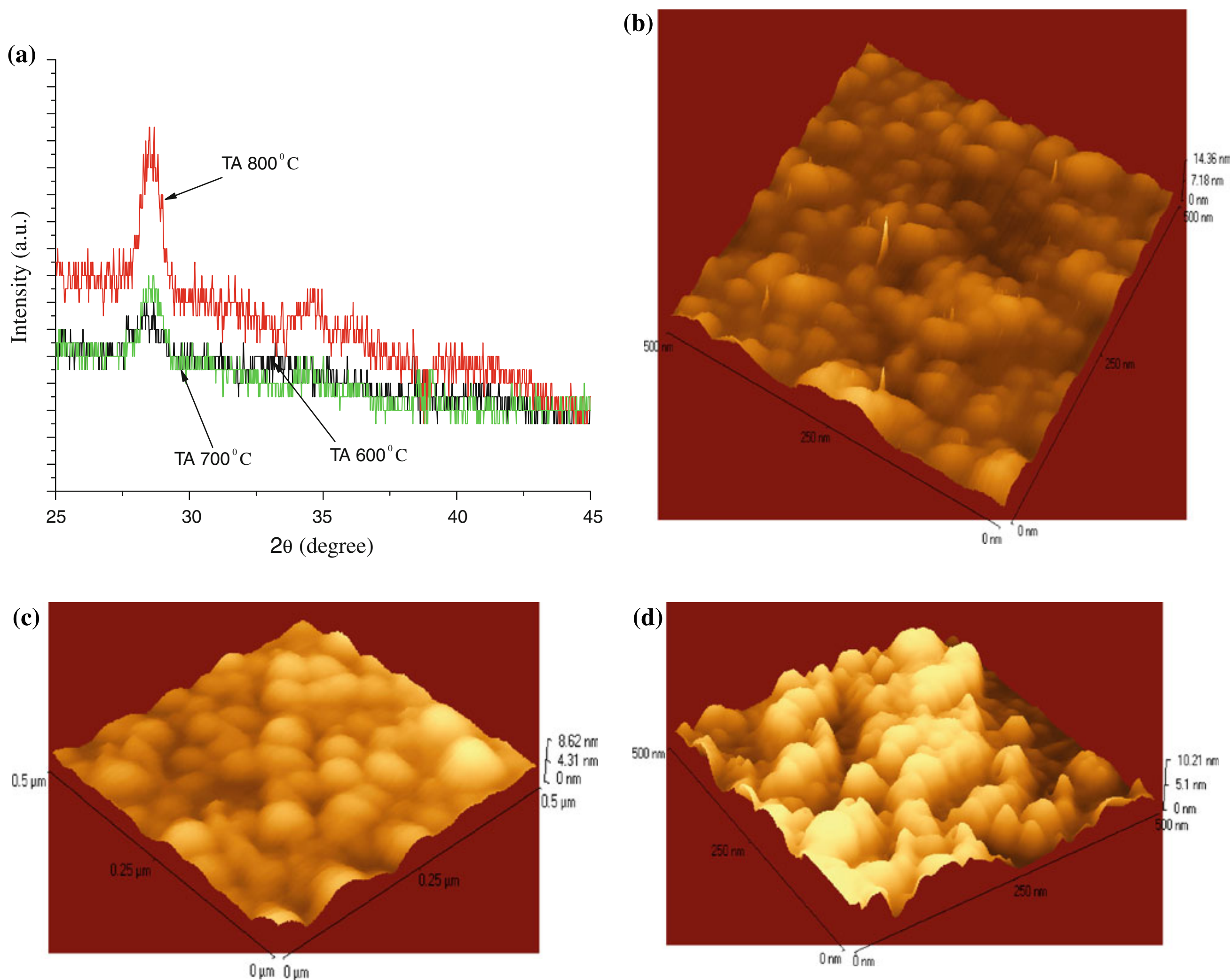


**Fig. 4** **a** XRD pictures and 3 D AFM pictures of sputtered $HfO_2$ film deposited at sputtering voltage of 0.8 kV, substrate bias of 80 V and thermally annealed in oxygen for 15 min at **b** 600 °C, **c** 700 °C, **d** 800 °C

improvement in the film properties is attributed to improvement in microstructure of the thin film. The 3 D AFM pictures of sputtered 20 nm $HfO_2$ thin film deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed in oxygen at 600, 700 and 800 °C are shown in Fig. 4b–d, respectively. It is observed from Fig. 4b–d that size of nano-structures are 14.4, 8.9 and 22 nm for 600, 700, and 800 °C, respectively. The variation of rms roughness and average roughness with temperature is tabulated in Table 2. The AFM nanostructures shows that the film surface roughness reduces maximum for post deposited sputtered samples thermally annealed in oxygen at 700 °C. It seems as the temperature is raised from 600 to 700 °C there is breaking of nanostructures but if the temperature is raised further from 700 to 800 °C the smaller nanostructure combine together to form a bigger nanostructure.

**Table 2** RMS and Average roughness of the post deposited annealed sputtered samples

| | TA600 °C | TA700 °C | TA800 °C |
|---|---|---|---|
| Rms roughness (nm) | 1.4 | 1.5 | 2.9 |
| Average roughness (nm) | 1.2 | 1.2 | 2.5 |
| | RTA600 °C | RTA700 °C | RTA800 °C |
| Rms roughness (nm) | 1.6 | 1.6 | 0.6 |
| Average roughness (nm) | 1.3 | 1.4 | 0.5 |

### 3.2 Dielectric study of MIM capacitor thermally annealed in oxygen for 15 min

X-ray diffraction (XRD) pattern of $HfO_2$ film of thickness of ∼0.2 mm deposited on platinized-silicon (Pt/Si) substrate at 700 °C is shown in Fig. 5. A dominant reflection

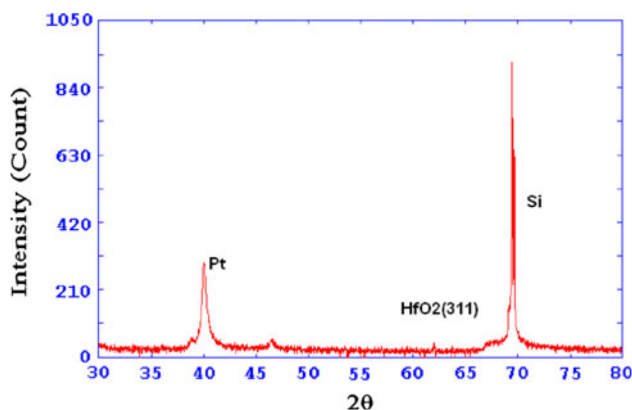


**Fig. 5** XRD pictures of sputtered $HfO_2$ film deposited at a sputtering voltage of 0.8 kV, substrate bias of 80 V and thermally annealed in oxygen for 15 min at 700 °C

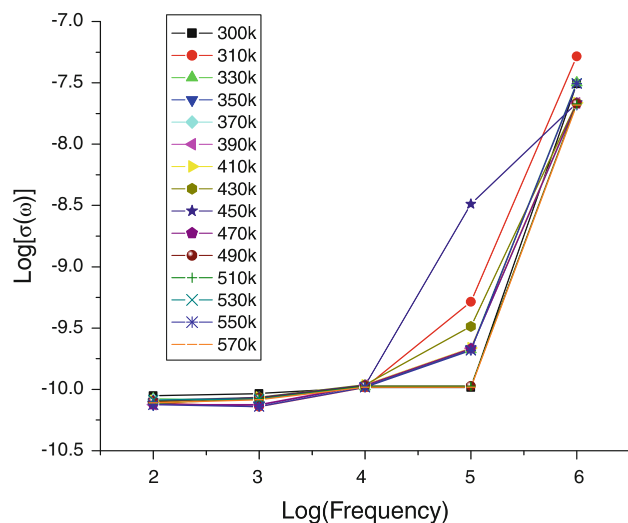


**Fig. 6** Log–log plot of $\sigma(\omega)$ of sputtered $HfO_2$ film as a function of frequency at different temperatures

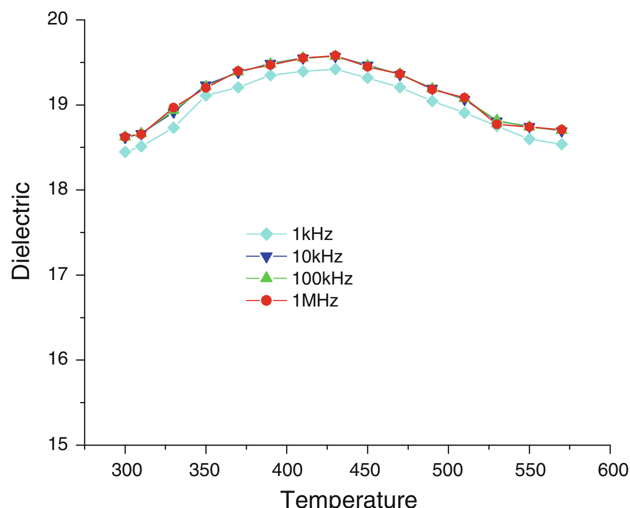


**Fig. 7** Dielectric permittivity of sputtered $HfO_2$ film as a function of temperature at different frequencies

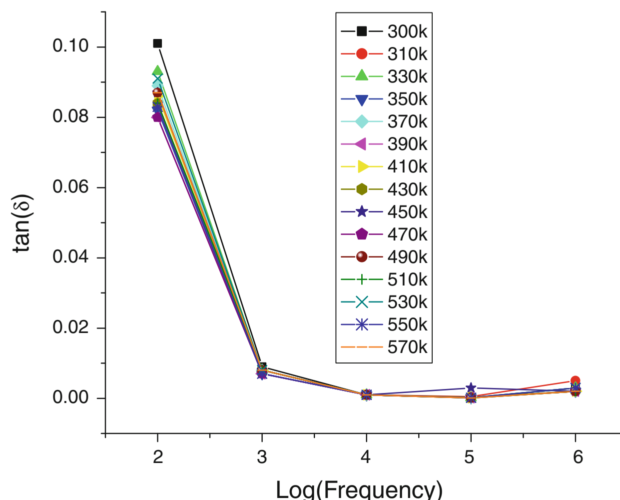


**Fig. 8** Dielectric loss (tan $\delta$) of sputtered $HfO_2$ film as a function of temperature at different frequencies

corresponding to (311) directions was observed along with the weak XRD peaks indicating that the preferential growth of $HfO_2$ film is along (311) on the Pt/Si substrate.

The variations of $\sigma(\omega)$ as a function of frequency measured at different temperatures are shown in Fig. 6. The estimated value of $\sigma(\omega)$ was found to increase slightly at higher frequency for all temperature regions. The variation of measured dielectric constant $\varepsilon(\omega)$ as a function of temperature at the fixed frequencies (1, 10, 100 kHz, and 1 MHz) is shown in Fig. 7. We observe that dielectric permittivity is almost constant for all temperatures and frequencies which is around 19. The variations of dielectric loss tan ($\delta$) as a function of frequency measured at different temperatures are shown in Fig. 8. The value of tan ($\delta$) was found to increase slightly at lower frequency for all temperature regions.

### 3.3 Rapid thermal annealing in nitrogen for 30 s

The I–V characteristics of sputtered $HfO_2$ thin film as MOS capacitor structure deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V annealed under different RTA temperature in nitrogen for 30 s is shown in Fig. 9. It is observed that the leakage current increases with the increase in annealing temperature from 600 to 700 °C while decreases with the increase in annealing temperature from 700 to 800 °C. These leakage current have opposite trends when we see it in the inversion region for 800 °C which forces us to choose around 800 °C as an optimum temperature for minimum leakage current.

The high frequency (1 MHz) C–V curves of sputtered $HfO_2$ thin film as MOS capacitors structure deposited at

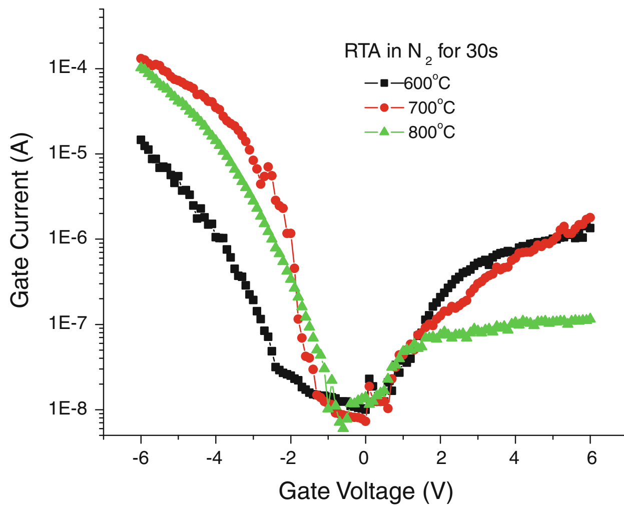


**Fig. 9** I–V characteristics of sputtered $HfO_2$ thin film MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V rapidly thermal annealed under different temperature in nitrogen

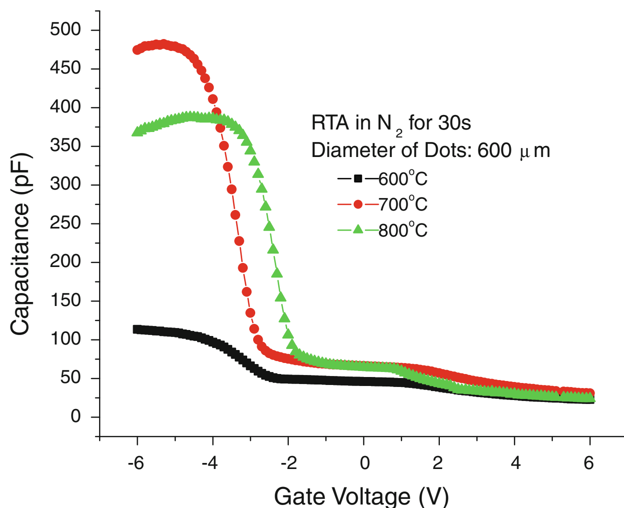


**Fig. 10** Comparison of C–V characteristics of sputtered $HfO_2$ thin film MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V rapidly thermal annealed under different temperature in nitrogen

sputtering voltage of 0.8 kV and substrate bias of 80 V annealed under different RTA temperature in nitrogen is shown in Fig. 10. It is observed that the oxide capacitance ($C_{ox}$) is found to rise with RTA temperature indicating improvement in oxide stoichiometry with annealing. This can be attributed to the fast introduction of nitrogen at high temperature making the compound into hafnium oxy-nitride. One can observe that the effective oxide capacitance rise to maximum at 700 °C as can be seen in Fig. 10. This directly improves the dielectric permittivity *k*-value of the new gate dielectric stack. The flat band voltage shift for films deposited under RTA in nitrogen for 30 s is compared

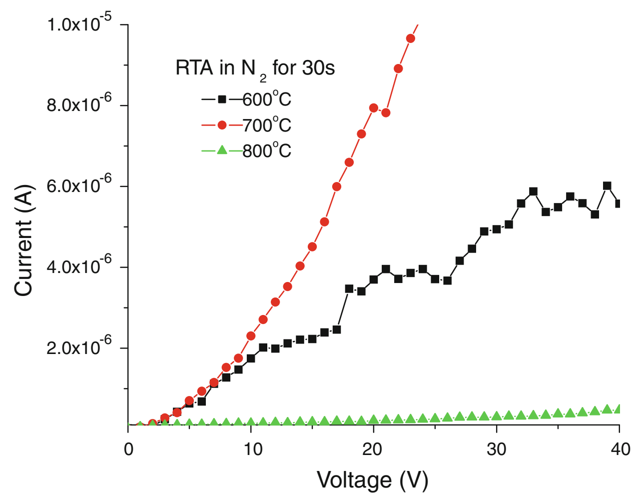


**Fig. 11** Breakdown characteristics of sputtered $HfO_2$ thin film MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V rapidly thermal annealed under different temperature in oxygen

in Table 1. The oxide charges and interface states are the main factors that govern the shift in flat band voltage. It is observed that oxide charges is minimum for annealing temperature of 800 °C and increases with decrease in annealing temperature done with RTA.

The breakdown characteristics of sputtered $HfO_2$ thin film as MOS capacitors structure deposited at optimized sputtering parameters of RTA under different temperatures in nitrogen is shown in Fig. 11. It can be observed from Fig. 11 that breakdown for the film deposited under optimized rf parameters in nitrogen at 600 °C is around 6 V, at 700 °C is around 7 V and at 800 °C is around 7 V for post deposited RTA MOS capacitors.

Figure 12a shows the XRD measurements of sputtered 20 nm $HfO_2$ thin film deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V RTA in nitrogen for 30 s at 600, 700 and 800 °C. Hafnium oxide shows amorphous structure at 600 and 700 °C and begins to crystallize at 800 °C. The RTA of post deposition sputtered samples in nitrogen exhibits higher crystalline temperatures with respect to samples thermally annealed in oxygen. Surface morphology of the thin film that effects electrical properties of the MOS capacitor structure and the improvement in the film properties which is due to improvement in microstructure of the thin film is discussed for the hafnium oxide gate dielectric stack annealed in nitrogen. The 3 D AFM pictures of sputtered 22 nm $HfO_2$ thin film as MOS capacitors deposited at sputtering voltage of 0.8 kV and substrate bias of 80 V, post deposited RTA in nitrogen at 600, 700 and eight 800 °C are shown in Fig. 12b–d, respectively. The variation of rms roughness and average roughness with temperature is tabulated in Table 2. The AFM nanostructures shows that the film surface roughness

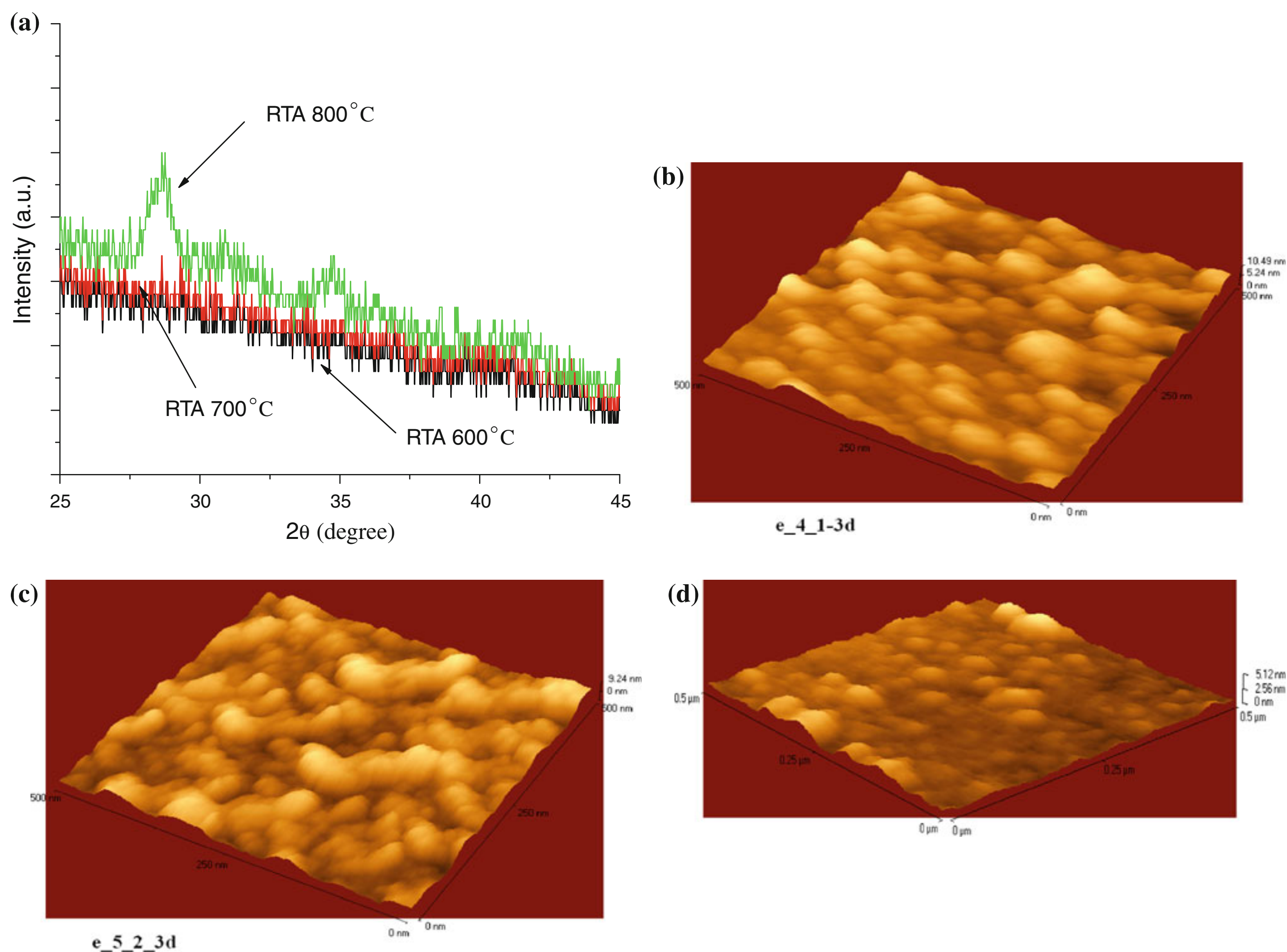


**Fig. 12** **a** XRD pictures and 3 D AFM pictures of sputtered $HfO_2$ film deposited at sputtering voltage of 0.8 kV, substrate bias of 80 V and rapid thermally annealed in Nitrogen for 30 s at **b** 600 °C, **c** 700 °C, **d** 800 °C

reduces maximum for post deposited sputtered samples RTA in nitrogen at 800 °C. It is found that size of nano-structures decreases with increase in temperature as shown in Fig. 12b–d. The nano-structures are around 10.49, 9.24 and 6.74 nm for RTA temperatures of 600, 700, and 800 °C, respectively. It seems as the temperature is raised there is breaking of nanostructures of Hf–O–N gate dielectric stack resulting in reduction of oxide charge density.

## 4 Conclusions

It seems the best post deposited annealing temperature in oxygen for excellent electrical properties of hafnium oxide thin film MOS capacitor deposited at post-optimized sputtering voltage of 0.8 kV and substrate bias of 80 V is around 700 °C. This includes lower oxide-charge densities, lower leakage current and higher gate dielectric permittivity which may be attributed to the least size of nano-structures and lower film surface roughness of samples annealed in oxygen at 700 °C which is around 9 and 1.2 nm, respectively. The above conclusions can also be attributed to the XRD results of hafnium oxide which starts to crystallize at 600 °C and increases its crystalline nature with the further increase in temperature.

Dielectric study of $HfO_2$ thin films deposited on platinized silicon substrate using RF-sputtering deposition technique have been carried out in the metal–insulator–metal configuration over a wide temperature (300–500 K) and frequency (100 Hz to 1 MHZ) ranges. The films were deposited at pre-optimized sputtering voltage of 0.8 kV, substrate bias of 80 V and annealing temperature of 700 °C in oxygen in order to get the best results for oxide charges and leakage current as a MOS capacitor. XRD peaks indicate that the preferential growth of sputtered 200 nm thin film $HfO_2$ is along (311) on Pt/Si substrate. The ac conductivity showed weak temperature dependence, but slight increase with increasing frequency. The dielectric permittivity for all temperatures and frequencies was

around 19, while the dielectric loss tan ($\delta$) slightly increased at lower frequency for all temperature regions.

The leakage current is relatively higher which triggered us to do a further study of rapid thermal annealing in nitrogen. The RTA in nitrogen resulted in further lowering of leakage current. One observes lower oxide-charge densities, higher breakdown voltage and relatively higher gate dielectric permittivity for post deposited sputtered samples RTA in nitrogen at a higher temperature of 800 °C. This further improvement can be attributed to further lowering of nano-structures under rapid thermally annealed samples in nitrogen. AFM pictures also show that there is an improvement in roughness average (i.e. the quality of AFM film) for rapidly thermally annealed film in nitrogen as compared to thermally annealed in oxygen. Moreover, there is an improvement in the quality of films, in terms of roughness average with increase in temperature under rapidly thermally annealed conditions, which is about 0.6 nm at higher temperature. The shift in temperature for extraction of optimum electrical properties of the post deposited annealed samples in RTA to 800 °C in nitrogen can also be attributed to the XRD results of hafnium oxide which exhibits higher crystalline temperatures with respect to samples thermally annealed in oxygen.

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