

Capacitance–voltage characteristics of Pt/Bi₂VO_{5.5}/p-Si structures

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Received: 4 March 2010 / Accepted: 6 July 2010 / Published online: 18 July 2010
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Abstract Ferroelectric Bi₂VO_{5.5} thin films were fabricated on p-type (100) Si substrates by sol–gel method and then annealed at different temperatures. The microstructures and surface morphologies of the Bi₂VO_{5.5} thin films were examined by X-ray diffraction and atomic force microscope, respectively. The results indicate that the Bi₂VO_{5.5} thin films show high *c*-axis preferred orientation and are compatible well with p-type Si substrates. The capacitance–voltage characteristics of Pt/Bi₂VO_{5.5}/Si capacitors measured at 1 MHz shows a clockwise hysteresis loop. The memory window of the hysteresis loop is 0.42 V with the gate voltage from –4 to 4 V. It is found that the memory window may be determined by the competition between ferroelectric polarization and charge injection.

1 Introduction

Recently, ferroelectric thin films have attracted more and more interests due to their applications for ferroelectric random access memory (FeRAM) [1], which has been developed as an ultimate memory with both nonvolatility and high-speed of read/write operation cycle [2]. Among these various types of FeRAM, ferroelectric field effect

transistor, wherein ferroelectric thin film as the substitute of gate oxide, has the advantage of small cell size, simple process and low power consumption, compared with other field effect transistors (FET). In the past, the ferroelectric materials such as SrBi₂Ta₂O₉ [3], Pb(Zr,Ti)O₃ [4], BiFeO₃ [5] and (Bi, La)Ti₃O₁₂ [6], have been studied. Compared with other materials, the materials with bismuth layer structures have better fatigue properties, which have drawn more attentions of the researchers.

Bismuth vanadate (Bi₂VO_{5.5}, BVO) is one of the most promising ferroelectric materials with single bismuth layer structure, particularly for its application to FET-type FeRAM configured [2]. Over the last few years, the BVO thin films have been fabricated by different methods including MOCVD, chemical solution decomposition [2, 7] and pulsed laser deposition [8, 9]. Among these methods, sol–gel has been extensively employed to fabricate ferroelectric oxide thin films because of its simplicity, low cost and easy compositional and structural control of the films [4, 7].

In this paper, we studied the fabrication of ferroelectric Bi₂VO_{5.5} thin films on p-type silicon (100) by sol–gel method; both structural and electrical properties of the films with different annealing temperatures have been investigated; the effects of different annealing temperatures on the structural and electrical properties of the BVO thin films have been demonstrated.

2 Experimental

The BVO thin films were prepared by sol–gel method using bismuth nitrate [Bi(NO₃)₂] and ammonium metavanadate [NH₄VO₃] as raw materials. Ammonium metavanadate was initially dissolved in a mixture of acetic acid and ethylene glycol with stirring. Then acetyl acetone was

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added into the prepared solution to increase its stability. Finally bismuth nitrate was added into the solution. The resultant solution was stirred for 0.5 h to form the BVO precursor. Before spin-coating, the p-type Si(100) substrates were preheated in air at 200 °C for 3 min. Each individual layer, spinning coated at 3,000 rpm for 20 s, was baked at 350 °C for 3 min to remove solvents and residual organics. Totally 8 layers were deposited on the Si substrate. Then the samples were annealed using a rapid thermal process furnace at 550, 600, 650 and 700 °C, respectively. All the processing was performed in the air.

X-ray diffraction (XRD, Rigaku D/max-2200) with CuK α was used for phase analysis of the films. The surface microstructure of the films was examined using contract mode atomic force micrograph (AFM, Dimension 3100). The cross sectional scanning electron micrograph (SEM, JSM-5610) was utilized to confirm the thickness of 400 nm for the film. Top Pt electrodes with a diameter of 300 μ m were deposited on the surface of the films through the mask. The capacitance–voltage (*C–V*) characteristic measurement was carried out at 1 MHz using Alpha-A High Performance Frequency Analyzer.

3 Results and discussion

Figure 1 shows the typical X-ray diffraction (XRD) patterns of the BVO thin films deposited on p-type Si annealed at 550–700 °C. As is shown, the diffraction peaks of the films above 600 °C reveal strong BVO (00*l*) reflections, which indicate the high *c*-axis-preferred orientation [10] of the BVO films. With the increase of the annealing temperature, the peaks become much stronger and sharper due to further enhancement in crystallization. Typically, the calculated widths at half maximum of (002) are 0.55°, 0.2° and 0.1° for the annealing temperatures at 600, 650 and 700 °C, respectively. The XRD patterns of the BVO films fabricated on Si substrates suggest that higher annealing

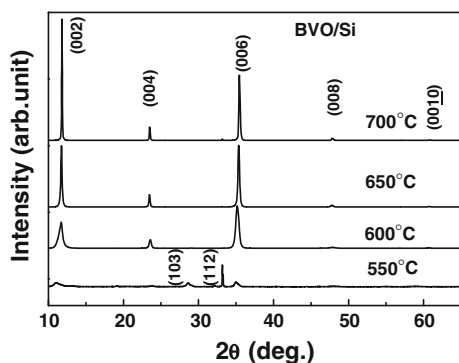


Fig. 1 XRD patterns of the BVO thin films deposited on p-type Si (100) substrates at various annealing temperatures

temperature leads to stronger *c*-axis-preferred orientation of the films.

Microstructure and surface morphology of the BVO thin films annealed at different temperatures were characterized by AFM. Figure 2a–c show the three dimensional and surface micrographs of the BVO thin films annealed at 600, 650 and 700 °C, respectively. From the pictures, homogeneous distribution of grains in the BVO thin films was observed. The films have relatively smooth surfaces without cracking, which indicates good microstructure qualities of the BVO thin films deposited on the Si substrates. From the two dimensional micrographs of the BVO thin films in Fig. 2, it is obvious that the grain size increases from 250 nm to 650 nm with the annealing temperature increasing from 600 to 700 °C. The root-mean-square (RMS) value of the surface roughness increases with the annealing temperature increasing. The values of RMS increase from 5.085 to 11.048 nm with the annealing temperature increase from 600 to 700 °C. The results demonstrate that the grain size and the value of RMS are dependent on the annealing temperature of the thin film.

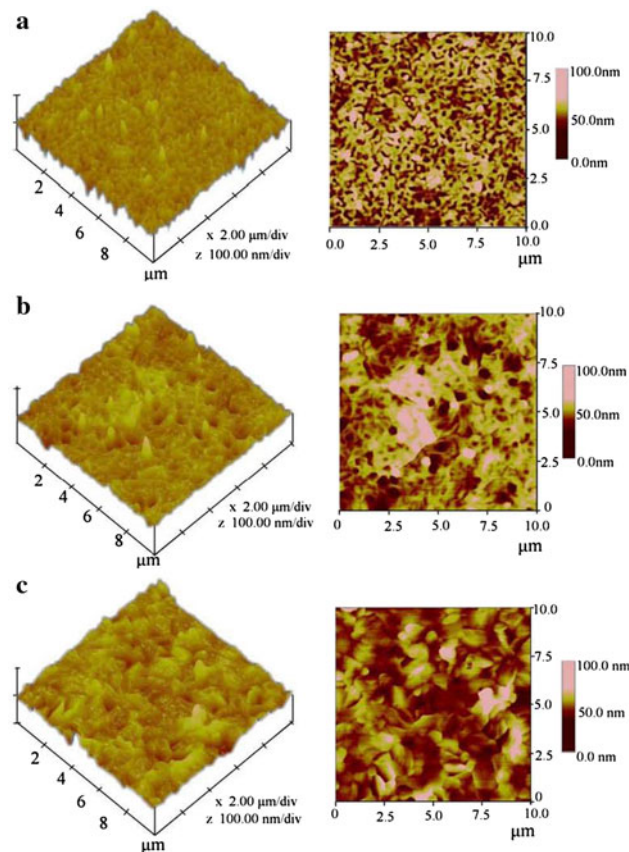


Fig. 2 AFM three dimensional and surface micrographs of BVO thin films annealed at **a** 600 °C, **b** 650 °C, and **c** 700 °C, respectively

The C - V properties of the Pt/BVO/Si structures are shown in Fig. 3. It can be found that the C - V curves show clockwise hysteresis loops for the -4 to 4 V sweep voltage, i.e., the memory window of the metal/ferroelectric/semiconductor (MFS) structure. These hysteresis loops are induced by the process of the switched ferroelectric polarization. It is also obvious that the C - V curves show different shapes with the various annealing temperatures. In order to compare with other annealing temperatures, we define here the memory window as the width of the hysteresis loops at half of its normalized capacitance. When the annealing temperature is 650 °C, the C - V curve shows a maximal memory window and the value is about 0.4 V. However, when the annealing temperatures are 600 and 700 °C, the memory windows decrease to 0.21 and 0.2 V, respectively. The value of the memory window is closely related to the polarization of the ferroelectric layer and the charge injection from the substrate or/and the metal gate electrode [5]. It is reported that the ferroelectric polarization of the BVO thin films increases with the annealing temperature in range of 600 – 700 °C [7], which can lead to larger memory window. When the annealing temperature reaches 700 °C, the interfaces characteristic of BVO/Si would deteriorate to some extent. Consequently, charge injection at this interface alters correspondingly and in turn can affect the memory window significantly. This may be the main cause for the decrease of the memory window at 700 °C, as shown in Fig. 3.

Figure 4 shows the memory window of the C - V characteristics for PT/BVO/Si structure vs different sweep voltages at 1 MHz. The C - V curves also show hysteresis loops with a clockwise trace as expected for MFS capacitor fabricated on p-type Si. At the sweep voltage 2 , 3 and 4 V, the memory window value of the MFS structure are 0.05 , 0.11 and 0.42 V, respectively. It is obvious that the value increases slightly with the applied voltage and shows a maximum value of 0.42 V when the sweep voltage is 4 V. The increase of the memory window can be explained by

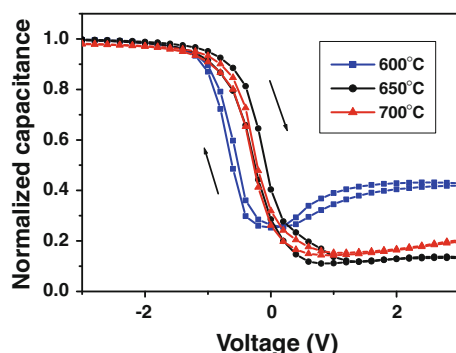


Fig. 3 C - V characteristics of the Pt/BVO/Si capacitors at different annealing temperatures

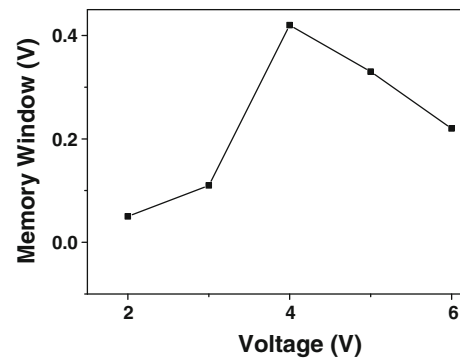


Fig. 4 The variation of the memory window of the Pt/BVO/Si structure at different sweep voltages

the fact that the polarization and the coercive voltage are being increased with the applied voltage [2, 5]. With the increase of the sweep voltage above 4 V, the memory window decreases. This could be attributed to the charge injection [2]. The results indicate that the memory window increase due to the increase of ferroelectric polarization for higher sweep voltage, while the injection charge which appears at much higher sweep voltage (above 4 V) may decrease the memory window.

4 Conclusions

In summary, the BVO thin films with good structure and morphology were prepared on p-type Si substrates by sol-gel spin coating method. The XRD results indicate that the prepared BVO thin films show high c -axis orientations. AFM results reveal the homogeneous distribution of grains, and the grain size was found to increase with the annealing temperature. The C - V characteristics of the Pt/BVO/Si MFS structure have been discussed in terms of the competition between ferroelectric polarization and charge injection. The maximum value of memory window of BVO was about 0.42 V at the gate bias of 4 V for the sample annealed at 650 °C.

Acknowledgments This work was supported by the National Natural Science Foundation of China (No. 60990312), the State Key Basic Research Program of China (2007CB924902), Shanghai Leading Academic Discipline Project (B411) and Science and Technology Commission of Shanghai Municipality (10JC1404600).

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