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REVIEW

High-κ dielectrics and advanced channel concepts for Si MOSFET

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Abstract With scaling of the gate length downward to increase speed and density, the gate dielectric thickness must also be reduced. However, this practice which has been in effect for many decades has reached a fundamental limitation because gate dielectric thicknesses in the range of tunneling have been reached with the SiO_2 dielectric layer for MOSFETs. Consequently, the gate dielectrics with higher dielectric constants, dubbed the "high-κ", which allow scaling with much larger thicknesses have become active research and development topics. In this review technological issues associated with the likely high-κ materials which are under consideration as well as challenges, and solution to them, they bring about in the fabrication of Si MOSFET are discussed. Moreover, in order to squeeze more speed out of CMOS, channels for both *n*- and *p*-type MOSFET enhanced with appropriate strain and the concepts behind them are discussed succinctly. Finally, the longer term approach of replacing Si with other channel materials such as GaAs (InGaAs) for *n*-channel and Ge for *p*-channel along with technological developments of their preparation on Si and likely gate oxide developments are treated in some detail.

1 Introduction

Since the inception of the integrated circuit in 1959, the Si based semiconductor industry has enhanced the performance of integrated circuit following Moore's law [1]. By about 1965, Gordon Moore observed that for silicon-based integrated circuits the number of transistors per square centimeter doubled every 12 months. The doubling took hold in the industry and the industry even at the time of the writing lives or dies by the observation providing a tremendous impetus to stay on or about the line extrapolated by Moore's law. Actually, throughout the 1970s and 80s, the doubling time was closer to 18 months. However, for the past few years, the doubling time has retuned to about 12 months. Having to follow Moore's law for the past four decades forced the leading-edge companies to manufacture devices with feature sizes below 100 nm (will be approaching even under 10 nm). As can be expected, with shrinking dimensions we have arrived at a point where the device structures, device concepts, choice of dielectrics, etc., used would have to be reevaluated.

At the heart of the Si revolution, is the metal oxide semiconductor FET, MOSFET. Use of *n*- and *p*-channel varieties in unison is the basis for complementary MOSFET. Integrated circuit fabrication based on MOSFET relies on amorphous, thermally grown SiO_2 as a gate dielectric. The $Si:SiO_2$ system offers several important materials properties (and therefore electrical properties) including a stable thermodynamic $Si:SiO_2$ interface in addition to superb electrical insulation and interfacial bonding properties. In modern CMOS technology, defect charge densities associated with the $Si:SiO_2$ interface are on the order of $10^{10}/cm^2$, mid-gap interface state densities are about $10^{10}/cm^2$ eV, and hard breakdown fields in excess of 10 MV/cm are routinely obtained and are therefore expected regardless of the device dimensions. These outstanding electrical properties clearly present a significant challenge for any alternative gate dielectric candidate.

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With scaling, however, in order to avoid severe short channel effects SiO_2 must be reduced to the point that leakage current becomes unacceptable. Therefore, a replacement for SiO_2 must be found. In more detail, with increasing demand for increased speed and device density, the device dimensions are continually scaled down following what is termed as the Moore's law. However, reduction of gate dimensions, the corner stone of which is the reduction of the gate or the channel length, requires decreasing oxide thickness in order to prevent the short channel effect and or render it manageable. The thinness required by SiO_2 even before the 65 nm node technology (projected to go down to 16 nm by 2016) and lower technology is such that direct tunneling, therefore the undesirable gate leakage current is substantial and increases exponentially with decreasing thickness. This calls for other dielectrics with much higher dielectric constants, thus the term high-κ dielectrics which allow maintenance of the gate oxide capacitance (or the inversion capacitance) needed for reducing short channel effects while still using sufficiently thick oxide layers to prevent current conduction through it. Being such a crucial part of the highly successful CMOS technology naturally paved the way for extensive research and developmental activities to find a replacement for SiO_2. At the very minimum, in addition to compatibility with CMOS processing, the high-κ dielectric must have a large dielectric constant, large band discontinuity for both the conduction and valence bands which means large bandgap and low interface and bulk trap density. In this review, after making the case for a different gate dielectric, brought about by scaling trends, various gate dielectrics that have and or are being explored with their associated technologies will be discussed. Because processing is an integral part of any CMOS development, this issue will be discussed as well. This then will pave the way for a discussion of the techniques used to increase speed performance of CMOS as well as the methods under consideration beyond Si channels and gate dielectric related developments.

In this review paper, at first we concern about the growth issues for the high-κ materials. Then we will focus on the fabrication and processing issues for them. At last the high-κ dielectric materials properties and the integration of the high-κ materials with the MOSFET engineering will be discussed. The second motivation of this review paper is to discuss the channel materials and how to increase the MOSFET running speed. We will discuss the GaAs and Ge channel materials for the replacement of the Si *n*- and *p*-MOS.

2 Scaling and need for high-κ dielectrics

Following a dramatic ride, characterized by exponential growth, spanning over several decades with relentless scaling to ever smaller dimensions for higher packing density, faster circuit speed, and lower power dissipation, CMOS technology has become the dominant technology for very large scale integration (VLSI). These advances led to computers and networks with far superior performance and dramatically reduced cost per function. In fact it can safely be stated that the semiconductor manufacturing is the only one that provides better performance for less with each passing day. As the device dimensions are scaled downward for increased speed and reduced area per device, avoidance of short channel effects dictate that the oxide thickness be reduced. And finally, the industry is encountering fundamental and technological challenges, some fundamental in nature, which it did not face before [2].

Until present, the CMOS circuit experienced scaling with little or no concern about fundamental limits. Accompanying developments included halo-doping of source and drain (1985), which paved the way for scaling of the channel lengths down to $\sim$0.1 μm, the basic device structure and thus physics underlying the operation of the MOSFET has remained substantially unchanged over all these years. Together several factors make further evolutionary change difficult for sub-0.1 μm gate lengths such as lithography, controlling diffusion profiles, and generating sufficiently shallow and low-resistance contacts. However, new limits in fundamental nature are being faced, among which are tunneling through thin oxides and narrow depletion layers, as well as increasing variability in device characteristics caused by random impurities due to much reduced device volume. Among these factors, the gate oxide leakage current is considered the most restrictive. Gate oxide thickness must be reduced as channel length is reduced to avoid short channel effects (simply loss of drain current control by the gate bias and increased effect of drain bias on drain current even in what would otherwise has been the saturation regime). This causes a reduction in the ON/OFF current ratios (i.e. exponentially larger off-state drain currents for a given on-state current). Moreover, reduced oxide thicknesses result in increased gate leakage current which is a formidable problem particularly for large density circuits. In addition to the leakage current, the reverse short channel effect is another point of attention for scaling. Halo doping near the source and drain terminals in a submicron MOSFET serves to reduce the size of the depletion region in the vicinity of these junctions. For short channel lengths the halo doping of the source overlaps with that of the drain, increasing the average channel doping concentration, and thus increasing the threshold voltage. This increased threshold voltage requires a larger gate voltage for channel inversion. The conventional SiO_2 thin gate dielectric cannot withstand the higher gate voltage bias in a submicron MOSFET.

The thinness required by SiO_2 even before the 65 nm node technology (the actual gate length is projected to go

down to 6 nm by 2020) (Fig. 1) and lower technology is such that direct tunneling, therefore the undesired gate leakage (Fig. 2) becomes substantial and increases exponentially with decreasing thickness. This calls for other dielectrics with much higher dielectric constants, thus the term high-κ dielectrics which allow maintenance of the gate oxide capacitance (or the inversion capacitance) needed for reducing short channel effects while still using sufficiently thick oxide layers to prevent current conduction through it (Fig. 3). The benefits of high-κ dielectrics can clearly be gleaned from Eq. 1 where in the equivalent thickness for a certain gate capacitance made of SiO_2 can be increased by a factor of $\left(\varepsilon|_{\text{high}-\kappa}\right)\Big/\left(\varepsilon|_{SiO_2}\right)$. Approximating the dielectric constant of SiO_2 with 4, a 1 nm thick

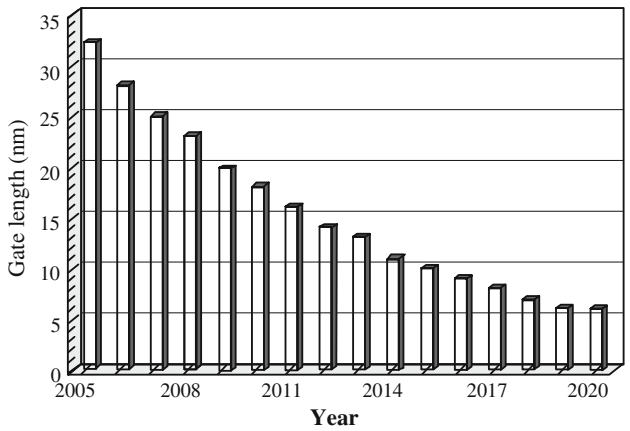

Fig. 1 Gate length (Lg) scaling (data from 2005 and 2020 ITRS) (The International Technology Roadmap for Semiconductors)

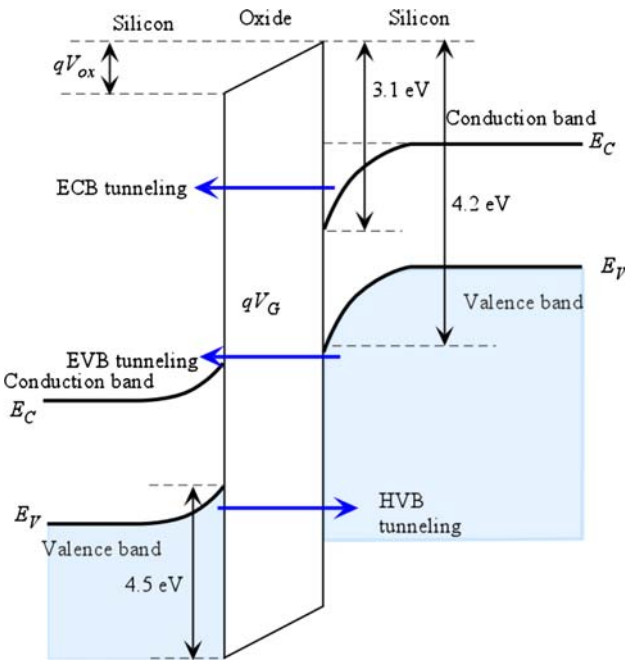

Fig. 2 Details of electron tunneling through the oxide

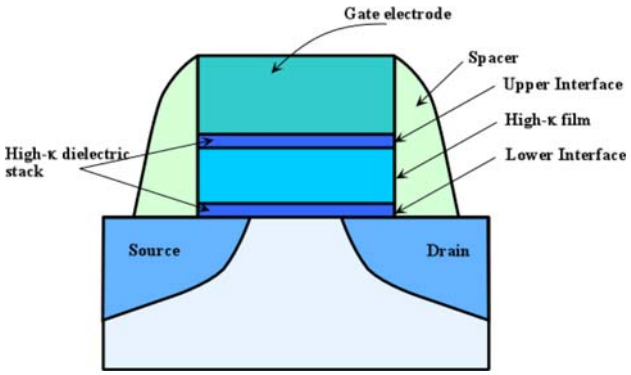

Fig. 3 Simplified cross-section of high-κ gate dielectric stack

SiO_2 gate dielectric (referred to as the equivalent thickness) can be replaced with a 4 nm thick high-κ dielectric with a relative dielectric constant of 16.

$$t|_{\text{eq}} = t|_{SiO_2}\frac{\varepsilon|_{\text{high}-\kappa}}{\varepsilon|_{SiO_2}} = t|_{SiO_2}\frac{\varepsilon|_{\text{high}-\kappa}}{3.9} \quad (1)$$

Finding a material to replace SiO_2 is a more than just a formidable challenge because SiO_2 is nearly a perfect dielectric whose only drawback is the relatively low ε, and it turned out to be the major issue placing a roadblock on the long and successful saga of SiO_2 dating back to birth of the microelectronics industry based on Si. Despite the fact that there are many dielectrics with much higher dielectrics constant ε (20–100) at present than that of SiO_2 it is a formidable task to replace SiO_2 because of such issues as lower channel-dielectric interface quality, reliability, high leakage current. To reiterate the main criteria for a gate dielectric include band offsets that block hot charge carriers, chemical stability in contact with both the silicon substrate and the gate material, and low density of interface and bulk states. Attempts to introduce high-κ dielectrics into CMOS technology began as early as 70–80s, but was delayed because of their high defect concentrations, particularly O vacancies, which resulted in charge trapping, transient threshold voltage shifts, and a degradation of Si carrier mobility due to Coulombic scattering. There have been several excellent review papers on different aspects of high-κ dielectrics [3, 4] but the field is progressing very rapidly and is on the verge of converging on a successful replacement for SiO_2. De Almeida and Baumvol [4] analyzed in details reaction and diffusion properties of dielectric/gate and dielectric/channel interface. Wilk et al. [3] reviewed the status of the of the high-κ dielectric studies, vista 2000, which was followed by a similar review by Wallace and Wilk [5], vista 2003, with some updates. Since this area of research is studied very intensively, for past few years a great number of publications on high-κ dielectrics appeared, which warrants a reexamination of the

field at least succinctly. In deference to what has already been reported, the focus of the present discussion will be on the very recent progress.

HfO_2 and ZrO_2 high-κ dielectric oxides have received greater interest, commensurate with a large number of reports which has been made devoted to these materials. Also an old timer, Ge, has gained increased attention as a channel material for high mobility FET devices, due to higher low-field intrinsic carrier mobility than that of silicon. Thus, this semiconductor has been the focus of research for many groups and it was used as a substrate for high-κ dielectric growth, therefore, problems facing these materials as a channel layer for high-κ dielectrics in the context of MOSFETs will be discussed in this section. Also the issues related to the passivation and etching of high-κ dielectrics will be discussed.

There are different requirements for DRAMs and metal–oxide–semiconductor field-effect transistor (MOSFET) applications. This then follows that depending on the aim there are different requirements for the dielectric layers to be grown as well. For example, memory capacitors require low leakage current and high capacitance density (per unit area) for charge storage, but the interface quality is not as critical as the switching device. Some level of control of the interface is required primarily to limit interfacial reactions to keep the total capacitance high. Since the main purpose of the capacitor is to store charge, current transport along the interface is not critically important. Also no electric field penetration is required below the bottom electrode. Thus, the key parameters to optimize for DRAMs applications are the leakage current and the dielectric constant, making the main the purpose is to obtain films with dielectric constant (high-κ) and low leakage current. In contrast, the main requirement of a MOSFET device is that electric field penetrates into the Si channel to modulate carrier transport, and therefore, the quality of the dielectric-channel interface must be very high.

The dielectric layer should be uniform in crystalline structure and in physical properties. For this reason the dielectric layer should be either amorphous or *extremely high quality single* crystalline. All SiO_2 dielectric layers used in SiO_2/Si based MOSFET and DRAM technologies today are in the amorphous state. There are a number of factors which favor amorphous layers: (i) there is only a single amorphous structure for a given composition that implies uniform physical properties; (ii) there are no dislocations or grain boundaries; (iii) stress can be eliminated by moderate topological variations in a random network rather than through misfit dislocations; (iv) a continuous random network tends to minimize electrically active defects. For these reasons less than simply perfect crystallization is an undesirable feature since it introduces non-uniformities in the scale of grain size. Polycrystalline dielectrics have non-uniform leakage distribution and can give rise to large statistical variations for nanometer sized device across the chip. Because the grain boundaries in crystallized gate dielectrics can serve as pathways for Si, oxygen and or dopant diffusion in or out of the gate the gate dielectric, whichever is applicable, and even to the channel region in the silicon bulk, it is imperative that they be reduced and if not totally eliminated.

There are a number of high-κ dielectrics, which have been and or are actively being pursued for replacing SiO_2. A list of dielectrics and their physical properties such as the dielectric constant, band gap, conduction band offsets relative to Si and Ge, and crystal structures is tabulated in Table 1. Beyond silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), a number of high-κ dielectric candidates such as gadolinium oxide (Gd_2O_3) [6], magnesium oxide (MgO) [7], erbium oxide (Er_2O_3) [8], neodymium oxide (Nd_2O_3) [9] praseodymium oxide PrO_2 [10], cerium oxide (CeO_2) [11, 12], aluminum oxide (Al_2O_3), lanthanum aluminum oxide ($LaAlO_3$), La_2O_3 (lanthanum oxide) [13, 14], yttrium oxide (Y_2O_3) [15], tantalum pentoxide (TaO_5) [16, 17], titanium dioxide (TiO_2) [18], zirconium dioxide (ZrO_2) [19], zirconium silicate ($ZrSiO_4$) [20], hafnium oxide (HfO_2) [21, 22] hafnium silicate ($HfSiO_4$) [23], dysprosium oxide (Dy_2O_3), strontium titanate ($SrTiO_3$), etc. have been proposed and investigated with HfO_2 getting special attention.

To be amenable to commercial production, high-κ materials for both capacitors and transistors must simultaneously satisfy a set of requirements such as low leakage current, large band offsets with Si, chemical and thermal stability, and low density of interface states. The TiO_2 and Ta_2O_5 systems have been heavily studied for high-κ applications owing to their high permittivity of $\kappa = 30$–110, depending on the crystal structure and method of deposition. However, these dielectrics suffer from such ailments as high leakage current and relatively poor chemical stability. Among the above mentioned potential candidates to replace SiO_2 as the gate dielectric, hafnium dioxide (HfO_2) and somewhat early on zirconium dioxide (ZrO_2) were found to be the most promising combining high dielectric permittivity and thermal stability with low leakage current due to a reasonably high barrier height that limits electron tunneling. Various pertinent properties of the abovementioned oxides are also tabulated in Table 1 with a graphical representation of the known band alignment between Si and various high-κ dielectrics shown in Fig. 4. Currently HfO_2 is under intensive investigations with the emphasis being placed on interface states, gate compatibility, structural, physical and chemical stability at both the gate electrode/dielectric and dielectric/channel interfaces, and process compatibility.

Table 1 Some physical parameters of high-κ dielectrics and heterostructures with Si and Ge

Material	Dielectric constant (k)	Band gap E_G (eV)	Band offset ΔE_C (eV) to Si	Band offset ΔE_C (eV) to Ge	Crystal structure
SiO_2	3.9	8.9	3.2		Amorphous
Al_2O_3	9	8.7	2.8	2.6 [24]	Amorphous
Si_3N_4					Amorphous
TiO_2	80–100	3.5	1.2		Tetragonal
Ta_2O_5	26	4.5	1–1.5		Orthorhombic
HfO_2	25	5.7	1.4	2.0 ± 0.1 [25]	Monoclinic, tetragonal, cubic
ZrO_2	25	7.8	1.5		Monoclinic, tetragonal, cubic
La_2O_3	30	4.3	2.3	2.56 [24]	Hexagonal, cubic
Y_2O_3	15	5.6	2.3	2.56 [24]	Cubic
Gd_2O_3	24 ± 2 [6]			2.44 [24]	
MgO	9.8 [7]	7.3 [7]			Cubic
Er_2O_3	14.4 [8]	7.5 [8]	3.5 [8]		
Nd_2O_3		5.8 [9]	2.2 [9]		
PrO_2	25 [10]	3–4 [10]	>1 [10]		Cubic
CeO_2	52 [11], 26 [12]	4.5 [12]			
$LaAlO_3$	26 [13]	6.0 [10]		2.2 [24]	
$ZrSiO_4$					Amorphous
$HfSiO_4$				2.2 [24]	Amorphous
(Dy_2O_3)	14	4.8			

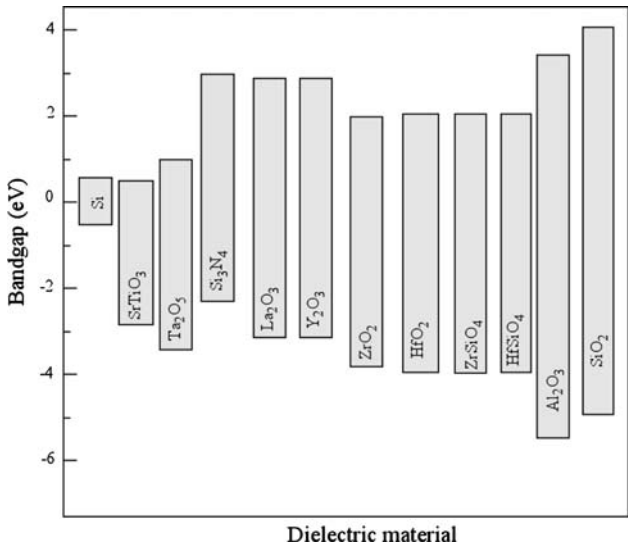

Fig. 4 Bandgaps and the bandgap discontinuities between various high-κ dielectric materials and Si along with the well known SiO_2 and Si_3N_4

3 High-κ dielectric layer growth

Because gate oxide is the most critical component of a MOSFET, extremely reliable high-quality high-κ gate dielectric thin films are imperative. For this reason gate oxide film growth of the films is a very important issue and as such received considerable attention. Several thin film growth techniques such as reactive thermal evaporation [26], atomic layer deposition (ALD) [27, 28], chemical vapor deposition (CVD) [29, 30], pulsed-laser deposition (PLD) [31], and molecular beam-epitaxy (MBE) [32, 33] have all been employed in many efforts to obtain high-quality high-κ dielectric thin films. The properties of the thin films so produced have been reported to be closely dependent on the growth method. Studies to glean an understanding of any correlation amongst the properties of the films, the interfacial layers, and growth conditions have been undertaken. Let us now discuss the deposition methodologies applied to high-κ dielectrics. Below a succinct review of the above mentioned deposition techniques to high-κ material is given.

3.1 Atomic layer deposition (ALD)

The atomic layer deposition (ALD) is one of the methods for preparing ultra thin metal-oxide layers with excellent electrical characteristics and near-perfect films because of the layer-by-layer nature of the deposition kinetics. An ideal ALD process proceeds as a self-limiting mechanism. The growth surface becomes saturated with the governing precursor so that the deposition automatically self-limits at one or two monolayers. ALD is carried out by the surface exchange reactions between the chemisorbed metal-containing precursor fragments and adsorbed nucleophilic reactant molecules. Therefore, the growth rate is

independent of the precursor dose but surface-controlled. The ALD mechanism involves a full cycle [34], and one cycle consists of four steps, namely supplying the first and second precursor gases to the surface repeatedly and alternatively until a film of desired thickness is obtained, as shown in Fig. 5. In this 4-step ALD process, the substrate surface is first exposed to a pulse of the first precursor and the chemical absorption of the first precursor is allowed to take place on the substrate surface. Then, an inert gas is allowed into the growth chamber to remove the remaining and un-reacted precursors. Thirdly, the second precursor is introduced into the chamber and allowed to react with the precursor absorbed on the substrate surface. A complete atomic layer deposition takes place during this step. Lastly, the inert gas is allowed into the growth chamber again to expel the gaseous reaction by-products and un-reacted precursors.

Similar to other CVD processes, there are many key factors with which one must be concerned and must optimize. Suntola et al. [35] introduced the concept of "ALD-window" to indicate the temperature range where thin film growth proceeds by surface control in an ALD-mode, just as shown Fig. 6. Outside the ALD-window, the growth is

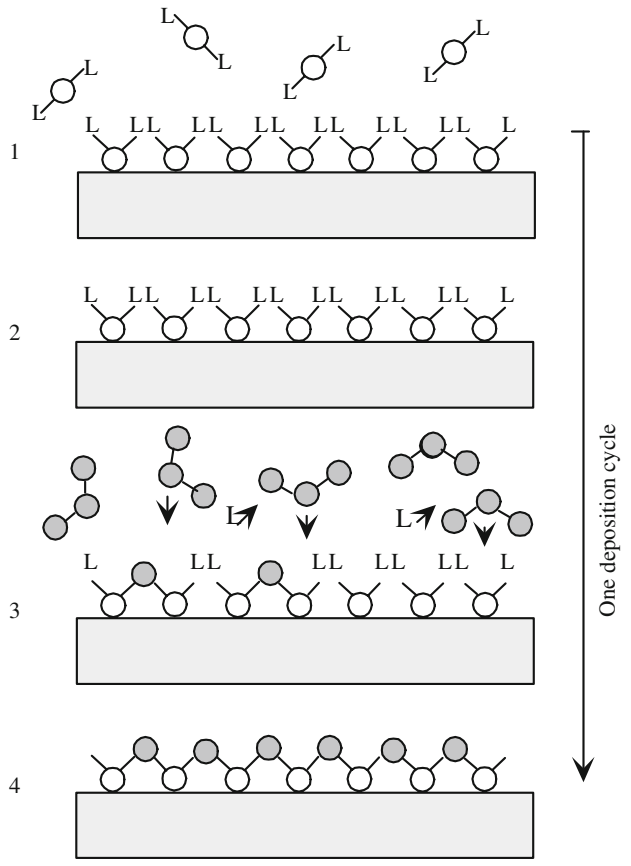

Fig. 5 Schematic illustration of an ALD growth cycle (1–4) leading to the formation of an imaginary binary oxide film of metal (*white circle*) and oxygen (*gray circle*). L refers to the precursor ligand [34]

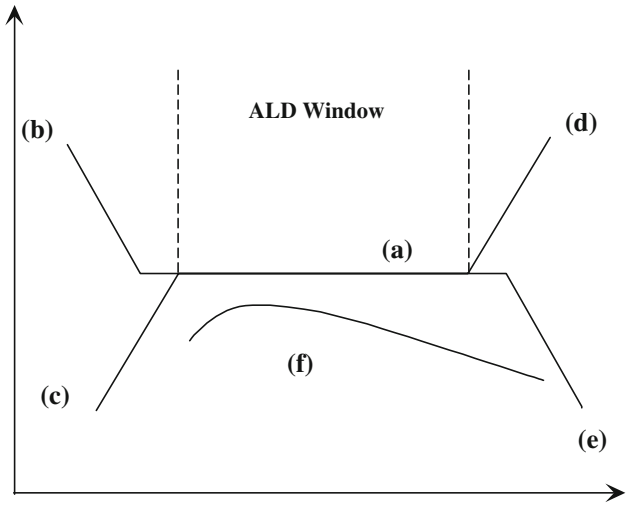

Fig. 6 Scheme of (a) an ALD processing window limited by (b) precursor condensation, (c) insufficient reactivity, (d) precursor decomposition and (e) precursor desorption. If the deposition rate is dependent on the number of available reactive sites as in (f), actual ALD window cannot be observed [34]

limited by precursor condensation, decomposition, and insufficient reactivity.

As mentioned above, in this so-called surface-controlled ALD mechanism, the growth rate is independent of the precursor pulse length (dose). The only requirement is that there are sufficient precursor molecules (more is fine) to satisfy the adsorption sites on the surface. The excess and un-reacted precursors are then blown away by inert gas purging. However, many of the recently used organometallic precursors for oxide films do not exhibit a distinct ALD window. Thus, the deposition rate in these processes is dependent on the temperature, while the self-limiting feature of the ALD processes remains. Furthermore, this method is known to have a relatively high concentration of residual impurities due to the use of precursors and thus is unfavorable to the quality of the gate dielectric. From this point of view, we can see that the choice of the precursor is very pivotal in improving the crystal quality of ALD grown films.

Many varieties of precursors have been used for the high-κ dielectric material deposition in an attempt to find the optimal growth window for each of the various oxide materials and reduce the by-product contamination. In the case of the most popularly studied high-κ oxides, ZrO_2 and HfO_2, halide, metal alkoxide, and alkylamide precursors have been widely used for the ALD growth. For instance, the halide precursors $ZrCl_4$ [36], ZrI_4 [37], $HfCl_4$ and HfI_4 [37] have been used for the crystalline ZrO_2 and HfO_2 film deposition by ALD. Aarik et al. [38] used $HfCl_4$ and H_2O as the precursors and found that the layer-by-layer growth is self-limiting at temperatures above 180 °C. By using the same precursor, Cho et al. [39] found that the film

thicknesses decreased with increasing deposition time after reaching a certain maximum value at 300 °C and 400 °C due to the enhanced dissolution of SiO_x into the growing films at these temperatures.

Kukli et al. [40] used the alkoxide complex $[Hf(mmp)_4]$ and H_2O precursor to deposit HfO_2 on borosilicate glass and Si(100) substrates by ALD in the temperature range of 275–425 °C. It was shown that the adsorption of hafnium complex was not entirely self-limiting, probably because of the thermal decomposition of the precursors. Crystalline films containing the monoclinic HfO_2 phase were grown at temperatures exceeding 300–325 °C. The C–V curves of the as-deposited films (Fig. 7) showed a clockwise hysteresis due to the presence of positive mobile charge in the films. The voltage shift is in the range of 0.5–1 V. The effective permittivities of the dielectrics in $Al/HfO_2/Si$ structures varied between 12 and 17. The refractive index measurement shows a value about 1.8–2.0, which is less than the value (2.0–2.2) obtained from the samples deposited by using the $HfCl_4$ precursor. This means that the alkoxide complex $[Hf(mmp)_4]$ precursor led to less dense films than those grown from $HfCl_4$.

Lee et al. [41] obtained HfO_2–Al_2O_3 films with EOT 22.5 Å and low leakage current (1.0 fA/cell at 1.65 V) by using the liquid alkylamide complex $[Hf(NMeEt)_4]$ precursors. Additionally, the $HfCl_4$ precursor also has been tried and compared with the $[Hf(NMeEt)_4]$ precursor. Compared with the $HfCl_4$ precursor, the ALD grown HfO_2 dielectric films have better step coverage and higher throughput. Relying on these results, those authors stated that the $HfCl_4$ precursor has two major drawbacks. The first one is the poor step coverage. The second one is that the saturation time of the self-limiting reaction for $HfCl_4$ which is directly proportional to the process time is longer than that of the $[Hf(NMeEt)_4]$ precursor.

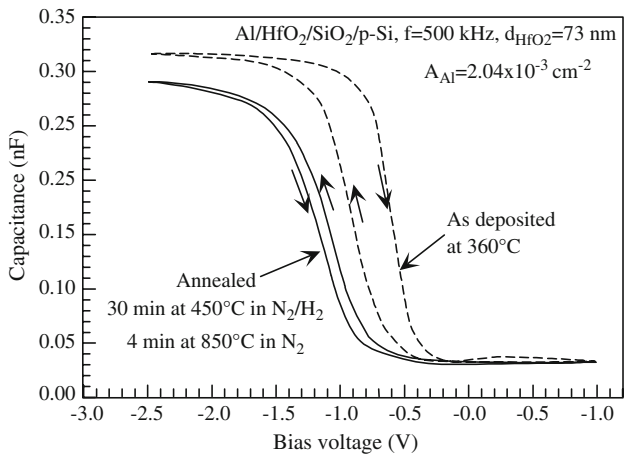

Fig. 7 Capacitance–voltage and dissipation curves measured for $Al/HfO_2/SiO_2/p$-Si(100) deposited by ALD using $[Hf(mmp)_4]$ and H_2O precursor with capacitor at AC signal frequency of 500 kHz [40]

Amorphous praseodymium oxide (PrO_2) films have been explored as well for gate oxides. Kukli et al. [42] have grown the PrO_2 amorphous films on Si (100) substrates in the temperature range 200–400 °C by using $Pr[N(SiMe_3)_2]_3$ belonging to the trigonal-bipyramidal coordinated lanthanide (III) system and H_2O as the precursor. Crystallization was attained after annealing at 900–1000 °C, and X-ray diffraction data indicated that the composition of the films was $Pr_{9.33}(SiO_4)_6O_2$. In addition, the films were found to contain considerable amounts of residual hydrogen and residual or diffused silicon. The effective permittivity of 70–100 nm thick films was in the range of 14–16. Annealing at 800 °C in nitrogen increased the effective permittivity slightly to 15.6–21 and decreased the rechargeable trap density. It is evident in Fig. 8 that annealing at 800 °C caused the capacitance to increase and the hysteresis voltage shift decrease. There are two reasons for the reduction in capacitance. Firstly, after annealing a SiO_2 interfacial layer is formed. Secondly, the Si atoms diffuse into the metal oxide followed by the oxidation of the diffused Si. The differences in the electrical properties after nitrogen and air (oxygen-assisted) annealing could be attributed to the differences in the microstructure formation. Wakiya et al. [43] suggested that for slightly oxygen-deficient PrO_2 the annealing atmosphere caused different phase transitions. In nitrogen ambient, the C-type rare earth structure was detected between 700 °C and 1000 °C before the decomposition of the defect fluorite into the A-type rare earth structure. In oxygen ambient, however, such a transition was not detected.

We have so far discussed the ALD deposition of the HfO_2, ZrO_2 and PrO_2 with aid of precursors. The critical issue for improving the oxide quality seems to center

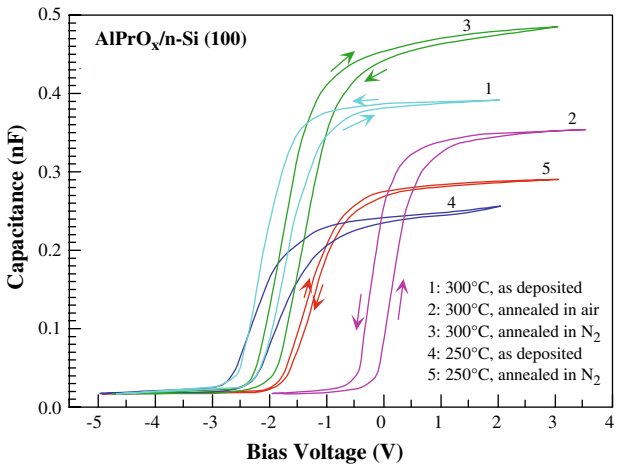

Fig. 8 Capacitance–voltage curves of $Al/PrO_x/Si$ capacitors based on 100 and 78 nm thick PrO_x films grown on HF etched Si(100) at 250 and 300 °C, respectively, in as-deposited and annealing states. Labels denote the growth temperature and annealing ambient. Annealing was carried out at 800 °C for 1 min in N_2 and 3–4 min in air [42]

around the choice of precursors with lower contamination and ability to self-limit. In addition to HfO_2, ZrO_2 and PrO_2, other oxide films prepared by ALD deposition and various precursors have been reported. The details for them will not be discussed here due to space limitation. However, those oxides along with the precursors used for their growth are listed in Table 2.

3.2 Pulsed-laser deposition (PLD)

The pulsed-laser deposition (PLD) method is also increasingly being utilized to prepare a wide variety of high-κ dielectric materials in thin-film form owing to its simplicity and fast deposition rate [31]. More importantly, PLD is known for the quality of the layers grown at relatively low substrate temperatures among the thin-film deposition methods. Ratzke et al. [49] applied PLD to deposit the thin films of high-κ praseodymium oxide (PrO_y) and hafnium oxide (HfO_x) on Si substrates using the third harmonic of a Nd:YAG laser for ablation. In this investigation, the two oxide materials were compared with their morphology, chemical composition, and crystalline structure, in particular that at the interface, in mind. The effect of the deposition temperature was also investigated. Both oxide films were observed to exhibit a grainy structure when deposited at substrate temperatures below 750 °C with the grain size increasing from 40 nm at room temperature to about 100 nm at 750 °C. The PrO_y films were noted to be much more uniform than HfO_2. HfO_2 showed increasingly larger holes which penetrated several nanometers into the silicon substrate. In addition, the interface was noted as being significantly different for both materials; a silicate formation for PrO_y and a rich abundance of SiO_2 and a silicide for HfO_2.

Desbiens and El Khakani [50, 51] have grown high-κ silicon oxynitride (SiO_xN_y) thin films by using a hybrid deposition process. Those authors combined the PLD plume of silicon species in an oxygen background with a remote plasma-based atomic nitrogen source (ANS) to complete the growth to help increase nitrogen incorporation into the SiO_xN_y films. At the highest N content (35%), the films exhibited a high-κ value of about 9.5 and a breakdown field as high as 19 MV/cm. The Poole–Frenkel emission with compensation was noted to dominate the conduction mechanism in the SiO_xN_y films, which typically leads to current leakage. It was noted that the dielectric

Table 2 Oxides other than HfO_2, ZrO_2 and PrO_2 prepared by ALE along with the metal precursors, O source, and deposition temperature used

Material	Metal precursor	Oxygen source	Deposition temperature (°C)	Relative dielectric constant
Sc_2O_3	$Sc(thd)_3$	O_3	335–375	13 [44]
	$(C_5H_5)_3Sc$	H_2O	250–350	
Y_2O_3	$Y(thd)_3$	O_3	250–375	9–14 [45]
	$Y(thd)_3phen$	O_3	250–375	
	$Y(thd)_3bipy$	O_3	250–375	
	$(C_5H_5)_3Y$	H_2O	200–350	
	$(C_5H_4CH_3)Y$	H_2O	200–400	
La_2O_3	$La(thd)_3$	O_3	225–275	
	$La[iPrNC(CH_3)NiPr]_3$	H_2O	300	
CeO_2	$Ce(thd)_4$	O_3	175–250	26 [46]
	$Ce(thd)_3phen$	O_3	225–275	
Nd_2O_3	$Nd(thd)_3$	O_3	310	10.4 [47]
Sm_2O_3	$Sm(thd)_3$	O_3	300	10 [47]
Eu_2O_3	$Eu(thd)_3$	O_3	300	11.1 [47]
Gd_2O_3	$Gd(thd)_3$	O_3	300	8.9 [47]
Dy_2O_3	$Dy(thd)_3$	O_3	300	8.4 [47]
Ho_2O_3	$Ho(thd)_3$	O_3	300	9.9 [47]
Er_2O_3	$Er(thd)_3$	O_3	250–375	10 [47]
Tm_2O_3	$Tm(thd)_3$	O_3	300	9.4 [47]
$LaAlO_3$	$La(thd)_3 + Al(acac)_3$	O_3	350–375	
$LaGaO_3$	$La(thd)_3 + Ga(acac)_3$	O_3	350–390	25 [48]
$LaMnO_3$	$La(thd)_3 + Mn(thd)_3$	O_3	250–300	
$LaCoO_3$	$La(thd)_3 + Co(thd)_2$	O_3	350	
$LaNiO_3$	$La(thd)_3 + Ni(thd)_2$	O_3	215–250	

properties of the SiO_xN_y thin films could be improved by adding more N, which increases the Si–N bond in the films.

Zirconium silicate films on *n*-Si (100) substrates with EOT = 1.65 nm have been achieved by using the PLD [52]. After a rapid thermal annealing (RTA) in N_2 at 800 °C, the films remained amorphous. However, the amorphous Zr silicate crystallized at 830 °C and the 900 °C RTA led to the phase separation.

Kitai et al. [53] deposited several lanthanoid oxide thin films such as those of PrO_x, Sm_2O_3, Tb_4O_7, Er_2O_3 and Yb_2O_3 on Si(100) wafers by PLD. PrO_x film showed thinner (EOT) and lower leakage current. A PrO_x thin films with EOT of 4.4 nm prepared at room temperature in high vacuum showed only slight growth of the interfacial layer, with a large hysteresis. After annealing at 600 °C, the leakage current and the hysteresis improved. An EOT of 2.6 nm and a leakage current density of 2×10^{-3} A/cm^2 at −1 V were achieved after a 600 °C annealing step.

3.3 CVD growth

Metal orgranic chemical vapor deposition (MOCVD), which is distinguished from CVD by the organometallic sources used, has been widely used in the epitaxy of semiconductor materials and their heterostructures. Especially, in the III–V compound semiconductor materials system, MOCVD is the most widely used equipment for production. Recently, as the high-κ dielectric materials came under intense investigations, MOCVD became a good candidate for the high-κ material deposition on Si substrates. However, what is different from the deposition of the III–V compound semiconductor materials is that many oxide precursors used for the high-κ materials by MOCVD deposition have low pressure and low thermal stability, both of which are detrimental to growth. Therefore, it is necessary to modify a standard MOCVD system to allow e.g. liquid injection where the precursors are dissolved in a solvent, for this technique to be applied fully to high-κ dielectric deposition. Even then, there remain some requirements for the precursors to meet. The precursors must be soluble and stable in the same liquid solution, but they must also not react with each other in the same solution. In addition, it would be convenient for the precursors to have nearly the same vapor pressure at conveniently attained temperatures to avoid multiple refrigeration/heating units that house the precursor sources. To fulfill the all the aforementioned requirements places sever restrictions in the choice of precursors. Below we discuss a few of the reports dealing with the MOCVD deposition of high-κ dielectrics by using different precursors for different oxide layers.

Van Elshocht et al. [54] investigated the effect of MOCVD growth temperature on the physical properties of the HfO_2 layers deposited by MOCVD. The organic precursor, tetrakis-diethylamidohafnium (TDEAH), and O_2 was used for the MOCVD deposition on Si (100) wafers. From the total thickness measurement of the HfO_2 layers, those authors found that the growth rate is dependent on the growth temperature. The deposition rates for the samples processed at 485 °C and 600 °C are almost identical, but less than the growth rate attained at 300 °C. From the RBS data it was found that the Hf atoms in these three samples are quasi identical, which means that the deposition at lower temperatures results in layers with a lower density. In Fig. 9, the densities of different samples deposited at different temperatures are shown. Clearly the density increases with increasing layer thickness and is distinctly lower for layers deposited at 300 °C. The difference in the layer density, caused by the growth temperature, naturally has an effect on the electrical performance of the HfO_2 layers. For example, the leakage current density was observed to be much higher for layers that are deposited at 300 °C as compared to layers deposited at 485 or 600 °C (Fig. 10), which yields functional MOS capacitors (EOT = 1.8–2.0 nm). Hence, a low density HfO_2 layer appears to result in an increased gate leakage current.

Marshall et al. [55] used the alkoxide precursors to deposit hafnium aluminate thin films by the liquid injection MOCVD method. The experiments showed high purity films without any detectable amount of carbon. The $(HfO_2)_x(Al_2O_3)_{1-x}$ films showed a structural transition from crystalline to amorphous when the gas-phase concentration of Al precursor was raised from 4% to 7%. While on the topic of liquid injection MOCVD, $ZrSi_xO_y$ and $HfSi_xO_y$ have been deposited by this method using the liquid precursors tetrakis(diethylamido)zirconium [$Zr(NEt_2)_3$] [56] (for ZrO_2 deposition using this precursor, see [57] or tetrakis(diethylamido)hafnium [$Hf(NEt_2)_4$] [58] (NEt_2 is $N(C_2H_5)_2$).

Titanium oxide (TiO_2) high-κ dielectric layers have also been deposited on the $Si_{0.3}Ge_{0.7}$ substrates by plasma

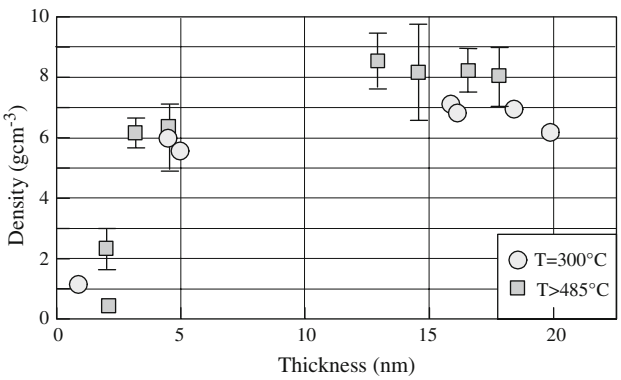

Fig. 9 Density (g/cm^3) as function of the HfO_2 thickness for layers deposited at 300°C (*circle*) vs. 485 or 600 °C (*square*) [54]

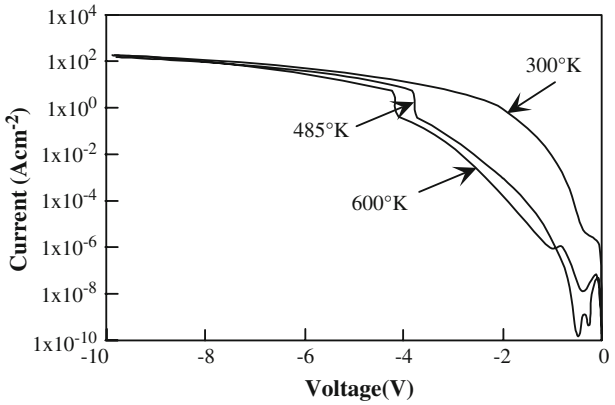

Fig. 10 I–V curves for HfO_2-based gate stacks deposited at 300, 485, and 600 °C [54]

enhanced chemical vapor deposition (PECVD) at low temperatures (150 °C). The effects of annealing in pure nitrogen ambient on the electrical properties of the TiO_2 films were studied by Chakraborty et al. [59] The annealing step was performed in the temperature range of 400–600 °C. Good electrical performance for the gate dielectrics was observed for the dielectric films annealed up to 500 °C in terms of the interface state density, leakage current, and charge trapping properties. Annealing at 600 °C was found to degrade the electrical properties due to Ge segregation and subsequent diffusion into the TiO_2 layer.

3.4 MBE growth

Molecular beam epitaxy (MBE) is a very powerful and sophisticated technique, which can precisely control the film growth parameters at the atomic scale and as such it provides uniform, high-quality films. However, up to now there have been only a few publications regarding the MBE growth of ultrathin oxide dielectric films which is to some extent due to the extremely slow growth rate if e.g. the HfO_2 is formed by the reaction of metallic components of oxides and molecular oxygen beams and the relative unfamiliarity of the Si processing personnel with MBE.

Investigations have been carried out in an effort to grow high quality high-κ dielectric films by using a modified MBE system. For example, Lu et al. [60] employed a laser molecular beam epitaxy (LMBE) system to grow amorphous HfO_2 on (100) *n*-type silicon. LMBE has been interested to fabricate the oxide based electronics, which combines the merits of both PLD and conventional MBE for depositing films with atomic scale thickness control. First a hafnium metal layer was deposited onto the Si substrate in an ultrahigh vacuum of 8×10^{-9} Torr at 200 °C, then the substrate temperature was raised to 500 °C, and the HfO_2 film was deposited onto the Hf layer in Ar/O_2 ambient. After growth, a post deposition anneal was carried out at 500 °C for 30 s in N_2 gas with residual O_2 to oxidize the Hf metal layer by the O ions penetrating during annealing. It was found that the growth of the interfacial layer depends strongly on the oxygen partial pressure in the deposition process. The HRTEM images show the as-deposited Hf layers have good interface quality on Si substrates. The interface between the amorphous HfO_2 and Si still remains smooth even after the annealing step. From the I–V measurements, it can be seen that the sample with 15 nm HfO_2 film shows the leakage current density of 1.5×10^{-2} A/cm^2 at 1 V, which is at least 4 orders of magnitude lower than that of SiO_2 with the same equivalent thickness of 1.3 nm.

Hong et al. [61] deposited the HfO_2 dielectric layer on *p*-type Si (100) substrate by using a variant of MBE, the metalorganic molecular beam epitaxy (MOMBE), with hafnium tetrabutoxide $Hf(O{\cdot}t\text{-}C_4H_9)_4$ as the Hf precursor. It was found that the dielectric constant of the HfO_2 layer increases with the oxygen flow rate during deposition. However, the excess oxygen flow also increases the density of trapped charges. I–V measurements indicate leakage current densities of $2.5–2.7 \times 10^{-2}$ A cm^{-2} at -1.5 V gate voltage. The monoclinic phase of HfO_2 crystal structure was found to be dominant with a dielectric constant κ of approximately 13–16 and the equivalent oxide thickness (EOT) of approximately around 43–52 Å. Vellianitis et al. [62] investigated the lanthanum-based high-κ gate dielectric epitaxy by MBE. The perovskite-like $LaAlO_3$ (LAO) and pyrochlore $La_2Hf_2O_7$ (LHO) were grown on the rapid thermal SiO_2 (RTO)/Si substrates. The LHO and LAO films were deposited at 550 and 400 °C, respectively. Then, Hf and Al were deposited by an electron beam gun and a high temperature effusion cell with a Ta crucible was used for La deposition. The oxide was formed during metal co-evaporation by exposing the substrate to atomic oxygen beams produced by an RF plasma source. The reactive oxygen atoms promote oxidation and prevent the formation of silicides or silicates. The dielectric permittivity of was estimated to be 14.2 and 18.1 for the LAO and LHO, respectively. The leakage current for the LAO with the EOT of 1.1 nm is only 2×10^{-3} A/cm^2 at 1 V gate bias and that of the LHO with the EOT of 1.14 nm is only 4×10^{-5} A/cm^2 at 1 V gate bias.

Kwo et al. [15] attempted to achieve amorphous and crystalline Gd_2O_3 and Y_2O_3 high-κ dielectric materials by MBE. The crystalline Gd_2O_3 and Y_2O_3 films are grown in the (110)-oriented Mn_2O_3 structure of two-fold symmetry on (100) Si. This two-fold degeneracy was effectively removed by using the vicinal (001) Si substrates with 4° misorientation along $[1\bar{1}0]$. The misorientation surface exposes surface steps of double atomic layers, thus giving monodomain Si steps with a spacing of approximately 80 Å for nucleating the (110) Gd_2O_3 single variety. The

film is predominantly oriented in one type of domain, with $[001]_{Gd_2O_3}$ parallel to the step edges $[110]_{Si}$. Along the perpendicular direction, $[1\bar{1}0]_{Gd_2O_3}$ is parallel to $[1\bar{1}0]_{Si}$. The amorphous Gd_2O_3 and Y_2O_3 films are grown on the standard (001) Si substrates. It was found that the amorphous Gd_2O_3 and Y_2O_3 films with smoother morphology have lower electrical leakage than the crystalline films. The grain boundaries in the crystalline films form the conduction path as the major leakage origin [63]. An amorphous Y_2O_3 film with the thickness of 45 Å ($\kappa = 18$) shows the leakage current as low as 10^{-6} A/cm^2 at 1 V gate bias with the EOT of 10 Å. Furthermore, after the forming gas anneal at 400 °C, the leakage current can be reduced again by an order of magnitude, which is about five orders of magnitude better than the best data obtained from a SiO_2 gate dielectric 15 Å. From the leakage and high-κ nature, it would appear that Y_2O_3 could replace SiO_2. Without the SiO_2 at the dielectric/Si interface, there is not such kind of low κ layer problems encountered in the HfO_2 and ZrO_2 films caused by the Si diffusion into the oxide layer. At last the amorphous Gd_2O_3 and Y_2O_3 remains stable without the dielectric property degradation after 850 °C anneal [64]. In addition to the above mentioned dielectrics, lanthanum-based high-κ gate dielectric epitaxy by MBE has also been reported [65]. The perovskite-like $LaAlO_3$ (LAO) and pyrochlore $La_2Hf_2O_7$ (LHO) were grown on the rapid thermal SiO_2 (RTO)/Si substrates. The dielectric permittivity was estimated to be 14.2 and 18.1 for the LAO and LHO, respectively. The leakage current for the LAO with the EOT of 1.1 nm is 2×10^{-3} A/cm^2 at 1 V gate bias and that of the LHO with the EOT of 1.14 nm is 4×10^{-5} A/cm^2 at 1 V gate bias.

4 High-κ dielectric processing

The treatment of high-κ dielectric processing is incomplete without consideration of the processes used in Si MOSFET production. The obvious requirements are for the high-κ materials to be chemically stable, unreactive and show no, or next to none, degradation during MOSFET processing after the high-κ is deposited. It is for this reason alone high-κ material development is synonymous with Si MOSFET processing. High-κ dielectric materials processing is an important issue for the integration of these materials with the conventional Si MOSFET technology and their application on the Si MOS scaling engineering. In addition, the optimization of the processing is necessary to improve the oxide layer quality and reliability, and reduce the gate leakage. As in the case of any gate oxide, the gate leakage is one of the overriding issues. Impurity atoms are added to the dielectrics to reduce leakage current as well as making them more compatible with CMOS processing.

N incorporation is a widely practiced technique to reduce the leakage current [66] in SiO_2. To follow suite N incorporation into high-κ dielectrics has been intensively studied both experimentally and theoretically, and in the process several useful observations have been made. The suppression of crystallization during high temperature treatment, the reduction of B penetration (from the B doped bulk Si and poly-Si gate, the concentration of which is continually increased to combat short channel effects), and the N-induced increase in the dielectric constant have been reported. Accumulation of nitrogen (N) at the SiO_2/Si interface can improve the hot carrier resistance, and the use of oxynitrides can also suppress boron diffusion from the poly-Si gate to SiO_2. There have been several reports on incorporating nitrogen into the binary metal oxides to increase the crystallization temperature by high-temperature annealing in oxygen free N_2 plasma [67, 68], and NH_3 ambient [69]. However, the high-κ dielectric materials nitrided by NH_3 lead to increased interface trap density and deterioration of the interfacial carrier mobility.

Umezawa et al. [70] investigated the effect of N at the atomic level on the leakage current through HfO_2. It was concluded that N atoms act to reduce the leakage current by coupling favorably with oxygen vacancies (V_O) in HfO_2 and extract electrons from V_O. This results in elevating the V_O energy level because of the change in the charge state in V_O from neutral to positive charge. Consequently, N incorporation removes the electron leakage path mediated by V_O related gap states, by deactivating the V_O related gap states. The detailed diagram for this leakage path elimination mechanism is shown in Fig. 11.

Huang et al. [71] used nitrogen instead of NH_3 and N_2O to control crystallization of gate dielectrics. ZrO_2 thin films in this work were deposited on *n*-type Si (100) wafers using a cathodic arc plasma source in a mixture of oxygen and nitrogen ambient. Introduction of nitrogen into the dielectric layer led to increased crystallization temperature. Moreover, the microstructure of the nitrided ZrO_2 thin films was improved as determined by X-ray diffraction and atomic force microscopy characterization.

Fluorine (F) has been found to be an effective passivant for reducing the trap density in conjunction with the high-κ gate dielectrics. The F atoms substitute for the O vacancies (F_O) in the gate oxides and reduce the charge trap density. For example, F incorporation in the HfSiON gate dielectric through channel implantation can effectively reduce the trap density and lower the threshold voltage (V_{th}) [72]. Comparing with the gate F implantation, the channel implantation can achieve a larger V_{th} shift. After annealing, the implanted F atoms diffuse into the HfSiN layer and slightly suppress the B diffusion into the HfSiN gate stack. The C–V measurements show a positive V_{th} shift with increasing F implant dose and no observable channel mobility degradation occurs

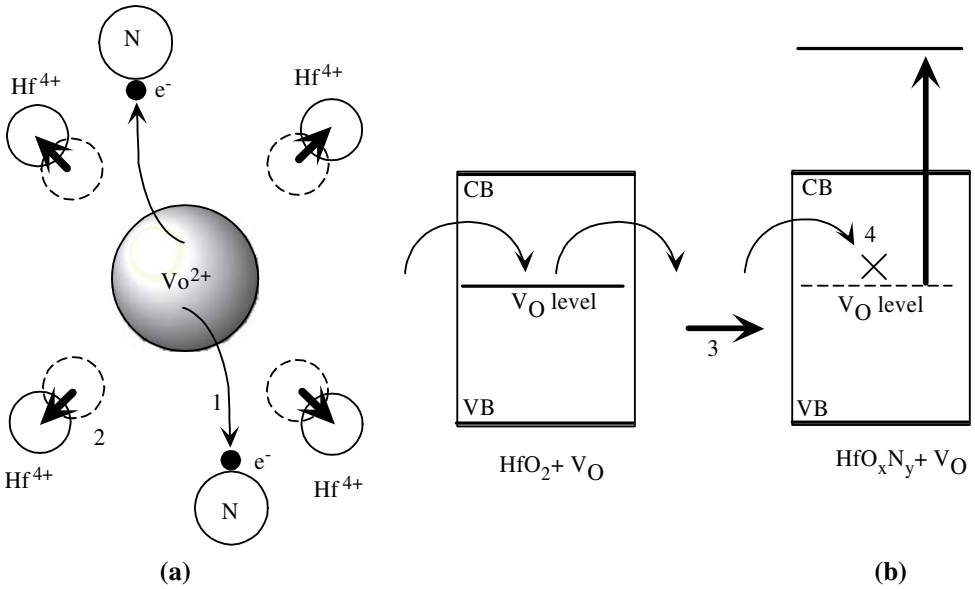

Fig. 11 Schematic illustration of N incorporation effects: (**a**) N-induced atomistic relaxation around V_O. (1) Electron transfer from V_O to N atoms; (2) outward movement of Hf^{4+} ions due to the increase in Hf^{4+}–Hf^{4+} Coulomb repulsion; (**b**) N-induced elimination of leakage paths; (3) drastic V_O level elevation due to the decrease in attractive Coulomb interaction from Hf^{4+} ions around V_O; (4) removal of leakage paths due to the elimination of a V_O level [70]

with F implantation. In addition, F incorporation has been reported to reduce the CV hysteresis and positive charge trapping of the gate stack and improve the device reliability [73, 74]. However, the gate leakage increases due to the EOT reduction caused by F incorporation. It is argued that F is a very good alternative passivant for the gate oxide because it is the only element that is more electronegative than O but with comparable bond length [75]. With F incorporation, the F atoms are bonded to metal ion dangling bonds resulting in annihilation of oxygen vacancies. As discussed above, different atoms such as F, N and O can be incorporated into the high-κ films to improve their properties. To this end, various models for the mechanisms involved have been put forth. Further studies must be undertaken to gain a deeper understanding of the fundamental physics underlying the processes involved.

Alternatively, Al and Si can be incorporated into the high-κ dielectric layer to improve its thermal stability. The pure HfO_2 dielectric layer crystallizes at about 400 °C. However, in the conventional CMOS processing high temperature annealing is frequently used which causes at least partial crystallization of the otherwise amorphous HfO_2 dielectric layer. In order to prevent the crystallization, Al and Si have been added to the HfO_2 dielectric layer. It is found that by adding 31.7% Al, the crystallization temperature of the HfO_2 dielectric layer can be increased by about 400–500 °C above that for pure HfO_2 dielectric [76]. However, this comes at a price in that the Al doped HfAlO dielectric exhibits a lower dielectric constant. Furthermore, addition of Al atoms also introduces negative fixed oxide charge due to Al accumulation at the HfAlO–Si interface, resulting in mobility degradation [77]. The fixed charge acts as scattering centers and degrades the channel carrier transport.

An alternative to Al is adding Si atoms into the dielectric layer instead. With 20% Si, a HfO_2 dielectric layer was found to withstand a 5 s rapid thermal annealing step at 1000 °C without any obvious HfO_2 crystal components in the layer [78]. Structural analysis indicated that the majority of the HfSiO remained amorphous but a small fraction crystallized into the tetragonal or orthorhombic phase. Moreover, HfSiO can fully phase separate into HfO_2 and SiO_2 via spinodal decomposition after 900 °C O_2 RTA treatment [79]. Another point of interest is that during the dielectric layer deposition a thin interlayer of SiO_2 is often formed between the dielectric layers and the Si substrate, which is different from the Si incorporation we discussed above. This kind of SiO_2 layer formation adds a parasitic series capacitance on the gate stack and should be avoided [80].

As discussed above, the incorporation of Al and Si into HfO_2 films suppresses the crystallization and increases the crystallization temperature which is desirable. However, addition of Al and Si causes the dielectric constant of the films to decrease, which is not desirable. To circumvent this, introduction of La and Y into HfO_2 has been studied [81]. By adding La atoms, the crystallization temperature of HfO_2 can be raised to 900 °C, without compromising on the dielectric constant ($\kappa = 20$ can be achieved). Similar to La, Y doping also shows the advantages beyond that which can be obtained with Si and Al doping. With the increase of Y concentration the dielectric constant increases as well. However, the dielectric constant value reaches a peak as a function of Y concentration.

In parallel to developments of high-κ gate dielectrics, fabrication technologies such as appropriate etching must also be developed. The chief requirement is directionality and anisotropy. Among the etching processes, wet etching

is the first choice because of its damage free nature. However, the etching selectivity and rate with this method are of the most concern in addition to etch rate control. It has been reported that the as-grown amorphous dielectric films can be easily etched in a dilute HF (DHF) solution [82]. But the etch rate has been reported to reduce (might be even stagnate) after annealing [83]. By subjecting dielectric film to ion bombardment, the etching rate for the annealed films can be greatly increased, but the caveat is the resultant damage. Saenger et al. [84] attempted to use O_2 plasma to treat the annealed HfO_2 and ZrO_2 samples. After one min and 150 W treatment, the etching time for 2.9 nm HfO_2 film reduced from more than 10 min to 4 s in an HF 10:1 solution. For the dielectric films deposited by different method, the etching solution and etching rate are different. Han et al. [85] reported the recipes for some dielectric materials deposited with different methods which is tabulated in Table 3.

As discussed above, wet etching of the high-κ dielectric materials is very sensitive to the etching conditions and the etching rate is not so controllable as compared to the dry etching processes. As far as the high-κ/Si etching selectivity, the RIE etching has been comprehensively studied and the etching conditions have been optimized. As clearly stated and understood already, it is imperative that the high-κ materials be etched with conventional Si processing methods and equipment.

Etching characteristics of HfO_2 films grown by atomic layer chemical vapor deposition on *p*-Si (100) wafers have been investigated by Sha et al. [86]. A high-density electron cyclotron resonance plasma reactor was used to conduct etching in BCl_3/Cl_2 halogen based chemistry by systematically increasing the BCl_3 percentage from 0% to 95% at 5 mTorr and RF power of 300 W with ion energy of 75 eV. The etch rate as a function of the BCl_3 percentage is shown in Fig. 12. BCl_3 is seen to increase the etch rate significantly reaching a maximum of $\sim$90 Å/min at 40% of BCl_3 before turning downward for higher BCl_3 concentrations and turning back up again. Furthermore, the etch rate of HfO_2 reached a local minimum at a 80% BCl_3 concentration and increased slightly for higher BCl_3 percentages reaching an etch rate of $\sim$50 Å/min for BCl_3 without Cl_2. The decrease in etch rate following the minimum is caused by the reduced density of the dominant ionic species, e.g. BCl and the dominant ion species in BCl_3/Cl_2 plasmas. Addition of BCl_3 in the Cl_2 plasma was also found to improve the etch selectivity of HfO_2/Si from $\sim$0.01 in pure Cl_2 plasma to $\sim$0.9 in pure BCl_3 plasma at ion energy of 75 eV. The etch selectivity was improved to above 4 as the ion energies reduced toward the threshold energy in pure BCl_3 plasma, as shown in Fig. 13. It is argued that the main difference in etching HfO_2 in Cl_2 and BCl_3 plasmas is the oxygen removal from the oxide film by the reducing chemistry of BCl_3. It is difficult for the Cl_2 plasma to remove oxygen and induce the subsequent chlorination of the surface, which is the cause of lower etch rates. Addition of BCl_3 significantly increases the metal oxide etch rate by enhancing the oxygen removal.

Nakamura et al. [87] studied etching characteristics of high-κ dielectric materials (HfO_2) and metal electrode materials (Pt, TaN) using high-density ECR chlorine-containing plasmas. It was found that the HfO_2 etching rates of

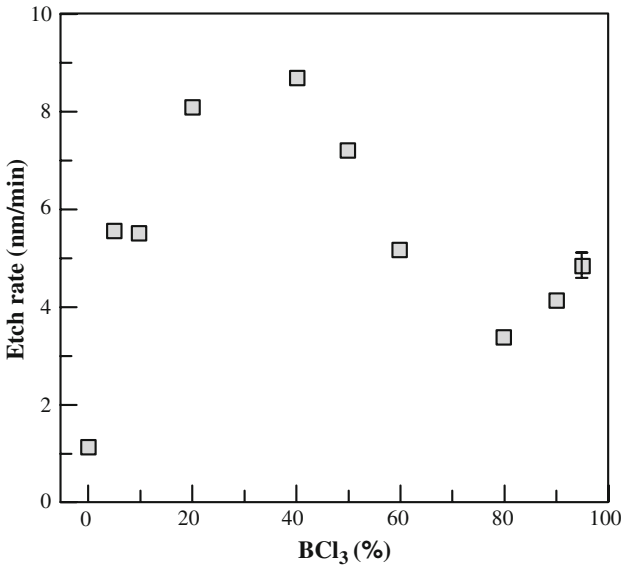

Fig. 12 HfO_2 etch rate as a function of BCl_3 percentage in the BCl_3/Cl_2 plasmas. The experiments were performed at 5 mTorr and 300 W, and an ion energy of 75 eV [86]

Table 3 Recipes for various high-κ dielectric materials (after Han et al. [85])

Dielectrics	Etching recipe
HfO_2 (PVD, RTCVD, MOCVD)	Ion milling: Ar (20 sccm), at 15 mTorr, 150 W, etching time: 2 min for 5–6 nm
HfO_2 (JVD)	Wet etching: BOE (10% HF); Temperature: 20 °C; Etching rate: 3.5 nm/min
ZrO_2 (RTCVD)	Ion milling: Ar (20 sccm), at 15 mTorr, 150 W, etching time: 2 min for 5–6 nm
ZrO_2 (PVD, MBE, JVD)	Wet etching: BOE (10% HF); Temperature: 20 °C; Etching rate: 6 nm/min
La_2O_3 (MBE)	Ion milling: Ar (20 sccm), at 15 mTorr, 150 W, etching time: 2 min for 5–6 nm
Y_2O_3 (RPECVD)	Wet etching: BOE (10% HF); Temperature: 20 °C; Etching rate: 6 nm/min

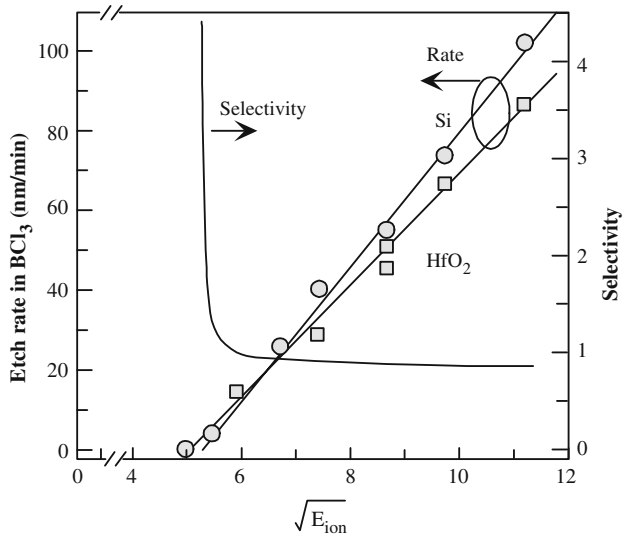

Fig. 13 Etch rate of HfO_2 and Si, and etching selectivity (*dash line*) as a function of square root of ion energy in BCl_3 plasma at 5 mTorr and 300 W [86]

5 nm/min and more than 10 etching selectivity over Si and SiO_2 can be obtained in a BCl_3 plasma source without rf bias. A Pt etch rate of more than 10 nm/min and a TaN etch rate of about 200 nm/min with more than 8 selectivity over HfO_2 and SiO_2 has been obtained in Ar/O_2 with high rf bias and in Ar/Cl_2 with low rf bias, respectively.

Etching properties of HfO_2 based high-κ dielectric films, i.e. HfO_2, HfON, HfSiO, and HfAlO, have been investigated by Chen et al. [88] by using inductively coupled plasma (ICP) of $Cl_2/HBr/CHF_3/CF_4/O_2$. Among HfO_2, HfON, HfSiO, and HfAlO, the etch rate of HfSiO increased most significantly with increasing rf bias power due to the difference of the ternary network of Hf–Si–O from the binary network of other films of Hf–O, Hf–N, Si–O, and Al–O. Etch rates of HfON were higher than those of HfO_2 due to high Hf–N etch rates compared to the Hf–O etch rates. The HfAlO etch rates were lower than those of HfO_2 due to the effect of the low Al–O etch rates. A significant amount of fluorides was shown to exist on the surface after the CF_4/CHF_3 etching. On the other hand, only a small amount of chloride and bromide existed after Cl_2/HBr etching. The amount of residues can be reduced with a high temperature post-treatment step.

Norasetthekul et al. [89] investigated and compared the etch rates and mechanisms for HfO_2 thin films grown on Si substrates in three different plasma chemistries, i.e. Cl_2-, SF_6- and CH_4/H_2-based plasmas, by varying the RIE r.f. source power, chuck power, and discharge composition. The Cl_2- and SF_6-based plasmas showed a chemical enhancement in the etch mechanism, with the selectivity for Si over HfO_2 between 0.2 and 5 obtained by using these two kinds of plasma sources. The HfO_2 etch rates as a

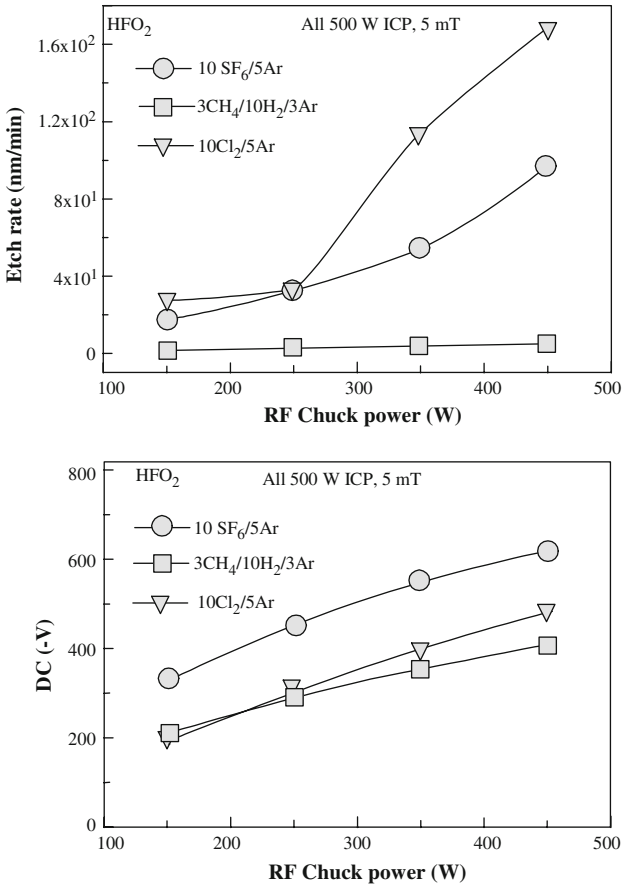

Fig. 14 HfO_2 etch rates as a function of ICP source power in three different plasma chemistries (*top*) and corresponding d.c. self-biases (*bottom*) [89]

function of ICP source power for the three different types of plasma chemistries for a fixed r.f. chuck power are shown in Fig. 14. The resulting d.c. self-biases developed at the sample chuck are shown at the bottom of the figure. In the Cl_2- and F_2-based discharges, an increase in the ion flux and reactive neutral density produces a rapid increase in the HfO_2 etch rate. The removal rates with $CH_4/H_2/Ar$ chemistry were noted to be slower than with pure Ar sputtering for the same conditions. The polymeric film formed during exposure to the $CH_4/H_2/Ar$ discharge prevents the surface from being ion bombarded to some extent and thus reduces the etch rate of HfO_2. Chlorine-based plasma etching was found to be anisotropic for Si except when very heavily doped *n*-type. Using chemistries mentioned above, highly anisotropic features in HfO_2/Si structures have been attained, as shown in the SEM micrographs of Fig. 15.

Pelhos et al. [90] investigated etching characteristics of $Zr_{1-x}Al_xO_y$ thin films in a high-density helical resonator plasma etcher using BCl_3 and Cl_2 plasmas as a function of gas composition and ion impact energy. Higher concentrations of BCl_3 was noted to enhance the etch rate as well

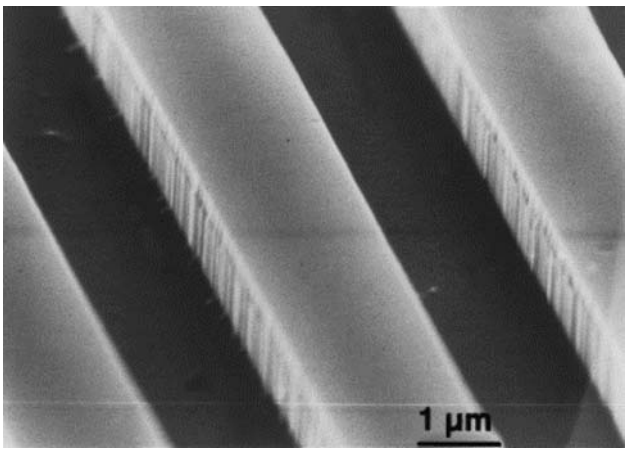

Fig. 15 SEM micrograph of features etched into HfO_2/Si structures using Cl_2/Ar at 10 mTorr. The photoresist mask has been removed [89]

as the selectivity of $Zr_{1-x}Al_xO_y$ vs. Si. On the other hand, increasing the ion energy was seen to increase the etch rates but decrease the selectivity. Etching rates on the order of 700 Å/min and a 1:1 selectivity were observed. The best selectivity was observed in a pure BCl_3 plasma, it was further improved ($\sim$3:2) when the ion kinetic energy was minimized. Angle-resolved X-ray photoelectron spectroscopy revealed that the etching rate of $Zr_{1-x}Al_xO_y$ did not change with time for the range of Cl_2/BCl_3 ratios and ion energies investigated, whereas the Si etching rate in pure BCl_3 plasma and at zero substrate bias decreased with time as a result of formation of an inhibiting B–Si film on the surface.

5 High-κ dielectric properties and challenges

Along with the production of high-κ dielectric materials, their electrical properties and integration with the conventional Si MOSFET technology have taken the central stage. Compared with the conventional SiO_2 oxide and poly-Si electrode, the high-κ oxides present many challenges in the context of compatibility with the Si MOSFET technology. In addition to incompatibility with annealing temperatures used for activating poly-gates, the relatively poor quality, compared to SiO_2, of the high-κ oxide materials causes charge trapping and makes the Si MOSFET gate unstable. The channel mobility degradation, and threshold voltage shift induced by high-κ materials also need to be addressed.

One of the first issues in the context of integration with MOSFET is the suitable gate electrode for the high-κ oxide stack. Nominally, the poly-Si is the dominant gate electrode. In the case of the poly-Si processing, annealing above 1000 °C is necessary for the activating the dopants in the poly-Si layer, which is problematic for the high-κ oxides. Therefore, it is imperative, that the high-κ oxide gate be thermally stable and withstand such a high temperature annealing step. For the HfO_2 gate dielectric, annealing at high temperatures causes crystallization of amorphous HfO_2 into the monoclinic polycrystalline which is not insulating [91]. In addition a 5–10 Å layer of SiO_2 is formed at the interface, which eliminates in part the benefits to be gained from high-κ dielectric [92]. The solution for this problem is to add Si, N or Al into the high-κ layer, each one of which acts to increase the crystallization temperature. Zhu et al. [93] investigated the effect of Al incorporation on the HfO_2 layer. By adding about 30% Al, the HfO_2 crystallization temperature can be increased by 400–500 °C. Furthermore the Al additional also causes an increase of the band gap and a decrease of the dielectric constant of HfO_2, the former being beneficial but no so for the latter. Nguyen et al. [94] added Si into the HfO_2 layer and found that 20% Si can prevent crystallization at the activation temperature used for the poly-gate.

Another issue of importance in considering any gate oxide, and high-κ dielectric is no exception, is that having to do with the channel carrier mobility degradation. Compared with the SiO_2 gate, the high-κ gate layer has soft optical phonons and the long-range dipole associated with the interface excitations would degrade the effective electron mobility in the inversion layer of the Si substrate [95]. Yang et al. [96] summarized the effects of all of the scattering and degradation mechanisms on the inversion channel carrier mobility, as shown in Fig. 16. The addition

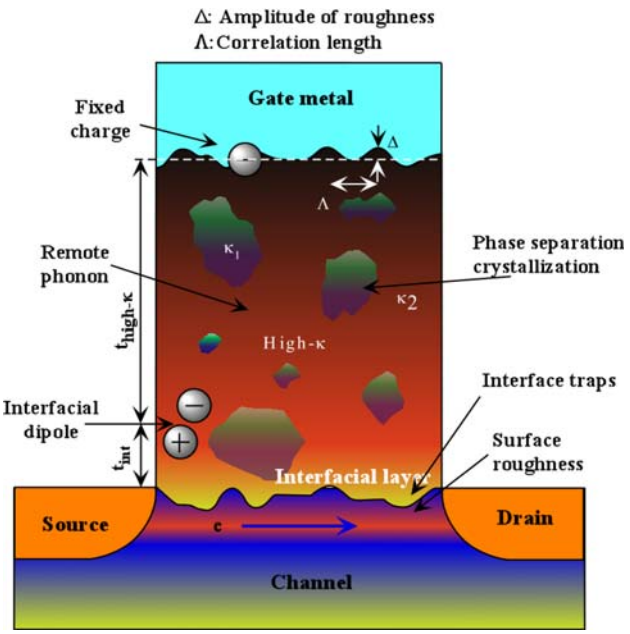

Fig. 16 Schematic representation of factors contributing to carrier mobility degradation in a high-κ oxide layer [96]

of Si into the HfO_2 enhances the mobility, which is argued as being due to the reduction of the remote phonon scattering [97]. As for the N incorporation mentioned above, the mobility is usually reduced. This is because N incorporation induces fixed charge in the high-κ layer and the resulting Coulomb scattering by the fixed charge reduces the carrier mobility [98].

The threshold voltage (V_{fb}) shift of the poly-Si/ high-κ stack is another challenge that must be considered. By introducing Si atoms into the oxide layer, the V_{fb} approaches to that for the SiO_2 case. In order to bring V_{fb} to within $<$0.3 V, which is necessary for the CMOS circuits, the Hf content in the oxide layer should be below 20%. N incorporation can also reduce the V_{fb} shift but to a limited extent. The threshold voltage shift has been attributed to the Fermi-level pinning at the interface [99, 100], which in turn has been attributed to the interfacial Si–Hf and Si–O–Al bonds of the HfO_2 layer as well as the oxygen vacancies at the polysilicon/HfO_2 interface. The interface states partially screen the electric field from the gate electrode, preventing it from modulating the channel fully. Therefore, the efficacy of the gate-induced tuning of the channel carriers is somewhat hindered. An efficient method to reduce the threshold voltage shift is to add a layer of Al_2O_3 on top of the oxide layer. Kim et al. [101] reported the Fermi-level effect free HfO_2 gate stack by depositing an Al_2O_3 capping layer onto $HfSiO_x$. The *p*-MOS gate threshold shift was only 0.2 V. It is likely that the negative fixed charge is introduced into the oxide layer by adding Al_2O_3. Frank et al. [102] used an AlN capping layer to prevent the threshold voltage shift and obtained shift values as low as 0.2 V. Besides an Al_2O_3 cap layer, other oxides have also been applied to prevent threshold voltage shift. La_2O_3 has been used to passivate HfSiO on N-MOSFET. The thermally stable band-edge N-metal work function based on interdiffusion of a bilayer gate dielectric stack (La_2O_3/HfSiO) was attained to reduce the threshold voltage by as much as 0.25V. After 0.5–1.0nm La_2O_3 deposition by MBE or PVD, a post deposition annealing step was used to cause the La_2O_3 layer to mix with the HfSiO layer to form N-metal work function with TaN metal gate. Compared with La_2O_3, a 0.5–2nm Dy_2O_3 cap layer mixed with HfSiO dielectric layer showed a reduction of 0.2V in the threshold voltage.

The last issue that we will discuss here involves the gate electrode used on the high-κ gate oxides. As discussed above, the poly-Si annealing processing causes inter-diffusion of Si. In order to circumvent this drawback, a metal electrode is used instead of a conventional poly-Si variety. However, when incorporating the new metal electrode the complications having to do with the channel mobility, and threshold voltage shift would have to be considered. Another challenge with metal gate is the fact that a poly-Si gate electrode can be used for both *n*- and *p*-MOS by simply adding different dopants. But the metal gate with a fixed work function is not as conducive in that there is not as much flexibility in the work function for *n*- or *p*-MOS when a metal gate is used.

Two approaches can be implemented for tackling the above problem. The first method is to use the so-called "midgap metals" such as TiN [103] with which the Fermi level would be at the midgap of the Si substrate, as shown in Fig. 17. The advantageous feature of these kinds of metal electrodes is the symmetrical V_T value for both *n*-MOS and *p*-MOS, because the Fermi level being at the midgap would allow for the same energy difference between the metal Fermi level and the conduction and valence bands of Si. This provides the basis on which a simpler CMOS processing scheme can be crafted, because only one mask and one metal would be required for the gate electrode, and no ion implantation step would be required.

Another method involves the use of the different metals for *n*- and *p*-MOS, as shown in Fig. 17. So far, many metal electrodes have been applied and studied. However, from the thermal stability point of view, the possible metal

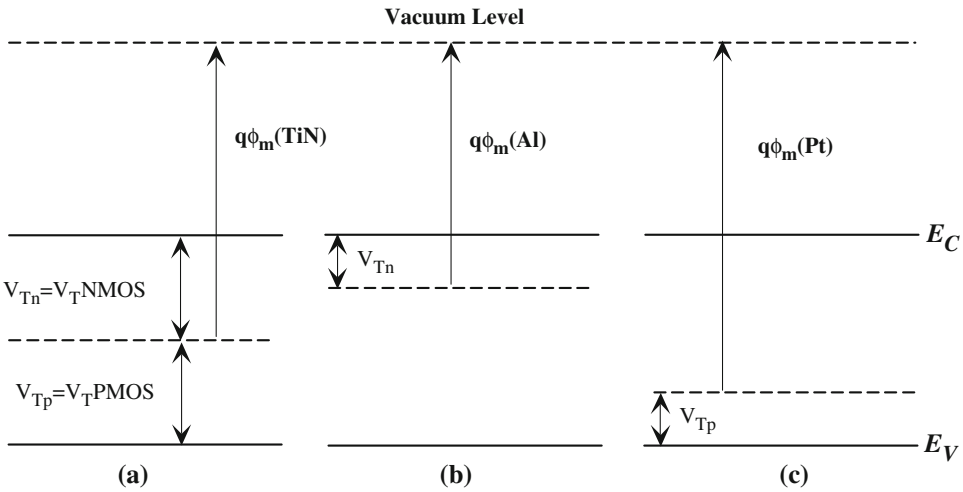

Fig. 17 Energy diagrams of threshold voltages for *n*-MOS and *p*-MOS devices using (**a**) midgap metal gates and (**b**) dual metal gates [3]

choices are limited. Most of the low work function metals are reactive and not stable under the conventional Si MOSFET processing, particularly high temperature annealing. Likely, most of the mid-bandgap metals and high work function metals are stable under these kinds of processing. Callegari et al. [104] used W as the metal gate and investigated the characteristics of the W/HfO_2. They found that even with low interface-state densities (N_{it}), low-temperature (<600 °C) processing resulted in very low electron mobilities. The oxygen diffusion is the key point for the mobility degradation. By preventing the oxygen diffusion and interface re-growth, the mobility degradation can be reduced.

Clearly, the high-κ dielectric materials and related methodologies are crucial for continuing the Si-based scaling engineering. A good deal of investigations dealing with different aspects of this problem has been carried out, particularly toward realizing the integration of high-κ dielectrics with conventional Si devices. However, there are still many obstacles that need to be conquered. In terms of the deposition aspects, the precursors and growth conditions for the high-κ films should be honed in and or optimized further. To prevent the crystallization of the dielectric films during subsequent high temperature processing, the thermal stability issue should be studied to increase the crystallization temperature of the high-κ films. The gate electrodes for the high-κ films and processing integration compatibility are also in need of further research and development.

6 New channel materials

Progress in Si-based MOSFET technology and scaling is not limited to the high-κ materials only in that the search is on for channel material for better transport properties as compared to bulk Si. An immediate approach is to use strained Si which allow occupation of only the low lying conduction bands with smaller in plane effective mass. Both compressive and tensile varieties depending on whether *n*- or *p*-channel MOSFET is being considered have been developed and already incorporated in high performance chips. The projections to longer term developments go beyond strained Si and include possible channel materials such as (In,Ga)As As for the *n*-channel device due to its relatively high electron mobility and velocity, and Ge for the *p*-channel device for its high hole mobility. Needless to say, there is a plethora of challenges that must be faced and overcome before the aforementioned channel materials and possibly others will be implemented. Below, we begin the discussion with strained Si channel and extend it to include GaAs and Ge channels with the associated gate oxide development.

6.1 Strained Si channel

CMOS-based chip speed as well and the density is of paramount importance to the semiconductor industry in particular and electronics industry in general. The conventional Si-based MOSFET is no longer able to fulfill the continued relentless demand for increased speed. The improvement of the channel mobility is a highly important issue for increasing the CMOS circuits speed. A preferred solution is to increase the effective MOSFET mobility while still using the conventional silicon material by utilizing strained silicon channels. The basic idea for the mobility enhancement is to increase the time between carrier scattering events through reducing the effective mass by introducing strained Si channels [105]. Mechanical strain introduced by the lattice mismatch between the Si channel and substrate breaks the crystal symmetry and removes the 2-fold and 6-fold degeneracy of the valence and conduction bands, respectively. This then leads to change of the band scattering rates and the carrier effective mass, which in turn enhances the in-plane mobility of the lower energy conduction electrons. As shown in Fig. 18, under a biaxial in-plane tensile strain (compression out of plane) the band structure of the 6-fold conduction band degeneracy of Si is lifted which results in a 2-fold Δ_2 (out-of plane) and 4-fold Δ_4 (in-plane) band splitting. The 4-fold degenerate conduction bands move upward in energy at a rate of 2.9 meV/kbar (in terms of stress) and the 2-fold degenerate conduction bands move downward in energy at a rate of 5.8 meV/kbar (in terms of stress). Under a biaxial in plane compressive strain (tensile out of plane) the direction of the shift in energy of these same bands is reversed, again as seen in Fig. 18.

In the biaxial in-plane tensile strain, the electrons populate the two low energy Δ_2 bands that also have smaller in-plane electron mass. Biaxial compressive strain (tensile out of plane) also splits the heavy and light hole bands. When used in conjunction with a 2-dimensional hole gas inversion layer, the band splitting caused by quantum confinement is negated by the in-plane biaxial compressive strain. Further increases in the strain begin to split the bands in the opposite direction from the confinement-induced splitting. As a result, high in-plane biaxial compressive strain (tensile out of plane uniaxial strain) results in a considerable valence band splitting which leads to hole mobility enhancement. Essentially, strained silicon can yield higher mobilities by up to 70% for *n*-channel and up to 30% for *p*-channel devices.

As for introducing stress in the Si channel, several methods are utilized. One of the most heavily studied way is to epitaxially grow strained-silicon on a relaxed SiGe layer. The unacceptably high dislocation densities have prevented this method from being implemented in the

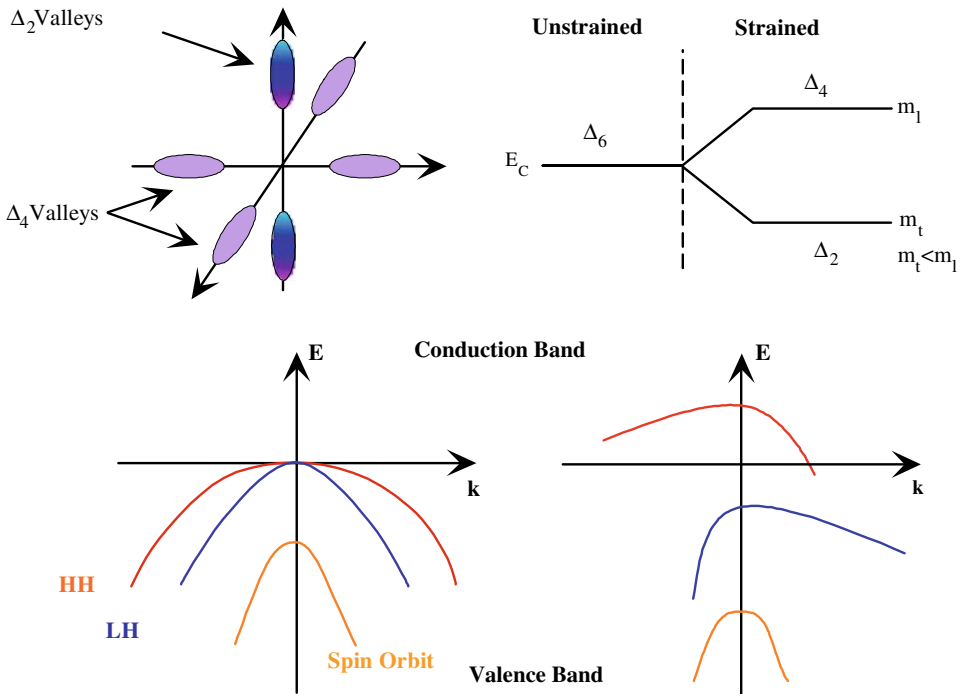

Fig. 18 Biaxial stress effects on the conduction and valence bands of strained Si

industry. Ignoring this for the moment, the lattice mismatch between Si and SiGe substrate can cause the needed stress in Si. Shown in Fig. 19 are three methods of strain introduction. The common method, in terms of the number of research papers on the topic, is to grow the strained Si layer on a relaxed SiGe buffer layer which in turn is grown on a Si substrate. As mentioned the lattice mismatch between SiGe and Si causes the desired strain as shown in Fig. 19a. An alternate approach takes advantage of Si/SiGe layer growth on a SOI substrate [106], as shown in Fig. 19b. The strained Si short channel MOSFET fabricated on an SOI substrate shows 20–25% device enhancement.

Depending on one's point of view, a more complicated method called "wafer-bonding" has been used to remove

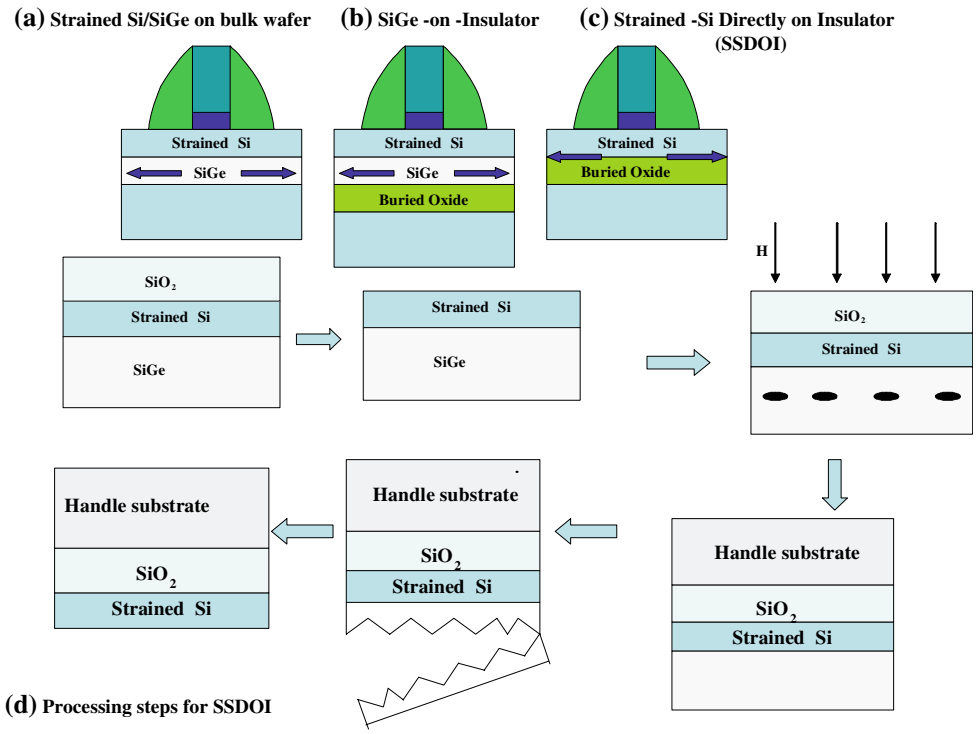

Fig. 19 Schematic diagram to show three ways of formation of strained Si MOS devices: (**a**) Strained Si/SiGe on bulk wafer; (**b**) SiGe-on-Insulator; (**c**) Strained -Si Directly on Insulator (SSDOI); (**d**) Detailed processing steps for Strained -Si Directly on Insulator (SSDOI) method

the SiGe layer from the Si substrate on which it is grown to obtain relaxed SiGe (Fig. 19c) [107]. To accomplish this, a series of steps are taken. First, a thin layer of Si is grown on the SiGe layer and an oxide layer formed on the Si layer. After planarizing the oxide surface with a chemical mechanical polishing step, hydrogen is implanted through the oxide and into the SiGe layer, and the wafer is bonded to a silicon wafer ("handle substrate"). Then by thermal annealing a cavity is formed in the SiGe buffer due to the hydrogen implantation. In the SiGe buffer layer the bonded stack splits at the interface created by these cavities, leaving the buried oxide layer, the strained Si layer, and a layer of relaxed SiGe on the new handle wafer. After a thermal annealing step to strengthen the bonding interface, the thin layer of SiGe on top of the transferred strained Si layer is selectively removed by a combination of polishing and chemical etching with a NH_4OH-based solution. The processing steps are shown in Fig. 19d.

Besides using the epitaxially growth of SiGe to introduce the strain needed in Si channel, strain can also be attained during the fabrication processing which in general is the preferred method in industry as the SiGe approach leads to somewhat dislocated material. Mechanical stress can be transferred to the Si channel through the Si active area and poly gate if a permanent stressor liner is deposited on the device. Ito et al. [108] fabricated 0.13 μm strain Si CMOSFETs by inserting a nitride contact-etch-stop layer that was deposited by PECVD after the silicide formation. The other steps are the same as those with the conventional CMOS fabrication process. However, there is a drawback in that the internal stress in the nitride layer changes the transconductance and degrades the NMOSFET performance by up to 8% although the PMOSFET performance can be enhanced up to 7%.

The stress can also be introduced by a processing scheme named "stress memorization technique". In this process, a tensile stressor capping nitride layer is deposited before the dopant activation annealing [109]. After an annealing step, the nitride layer is removed, and then a Co silicide film is deposited. The entire processing steps are shown in Fig. 20. During the annealing process, the stress can be transferred to the channel layer from the nitride layer and "memorized" by re-crystallization of the S/D and poly gate amorphized layers. Since the nitride film is disposable, a very thick capping layer can be used to increase the stress level without any process limitation.

The last method to form the strain to be discussed here is to fill the source and drain regions with SiGe in *p*-MOS. The epitaxially grown SiGe will lead to laterally compressive strain in the Si channel because of its larger lattice constant than that of Si. NMOS is protected by a capping layer to prevent Si recess during SiGe epitaxial growth. This structure can form a large uniaxial compressive stress

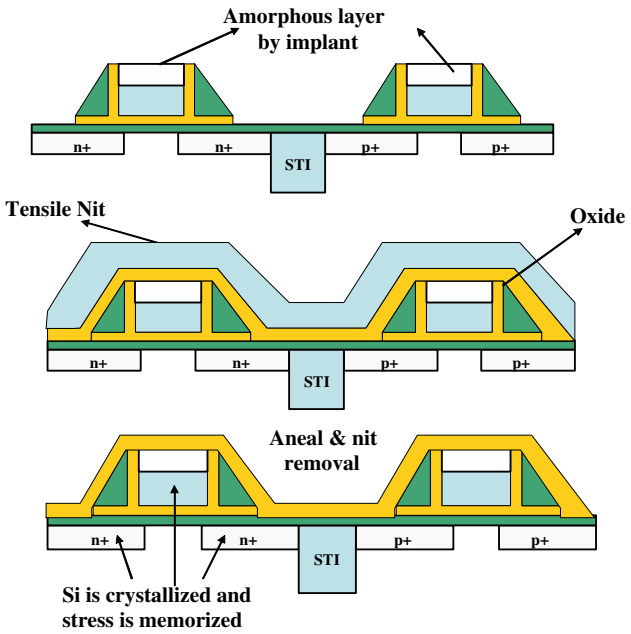

Fig. 20 Integration process of strain memorization technique (SMT). The processing can be expressed as five steps corresponding to the three diagrams in the figure: (**a**) After S/D implantation; (**b**) oxide and tensile nitride deposition; (**c**) S/D and poly dopant activation anneal; (**d**) nitride removal; (**e**) salicidation and subsequent processes. STI: Shallow Trench Isolation [110]

for the *p*-MOS channel and result in significant hole mobility enhancement [111].

Above, we discussed the approaches used to introduce strain in Si channels. There are, however, some specifics as the properties of strained Si *n*- and *p*-MOSFET that deserve further discussion. Since the strained Si *n*- and *p*-MOSFETs are used as part of scaling, both types of channel must be fabricated in the realm of the short channel MOSFET structures. Given the importance and extent of the reach of Si technology, a whole lot of investigations have been undertaken in regard to short channel MOSFETs and short channel effects. For *n*-MOSFET, the first problem is the extrinsic series resistances exacerbated by decreased Si layer thickness. Unless the extrinsic S/D resistance issue is addressed and those resistances are scaled, the gain afforded by strained channel can be negated and the ON current, I_{on}, would be reduced. It is, therefore, important to note that for experimental processes where the gate length is aggressively reduced but other aspects of the transistor remain the same as they are expected of a larger technology node, R_{sd} may constitute a much larger proportion of the total resistance, which could significantly offset any benefit of strained Si on I_{on} for the short channel *n*-MOSFET. An additional reduction of I_{on} enhancement can be expected if R_{sd} is larger for strained Si compared to bulk Si controls, which may be the case if the S/D implant and anneal process cannot be optimized to

compensate for the higher diffusivity and apparent lower electrical activation of As in $Si_{1-x}Ge_x$ [112].

Another issue for the strained Si MOSFET is the conduction band offset. Under strain, the Si conduction band will bend and thus the threshold voltage will change if the same polysilicon electrode layer is used in the strained Si MOSFET. It has been reported that the threshold voltage for strained Si MOSFET is 150 meV lower than that for the bulk Si MOSFET case because of the conduction-band offset at the surface [113]. If an n^+ polysilicon is used as the gate electrode layer, a heavier channel doping is required to compensate the threshold voltage shift. Rim et al. [114] found that for threshold-matched strained Si (on 13% Ge) and bulk Si short-channel *n*-MOSFETs, the effective vertical field E_{eff} for a given V_{GT} was 0.26 MV/cm higher in the strained Si case. However, only 30% mobility enhancement can be obtained in this sort of device. It is found that the Coulomb-scattering introduced by the heavier doping at high electric fields degrades the mobility enhancement in the strain Si channel [115]. This means that in order to obtain the higher mobility enhancement, the strain Si MOSFET should operate at higher effective vertical fields.

However, if a metal gate electrode is used to replace the polysilicon gate electrode, it is not necessary to increase the channel doping to compensate for the band offset. The offset makes strained Si more compatible with a single metal gate work-function solution for bulk CMOS. Xiang et al. [116] used NiSi as the metal gate electrode material to fabricate the 35 nm strained Si MOSFET and found further enhancement in performance with good control over the short channel effects and no degradation in the gate oxide integrity, compared with the polysilicon MOSFET. For strained Si devices with metal gates, I_{dsat} improvements are about 90% for long channel and 45% for 35 nm MOSFETs.

Another problem that is encountered is the *n*-type dopant diffusion in the SiGe layer. Usually, As and P have higher diffusivities in SiGe that in Si, which means that the *n*-type dopants will diffuse into the SiGe layer. This leads to a higher overlap capacitance which exacerbates the short channel effects. Wang et al. [117] found that enhanced diffusion of dopants along the misfit dislocations associated with SiGe/Si leads to increased off-state leakage in strained Si channel devices. They also noted that the process window narrows with increasing thermal budget since both strain relaxation and Ge diffusion are thermally activated. Choosing an optimal process window is, therefore, important for obtaining a robust and manufacturable substrate-strained Si technology.

The last issue we will touch upon for the *n*-MOSFET is the self-heating effect. Since the SiGe layer has a lower thermal conductivity than bulk Si, SOI-like self-heating in strained Si MOSFETs will reduce the current enhancement (Fig. 21) [118].

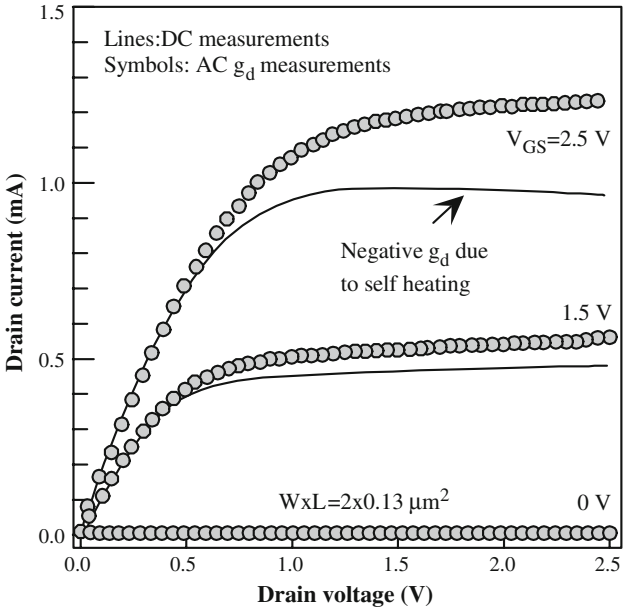

Fig. 21 Output characteristics measured by DC and AC (6 MHz) conductance methods for 0.13 pm strained-Si MOSFET [118]

For a long channel *p*-MOS, hole mobility enhancements vary as a function of gate overdrive. At low vertical fields, the hole distribution tends to be weighted below the surface due to the type-II band alignment between the relaxed SiGe and the strained Si. As the gate overdrive is increased, holes can overcome the band offset and shift toward the surface. The gradual increase of inversion density in the strained Si results in an increase in mobility enhancement with E_{eff} up to 0.35–0.5 MV/cm [119]. For short channel *p*-MOS, although the mobility enhancement for holes is much lower than for electrons the process integration may actually be easier in strained Si *p*-MOSFETs than in strained Si *n*-MOSFETs. *p*-MOSFETs do not exhibit the large reduction in V_T commonly observed in *n*-MOSFETs. Since B diffusion in SiGe is actually slower than in Si, and B has a higher solubility in SiGe than bulk Si, there is no dopant diffusion problem in the *p*-MOS.

From the discussion above, we can glean that the mobility enhancement can be obtained by introducing strain to the Si channel. The strain can be introduced by using a SiGe buffer layer, which captured good deal of attention in the literature, but not practical due to large defect concentration. What is common in industry, however, is the inducement of the same polarity strain by processing methods. However, in order to get as high a possible mobility enhancement, some issues such as the source and drain extrinsic resistances, the increasing electric field caused by band offset compensation, and the self-heating should be addressed.

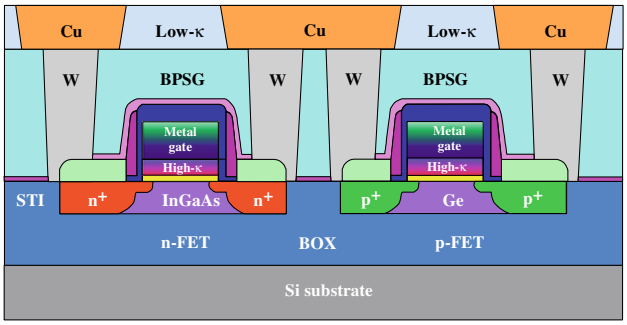

Fig. 22 Ideal CMOS structure for high performance [120]

6.2 Ge channel and pertinent gate oxides

As mentioned above, in order to continue scaling of the Si CMOS, the strained Si channel has been employed for its higher carrier mobility compared with the conventional Si channel. However, the main limitation of CMOS is due to the *p*-channel performance and approaches that would increase the *p*-channel device must be explored. In addition, while the improvements on the *n*-channel device with strained Si are welcome, further enhancements require more radical approaches. In this context, use of (In,Ga)As for *n*-channel and Ge for *p*-channel MOSFETs is carried out (Fig. 22). Bulk Ge has a hole mobility of 1900 cm^2 V^{-1} s^{-1} which is much higher than 450 cm^2 V^{-1} s^{-1} for bulk Si. As the best candidate for replacement of the conventional Si *p*-channel, because of its high *p*-type mobility, Ge has received considerable attention (It is ironic to note that Si was rejected in the early stages of Ge based transistor development, Ge seems to be coming back to help Si CMOS technology). Considering the heterogeneous integration of Ge channel with the Si substrate and the compatibility issues of a Ge channel with the conventional Si processing, there are many problems that must be resolved. First of all, a stable gate dielectric stack for Ge channel CMOS which is also compatible with Si processing must be developed. As alluded to earlier, the first generation of transistors was made of Ge. However, the thermodynamically unstable and water soluble GeO_2 as the perceived gate dielectric hampered efforts to use this material in the semiconductor industry. Besides, it is more difficult, as compared to silicon, to obtain stable oxides with low interface defect densities on Ge due to the chemical and electrical instabilities inherent to the GeO_2/Ge system. The most challenging issue is the Ge surface preparation and interface control before the high-κ dielectric deposition. A possible solution for the surface passivation lies in the conventional Si surface passivation method, namely removal of the native Ge oxide with HF solutions (e.g., HF, DHF) leaving behind a hydrogen passivated surface. Bodlaki et al. [121] found that the H- and Cl-terminated Ge (111) rapidly re-oxidizes in ambient on a timescale of minutes. S- and alkyl-terminations are more robust and show little sign of oxidation after a month of storage in ambient conditions. Thermal annealing is another method to remove the oxides on the Ge surface [122]. In this case, the Ge sample is UV-ozone oxidized at first, and then thermal annealed in the ultrahigh vacuum (UHV) at the temperature above 390 °C for more than 30 min to remove the oxidation layer on the Ge surface.

Nitridation Ge surface has in fact been found to lead to improved surfaces [123]. In this process, a Ge sample is in situ nitridated at 350–600 °C by exposure to an atomic N beam from a remote RF source, at 350 W for 30 s in an ALD chamber. The surface nitridation introduces positive trapped charges and dipoles at the interface, resulting in a significant flat band voltage shift. However, by employing a post-deposition anneal at 550 °C in O_2 before the electrode (gate) metal deposition, the flat band voltage shift can be reduced and the leakage current density introduced by the nitridation step can be reduced. With surface nitridation, the leakage current density, C–V hysteresis, charge trapping, and interface state density can be significantly reduced. Gusev et al. [124] found that nitrided interface shows better electrical quality. Films deposited on the nitrided surface which in an FET becomes the interface, are mostly amorphous, compared with the HfO_2 quasi-epitaxial growth in the case of direct deposition on the Ge surface. It has been found that the interface after thermal nitridation in ammonia is apparently better as compared to that after a wet chemical treatment. After the NH_3 treatment, the GeON interfacial layer forms on Ge surface, which plays a positive role as a diffusion barrier during the remaining portion of the growth [125].

In an alternative approach, annealing of Ge in $SiH_4 + N_2$ has been reported as the effective passivation method [126]. Specifically, the Ge sample in this particular investigation has been annealed in a 400 °C constant temperature chamber with a pressure of 3 mTorr and in $SiH_4 + N_2$ ambient at 5 Torr for 60 s prior to the HfO_2 deposition. The SiH_4 surface passivation can to a large extent prevent the formation of unstable germanium oxide at the surface and suppresses the Ge atom out-diffusion after HfO_2 deposition.

The second issue for the Ge channel MOS structure is the choice of gate dielectric oxide. At the time of this writing, the best oxide candidate for Ge appears to be Ge oxynitride (GeO_xN_y). GeO_xN_y has better thermal and chemical stability than the native Ge oxides (GeO and GeO_2) [127]. With long time nitridation to achieve oxynitride, a glassy network of germanium, oxygen, and nitrogen can be formed. In addition, the incorporation of nitrogen into Ge oxides has the benefit of reducing atomic diffusion between the gate dielectric and substrate and the gate electrode. High-quality thin GeO_xN_y has been formed

on germanium by nitridation of a thermally grown germanium oxide [128, 129]. NH_3 was chosen as the nitridation gas because of its ability to incorporate more nitrogen into the oxynitride film than other nitridation gases. For this process, a step dubbed as he rapid thermal oxidation (RTO) is first carried out at 500–600 °C with a 5–120 s soak time in dry oxygen to form a layer of Ge_xO_y. Then another processing step, rapid thermal nitridation (RTN) is performed at 600 °C with a 1–5 min soak time in ammonia ambient to convert the oxides into GeO_xN_y.

Shang et al. [130] have fabricated strained Ge channel *p*-MOSFETs with a thin gate stack of Ge oxynitride and low-temperature oxide (LTO) GeON dielectric layer on a bulk Ge substrate without a silicon (Si) cap layer. These devices show over two times higher transconductances and 40% hole mobility enhancement over the Si control with a thermal SiO_2 gate dielectric, as shown in the effective mobility curve of the fabricated Ge channel MOSFET (Fig. 23). However, the equivalent oxide thickness (EOT) is ~8 nm, which is not sufficient for MOSFET scaling. In order to stay with the development of the Si CMOS scaling guidelines, other dielectric materials should be considered and used to get higher EOT with thinner oxide layer.

Many high-κ materials developed for Si or strained Si channels have been used in the fabrication of Ge MOSFETs. Chen et al. [131] used remote plasma-assisted chemical vapor deposition (RPCVD) to achieve HfO_2 MOS capacitor structures (EOT = 9.7 Å) on a strained epitaxial Ge or SiGe layer grown on Si substrates. Wu et al. [132] deposited HfO_2 dielectric layers on Ge samples using a SiH_4 and nitridation surface passivation technique before the deposition. The SiH_4 passivated samples were characterized by an EOT of 16.1 Å and the nitridation passivated samples by an EOT of 19.5 Å. Chui et al. [133] deposited a 35–50 Å ZrO_2 dielectric layer on the Ge *p*-MOSFET and obtained a 6–10 Å EOT.

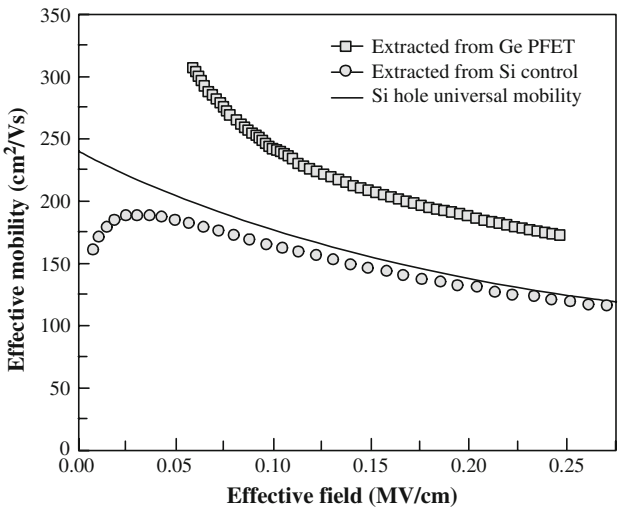

Fig. 23 Effective mobility extracted on (*solid*) of the fabricated Ge *p*-MOSFETs and on (*open*) Si control [130]

The choice of gate electrode for Ge channel devices is another issue that must be addressed. Obviously the conventional poly-Si gate electrode is not suitable for Ge channels because of the required high-temperature (1000 °C) dopant activation processing step for poly-Si and the low melting point of Ge. Therefore, a suitable metal electrodes must be explored for Ge channel devices. Al, and TaN have been tried in conjunction with Ge oxynitride and HfO_2 gate dielectric layers, respectively. As far as the Al electrode is concerned, the interaction between GeON and Al was found to form an interfacial layer between them [134], which causes the EOT of the gate stack to not be sufficiently thin. Compared with Al electrode, W electrode can be used to remove the interface problem and obtain a much thinner EOT stack. The LTO GeON process, as mentioned above, can be employed to prevent the interfacial interaction. By using TaN gate metal and HfO_2 dielectric oxide [135], the TaN/HfO_2/Ge gate stack with an EOT of 12.9 Å and low current leakage density can be obtained. It has been reported that Schottky emission dominates the current in the TaN/HfO_2/Ge gate stack deposited on Ge substrates. Huang et al. [136] employed the fully silicided NiSi (4.55 eV) and germanided NiGe (5.2 eV) dual gates on Al_2O_3/Ge-on-InsuIator (GOI) MOSFETs (EOT = 1.7 nm). The MOSFET with these kinds of gate electrodes showed higher drain current and better reliability, compared with the Al electrode.

As described above, the gate stack and the choice of the gate electrode are the key issues for Ge channel *p*-MOSFETs. Much work still remains, a part of which is the need for a processing technology which is compatible with the conventional Si MOSFET technology either in place or in development. However, to get a higher hole mobility and circuit speed, the MOSFET structure should also be optimized. In this context, many research groups have attempted to design different kinds of FET structures to fulfill the quest for mobility enhancement, as discussed below.

The first and most straightforward approach regarding Ge channel MOSFET is to employ the oxide gate stack on Ge substrate and fabricate it by using the standard processing technology. Before the discussion of Ge channel MOSFET, a key point for Ge channel MOSFET must be mentioned. Considering the integration of Ge channel MOSFET with Si-based technology and further the original idea of replacing the Si channel with the Ge channel, the Ge channel layer is typically epitaxially grown on the Si substrate or SiGe buffered Si substrate. Thus the Ge layer is strained because of the lattice mismatch with the substrate, which can enhance the carrier mobility. The compressively strained Ge channel further enhances the hole mobility due

to the very small effective hole mass (0.1 m_0). As mentioned at the beginning of this particular discussion, the *p*-type Ge channel is promising for replacing the Si channel because of its much higher hole mobility. Therefore, most of Ge channel MOSFET activity is focused on the Ge-based channel *p*-MOSFET. Different from the Si system which has the venerable SiO_2 native oxide, the oxide/Ge interface has a much higher interface defect density. In order to avoid the Coulombic scattering from the interface states and also reduce the leakage current, a very thin Si cap layer is typically inserted between oxide and Ge. Straddled by Si on both sides, the Ge layer acts as the quantum well and confines carriers. In the optimization schemes of this kind MOSFET structure, the thicknesses of Si cap and Ge layer are very important for reducing the band-to-band tunneling (BTBT) leakage current and improving the channel mobility [137]. There is, however, a design tradeoff between the channel mobility and BTBT leakage current. The thicker Si cap layer lowers the electric field in the high-mobility channel and thus reduces the BTBT leakage current. In the meantime, the scattering of the channel carriers by the interface states can also be reduced. However, the carrier density of the Ge channel will also be reduced. The optimal thickness of the Si cap must therefore be figured out. By reducing the thickness of Ge channel layer the defects caused the strain relaxation can be reduced, but at the expense of the channel carrier density which is reduced. Considering these two effects, the thickness of Ge channel layer should be optimized. Another problem with which we should be concerned is to prevent Ge diffusion into the Si interlayer during the annealing step. The Ge diffusion will reduce the thickness of the pure Ge layer and accumulate at the interface, which increases the interface states density and degrades the channel mobility. It has been found that a thickness of 2 nm is optimum for the Ge channel without obvious Ge diffusion. Also a MOSFET with 2 nm Ge channel shows a much higher mobility than those with thicker Ge channels. This is because the channel layer is sufficiently thin and not so readily relaxed through defect generation, at the interface. Furthermore, the quantum confinement effect in the 2 nm Ge channel is better for a higher effective bandgap compared with a thicker Ge channel. The optimum thickness for the Si interlayer is around 4–6 nm, as shown in Fig. 24. With optimized Ge channel and Si cap layer thicknesses, a 3.5 times higher enhancement has been achieved compared with the conventional Si MOSFET. Lee et al. [138] optimized the Si and Ge thicknesses to improve the mobility of Ge channel MOSFET fabricated on a SiGe virtual substrate. It was found that a MOSFET with a Ge layer thickness of 8–12 nm and a Si cap thickness of 3–5 nm shows 8–10 times mobility enhancement, compared to the conventional Si MOSFETs.

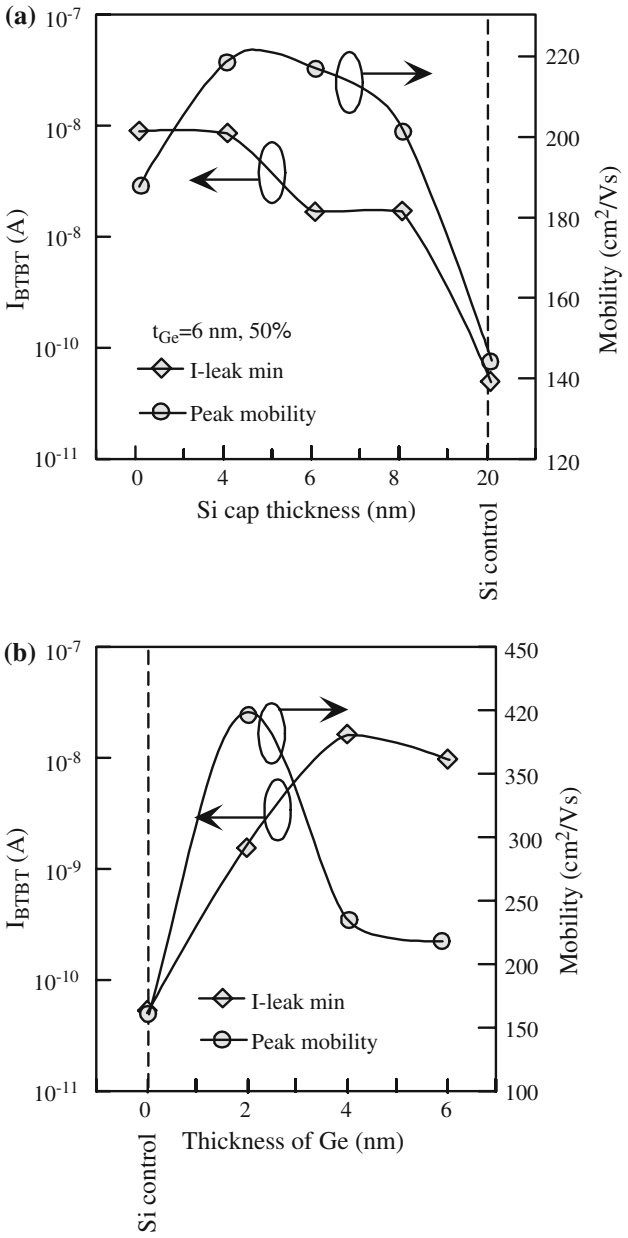

Fig. 24 (**a**) Mobility and band to band tunneling (BTBT) leakage current versus TSi cap; (**b**) Mobility and BTBT versus TGe channel showing that 2 nm is optimum for 100% strained Ge on bulk Si [137]

The second kind of design that should be mentioned is the dual-channel heterostructure MOSFET. A modified structure without the Si cap layer is called modulation-doped field-effect transistor (MODFET). The epi-structure of the MOSFET is shown in Fig. 25. Obviously, this dual-channel heterostructure SiGe MOSFET structure is somewhat different from the Ge channel MOSFET we mentioned earlier, but with some similarities. The strained SiGe layer acts as the trap well to confine the holes. Furthermore, the strain in the layer improves the hole mobility. As the name suggests, this device has two channels. First,

the strained SiGe layer confines the holes in one channel. Second, the Si cap layer forms the other channel when the inversion layer is formed under a gate bias. With increasing gate bias, the holes in the SiGe channel will be pulled to the inversion channel. The dual channel MOSFET has a higher hole mobility than the single channel varieties. Besides, with the strained Si layer and SiGe layer combined together, the strained Si *n*-MOSFET and dual channel *p*-MOSFET can be integrated into the whole epi-wafer simply by adjusting the doping profiles and gate stacks for different FET regions. However, compared with the single layer Si MOSFET, the processing for the dual channel MOSFET is pretty complicated and its performance is affected by several factors.

First of all, the thickness and Ge component of the strained SiGe layer is an important parameter affecting the MOSFET hole mobility. Leitz et al. [139] observed that a MOSFET with a thicker strained SiGe layer exhibited relatively high hole effective mobility. A thin layer of Si cap and a thick layer strained SiGe provide the best performance. A larger hole effective mobility enhancement over the conventional Si MOSFET can be reached by optimizing the thickness of the Si cap layer and SiGe layer. In addition, the alloy scattering, which is more effective at low temperatures, did not seem to hamper the hole mobility enhancement although the mobility varies with the Ge component. From theoretical calculations [140], one can find that the extension of the hole wave function into the Si cap layer and SiGe layer varies with the thickness of both layers. As shown in Fig. 26, the hole wave function extends into the Si cap layer by about 2 nm and the mobility is expected to be reduced due to the interface roughness and the Coulomb scattering centers located at the SiO_2/Si interface. A thinner SiGe layer means further extension of the hole wave function into the Si layer and thus increased scattering. The effect of the Ge concentration on the hole mobility is reasonably complicated because the strain status, valence band offset, and hole effective mass would change with the Ge composition, requiring more extensive treatments.

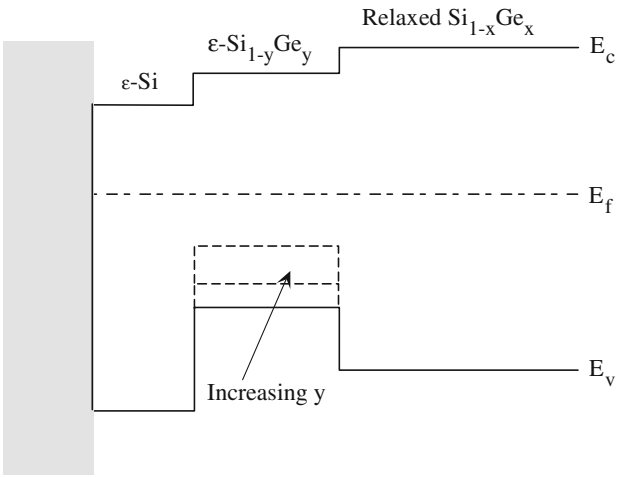

Fig. 25 Epi-structure diagram of the dual heterostructure SiGe MOSFET. The strained SiGe has higher Ge component than the relaxed SiGe substrate. The trapping well for holes will be deeper with the increasing of Ge component in the strained SiGe layer

The thickness of Si cap layer is also very critical for mobility enhancement. In order to attain a higher inversion charge density, the thickness of cap layer should be small. However, as mentioned above, the cap layer should be thick enough to prevent the hole wave function extension and thus reduce the surface-roughness scattering by the SiO_2/Si interface. There is an optimum Si cap layer thickness, as shown in Fig. 27 [141].

In order to get even higher mobilities, strained Ge channels have been explored. A typical strained Ge channel MOSFET is similar to the dual channel SiGe MOSFET. The only difference is that the SiGe strain layer in the latter case is replaced by a strained Ge layer. The Si cap layer in the Ge channel MOSFET is suitable and compatible for fabricating a high-κ gate stack. It has been reported that with strained Ge channel *p*-MOSFET, a hole mobility enhancement factor of 7.5 is possible in the realm of HfO_2 high-κ gate dielectric layer with a 3 nm Si cap layer and a 3 nm strain Ge layer [142].

In addition, the SiGe modulation-doped field-effect transistors (MODFETs) have also been studied. A typical SiGe MODFET is composed of a relaxed $Si_{1-x}Ge_x$ buffer

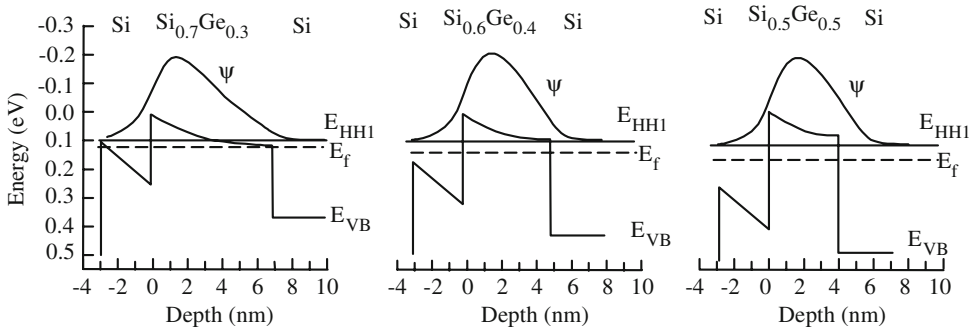

Fig. 26 Calculated wave-functions and energy levels for the first heavy-hole quantum level 7-nm $Si_{0.7}Ge_{0.3}$, 5-nm $Si_{0.6}Ge_{0.4}$, and 4-nm $Si_{0.6}Ge_{0.4}$ quantum wells [140]

layer grown on a Si substrate followed by a thin layer of $Si_{1-y}Ge_y$ ($y > x$), which leads to splitting of the valence bands, reducing inter-band scattering and improving the hole mobility under biaxial compressive strain. The band offset created by strain acts to confine the holes. A typical MODFET device structure is shown in Fig. 28 [143]. Researchers at IBM have investigated the SiGe MODFET extensively and developed MODFETs with different Ge compositions. It was found that the highest mobility could be attained at the point where the Ge concentration approaches 100% due to reduced alloy scattering and the lower valence-band effective mass. For the $Si_{0.3}Ge_{0.7}$/ $Si_{0.7}Ge_{0.3}$ and $Si_{0.2}Ge_{0.8}$/ $Si_{0.7}Ge_{0.3}$ MODFET, hole mobility enhancement of about 5–6 times have been achieved [144, 145]. For a $Ge/Si_{0.4}Ge_{0.6}$ MODFET, more than 6-fold mobility enhancement can be achieved [146].

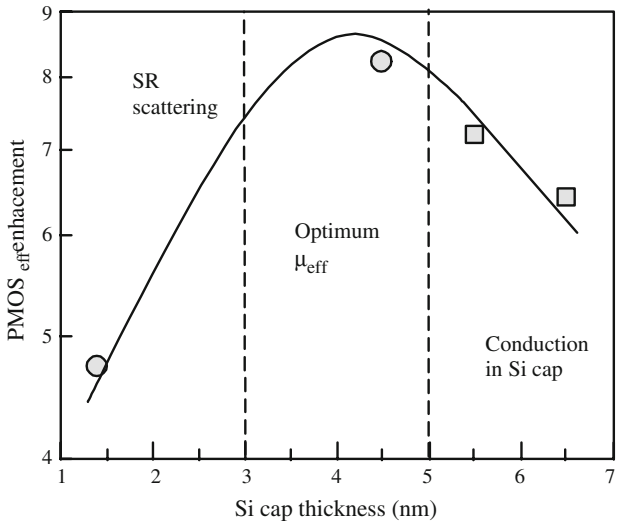

Fig. 27 Dual-channel PMOS mobility enhancement vs h_{Si} cap for strained-Si/strained-Ge heterostructures on $Si_{0.3}Ge_{0.7}$. h_{Ge} = 12 nm (*squares*); h_{Ge} = 6 nm (*circles*) [141]

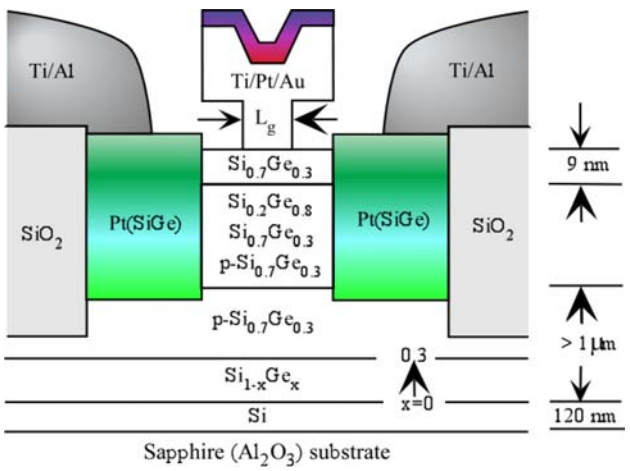

Fig. 28 The cross sectional diagram of a $Si_{0.2}Ge_{0.8}$-channel *p*-MODFET device structure fabricated on a silicon-on-sapphire substrate by IBM [143]

6.3 GaAs channel and associated gate oxide development

GaAs has many advantages over Si for some applications due to its relatively high electron mobility, velocity, and direct bandgap, and has been amply covered in the literature, including many books. In fact InGaAs is even better than GaAs in terms of the aforementioned characteristics. The notion of combining the attributes of GaAs or better yet InGaAs, and Si provided the impetus the scientists to figure out a way to combine them together and get more powerful and useful devices. As a result, GaAs growth on Si substrates has been widely studied by many research groups [147]. If GaAs could be grown on Si successfully, the integration of GaAs devices and Si circuits could be realized. Early investigations of GaAs on Si faced layer cracking due to thermal mismatch between the two materials which was really made harder than it had to be as the model used at the time was that uniform GaAs layers would be required on Si. In reality, however, only a thin sliver of GaAs would be needed to form the channel of an eventual *n*-channel MOSFET. Due to reduced dimensions which the industry has reached, and seeks to reduce them even further, not only the cracking issue would be mitigated but also the extended defect concentration can be reduced as the film dimension in at least two dimensions would be very small. To reiterate, if the conventional Si channel could be replaced by a GaAs channel, the MOSFET operation speed can be improved greatly. Conceptually, the InGaAs has the highest mobility and could even be a better choice for an *n*-channel device.

There are several problems regarding the growth of GaAs on Si substrates. An important one among them is the 4.1% lattice mismatch between silicon and GaAs, and 60% mismatch in thermal expansion coefficients, which to a first extent lead to the high density of defects and cracking, respectively. As mentioned above, small dimensions of the GaAs channel would mitigate much of the problem. Below, however, the issues faced by epitaxial growth of GaAs on Si uniformly over a large area will be discussed as they took much of the scientific discourse in 1980s when the topic picked considerable steam.

Two kinds of typical defects exist in the GaAs-on-Si system: dislocations caused by lattice mismatch and anti-phase domains (APDs). In order to reduce these defects and improve the crystal quality of GaAs on Si, many approaches have been explored. At the beginning of the growth, the most important issue for reducing the defects is the preparation of Si substrates. Contamination of the Si surface by carbon (C) and oxygen (O) is particularly harmful to the epi-layer growth. The oxygen contaminations can be

alleviated by heating Si substrate to 1000 °C. However, the carbon contamination cannot be removed by heating because of the very high heating temperature that would be required. Besides even if one could achieve the requisite high temperature, the carbon can react with the Si substrate and form SiC in the form of three-dimensional nuclei at 800 °C. Therefore, the pre-cleaning procedure is critical for the GaAs growth. The detailed substrate preparation procedure is shown in Table 4 [148].

We have mentioned above that the APD defects form in the GaAs growth on Si, particularly on (001) like surfaces. The APD defects are introduced by the non-uniform coverage of the first monolayer and single steps at the Si surface. Si crystal has the diamond structure with two interpenetrating face-centered cubic Bravais lattices. While, GaAs has the zincblende structure, similar to the diamond structure but the two face-centered cubic lattices either occupied by As atoms or by Ga atoms. Therefore, APDs take place when the allocation of each face-centered lattice to a type of atom is not the same throughout the crystal. In other words, the Ga and As atoms end up in the wrong sublattice in relation to the major portions of the GaAs layer. When present and both types of domains meet, they introduce Ga–Ga (or As–As) neighbors which are electrically charged defects acting as acceptors (or donors). To prevent the APD formation, at the beginning of the GaAs growth on Si, Si surface is usually covered by a monolayer of Ga or As followed by a low temperature buffer layer grown in conjunction with a vicinal (off axis) substrate. Because of the volatile nature of As, temperatures as low as 450 °C must be used [149]. In addition, the low growth rate (0.1 μm/h) during the initial stages of growth (low temperature buffer layer) is required in consideration of crystal quality improvement.

In addition to APDs, another challenge is the high dislocation density introduced by lattice mismatch and thermal expansion difference. Fisher et al. [144] have carried out extensive investigations of various approaches to reduce dislocation density. The first approach is substrate tilt. By adjusting the substrate tilting angles and the sizes of the Si atom steps, dislocation density can be greatly reduced. There are two types of edge dislocation in GaAs epilayers. Type I has its Burgers vector in the nominal substrate orientation ($B = \pm(1/2a)$ [011] or $\pm(1/2a)$ [01−1], (001) being the nominal substrate plane). While type II has its Burgers vector inclined at 45° to the nominal substrate orientation. The type I edge dislocation is preferred since it is more effective in accommodating the misfit compared with the type II. Besides, the type I does not generate threading dislocations, which would propagate into the epitaxial structure above and degrade the epilayer crystal quality. By utilizing vicinal substrates by a suitable angle, the type I dislocations can be preferentially introduced to reduce the dislocations. The diagram in Fig. 29 shows the effect of tilt on substrate surface. Theoretically, every 25 atomic planes a type I dislocation would needed to accommodate the misfit. That means a tilted plane providing one step every 25 atomic planes should be adequate for the misfit. Therefore, the tilt angle should be 1.6°. However, considering the steps at the regular intervals, a larger tilt angle should be prepared to ensure that there are only a negligible number of steps spaced by more than 25 atomic planes. From the experimental point of view, it has been observed that the threading dislocation density of GaAs epilayers grown on the 4° tilted (100) Si substrate toward [001] can be substantially reduced. As mentioned above, the problem could be mitigated considerably by growing only in small areas with one dimension being in a

Table 4 Si substrate preparation for growth of GaAs on it

1	Degrease by boiling in trichloromethane 3 min × 3times. Rinse in acetone/methanol/DI H_2O and blow with dry N_2. Immerse in hot 1:HNO_3, 1:HSO_4 for 5 min
2	5: HCI. 3:H_2O. 3:H_2O_2 at 60 °C for 5 min.
3	2 min. rinse in H_2O
4	1:HF. 10:H_2O for 20 s
5	Rinse
6	5:3:3 solution for 2 min
7	Rinse 1:10 solution for 20 s, rinse, repeat this step 4 times
8	5:3:3 solution for 5 min
9	Rinse in DI water and blow with dry N_2

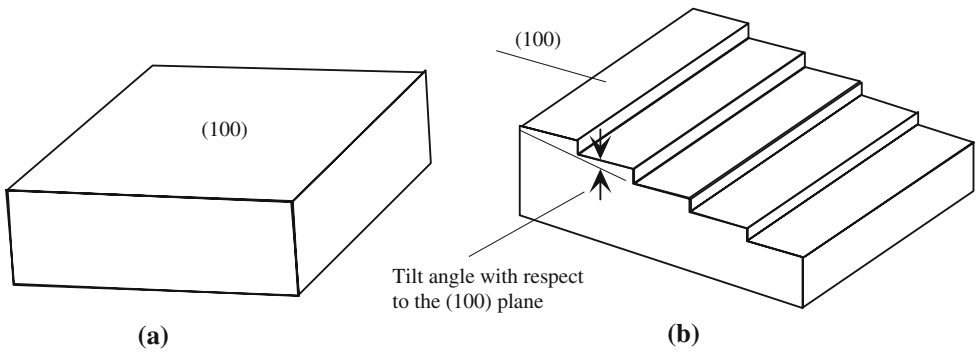

Fig. 29 Diagram showing the effect of tilting on the substrate surface. (**a**) Nominal (001) orientation, (**b**) the orientation tilt off (001) toward [011] [149]

few tens of nanometer in aggressive Si MOSFET designs. In order to reduce the dislocation density further, many other approaches, such as temperature cycling, both during and after growth, introduction of strained layers, and special surface treatments of the substrate have been tried.

Fisher et al. [150] also incorporated strained superlattice interlayers (10-period 100 Å GaAs/100 Å $In_{0.15}Ga_{0.85}As$) to reduce the dislocation density, aided by dislocation gliding direction to be along [111]. It was found that the superlattice structure can efficiently hamper the propagation of threading dislocations and reduce their density near the surface of a 2 μm GaAs epilayer on Si substrates. The strain field of the inserted superlattice can react with threading dislocations, and especially the mixed variety, but less likely with edge dislocations. The strain field introduced by the superlattice can bend the mixed dislocations at the superlattice interface [151]. Soga et al. [152] has used the MOCVD selective growth combined with superlattice interlayers to reduce dislocation density. The first 0.2 μm square (500 μm × 500 μm separated by 500 μm) SiO_2 mask was deposited on Si substrate, followed with a 10-period GaP/$GaAs_{0.5}P_{0.5}$ and 10-period $GaAs_{0.5}P_{0.5}$/GaP superlattice. Although a high quality single crystal GaAs was grown on the area without SiO_2 mask, poly crystalline GaAs appeared on the mask. While this did not necessarily led to dislocation reduction, this method can release the strain and reduce the wafer warping caused by the strain between the GaAs epilayer and Si substrates.

The thermal cycle annealing has been developed as another effective method to improve the crystal quality during MOCVD growth [153]. After a 2 μm GaAs epilayer growth, the thermal cycle, annealing, processing has been employed under the following conditions: at first the substrate was cooled to near room temperature; and then heated to an annealing temperature of around 700 °C for 5 min with AsH_3 flow for protection; this process was repeated 13 times. After the completion of thermal cycle annealing, another layer of GaAs was grown. High crystal quality GaAs epilayer with dislocation density of 2×10^6 cm^{-2} could be realized. The dislocation annihilation can be achieved by dislocation motion under the high thermal stress and temperature, and thermal cycle annealing. After molten KOH etching of the GaAs layer [154], etch-pit density (EPD) can be observed, which is equivalent to the 2/3 of the dislocation density measured by TEM.

The experimental results indicated that the dislocation density was reduced with the number of thermal cycle annealing and temperature difference in the cycle annealing increasing. The changes of EPD with the annealing temperature and cycle number are shown in Fig. 30. Meanwhile, from the numerical analysis results, it was found that the dislocation density can be significantly reduced at a temperature above 700 °C and the higher quality GaAs on Si could be realized with more thermal cycle annealing cycles if GaAs epilayer degradation during annealing can be avoided. A little different from the thermal cycle annealing, a post growth thermal annealing also has been shown to reduce the dislocation density in MBE grown GaAs on Si [155]. It was found that the twins and stacking faults can be by and large removed from the GaAs layer by this annealing step.

Soga et al. [156] developed the epitaxial lift-off (wafer bonding) process to reduce the stress and re-grow the GaAs layer by MOCVD. The schematic diagram for the entire growth sequence is shown in Fig. 31. First the 3 μm GaAs layer grown on GaAs substrate with 10 nm AlAs interlayer is bonded with Si substrate which is treated in the SeS_2 solution dissolved in CS_2. Then, the sample is immersed in HF:H_2O (1:2) for about 1 day at room temperature to lift-off the GaAs layer on the top of AlAs interlayer by selective etching of AlAs. After that, another 3 μm GaAs layer was re-grown on the substrate. The GaAs re-growth

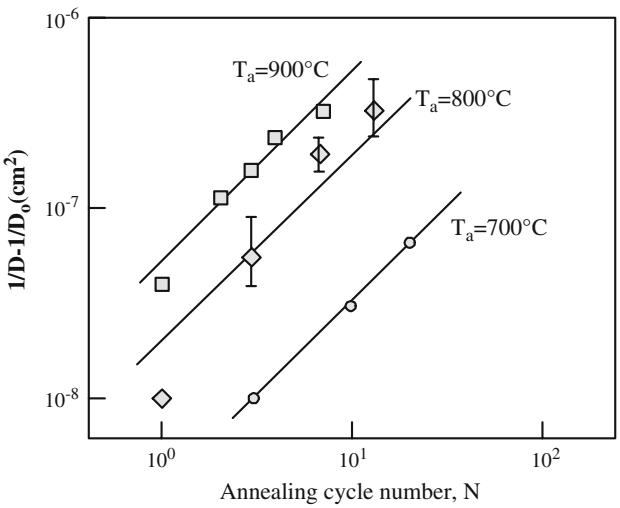

Fig. 30 Changes in inverse etch pit density 1/*D* for thermal cycle annealing as function of thermal temperature and cycle number [154]

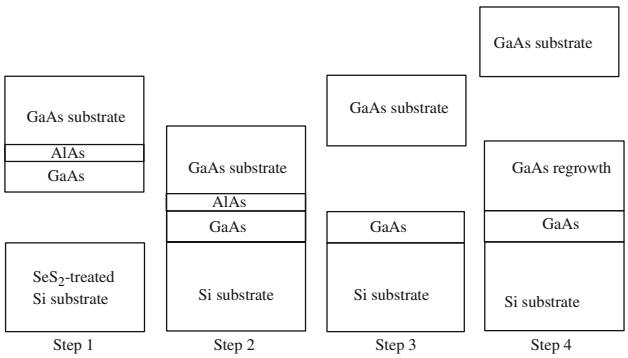

Fig. 31 Process diagram for the epitaxial liff-off and MOCVD regrowth [156]

layer with high crystal quality and almost zero stress can be realized since the bonding process can prevent dislocation formation efficiently compared with the conventional GaAs MOCVD growth on Si substrate.

The buffer layers used to relax the strain in GaAs epilayers have been studied extensively. Takano et al. [157] used an InGaAs interlayer combined with thermal annealing to grow GaAs on Si substrate by MOCVD. The InGaAs interlayer can relieve the strain between the GaAs layer and Si substrate, because of its larger lattice constant. The threading dislocations are sensitive to the In composition of the interlayer and the minimum dislocation density of 1.2×10^6 cm^{-2} corresponds to the In component of 0.09 in the InGaAs interlayer. In addition, the dislocation density can also be significantly reduced by the four-time thermal cycle annealing process compared to the one-time process. ZnSe is another kind of buffer layer material that has been used as an interlayer in MBE growth of GaAs on Si [158]. Due to its softer hardness compared with GaAs and Si, dislocations can be made to reside in the ZnSe interlayer and stopped from propagating into the GaAs epilayer. Combined with post-growth annealing, the crystal quality of GaAs layer can be improved further. Moreover, a-GaAs/a-Si double buffer layer has been applied to the GaAs MOCVD growth on Si substrate to reduce the defect density of the GaAs epilayers [159]. The diagram for the grown structure is shown in Fig. 32.

By using a $SrTiO_3$ (STO) [160] layer as a buffer layer in MBE growth, the dislocation density of the GaAs layer has been reportedly reduced to $<10^5$ cm^{-2} (care must be exercised when the density gets this low for accuracy). After the buffer layer growth, the GaAs epilayer is grown at the end. The GaAs MESFETs fabricated on Si substrate exhibited a mobility of 2682 cm^2/Vs. The 0.7 μm gate length MESFET was shown to operate for over 800 h under a voltage bias with 1.2% degradation in drain current.

6.4 Gate dielectrics on GaAs

Thus far we have discussed the issues surrounding GaAs epitaxy on Si substrates. In order for GaAs to be utilized in the realm of MOSFETs, dielectric materials for the GaAs, or (InGa)As, channel MOSFETs and the associated processing must be investigated in an effort to overcome considerable challenges that exist. As mentioned above, there is a whole host of dielectric materials that can be used as the gate dielectric. However, the critical point is the compatibility of the dielectric materials with both GaAs-based epilayer and conventional Si MOSFET processing.

When it comes to the oxide materials fabricated on GaAs epilayers, the native oxide, Ga_2O_3, surfaces. Passlack et al. [161] studied the Ga_2O_3–GaAs interface comprehensively by using MBE to grow the Ga_2O_3, both by in situ and ex situ means. The in situ method involves deposition of Ga_2O_3 on the GaAs epilayer immediately after the completion of GaAs MBE epitaxy without exposing the surface to atmospheric conditions. In comparison, the ex situ method allowed exposed the GaAs epi-wafer to the atmospheric conditions for as long as three days followed by the deposition of the native oxide on the wafer afterwards. A lower interface trap density, D_{it}, could be obtained by the in situ method, as low as 10^{10} cm^{-2} eV^{-1}, and the interface remained stable up to 800 °C. After the temperature stress by rapid thermal annealing (RTA), the Ga and As 3d binding energies did not change, which shows a good thermodynamic interface stability (Fig. 33). As far as the electrical properties are concerned, quasistatic and high frequency capacitance–voltage measurements did not show any notable frequency dispersion for frequencies above100 Hz for the depletion region, as shown in Fig. 34 which indicates that the characteristic time constant associated with processes involving traps is longer than 1 ms. The larger experimental characteristic time as compared to the calculated value indicated the oxide traps being located about 20 Å away from the interface [162]. In particular, the relatively low resistivity oxide layer in close proximity to the interface acts to reduce the effective oxide thickness and increase the observed capacitance with decreasing

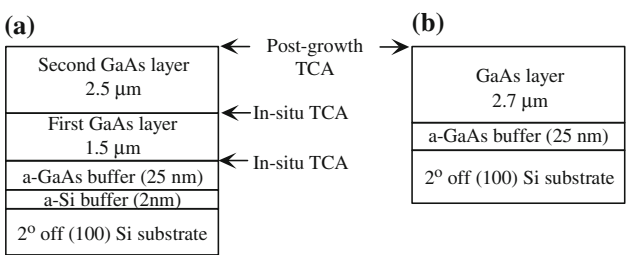

Fig. 32 Schematic of the epitaxial structures grown using (**a**) a-GaAs/a-Si double buffers and (**b**) a single a-GaAs buffer (TCA: thermal cyclic annealing) [159]

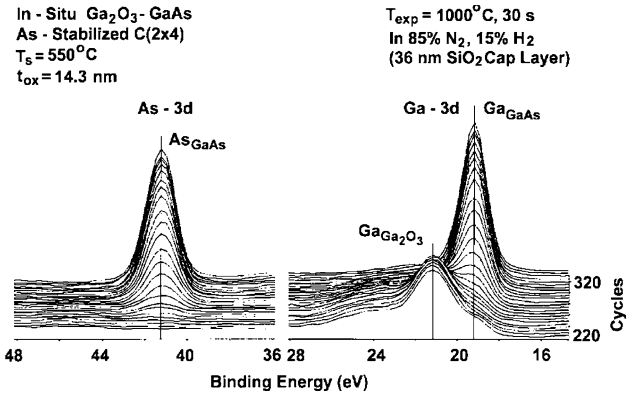

Fig. 33 Interfacial depth profiles of Ga and As 3d core levels of in situ fabricated Ga_2O_3–GaAs structures after RTA [161]

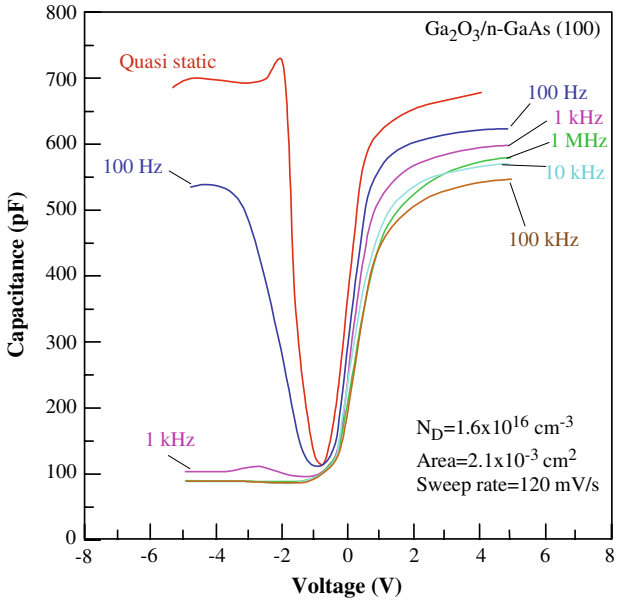

Fig. 34 C–V characteristic of *n*-type samples measured in the quasistatic mode and at various frequencies between 100 Hz and 1 MHz. The oxide thickness t_{ox} is 462 Å [162]

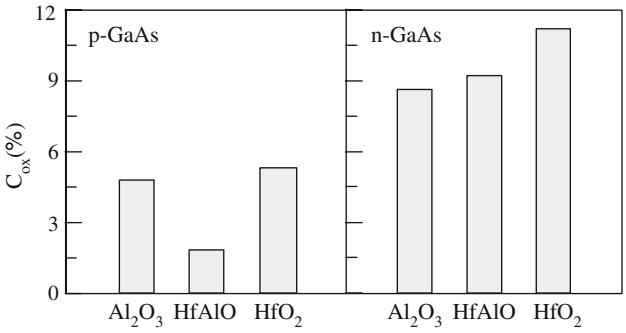

Fig. 35 Frequency dispersion in accumulation capacitance (%) between 20 kHz and 100 kHz for different high-κ on GaAs [164]

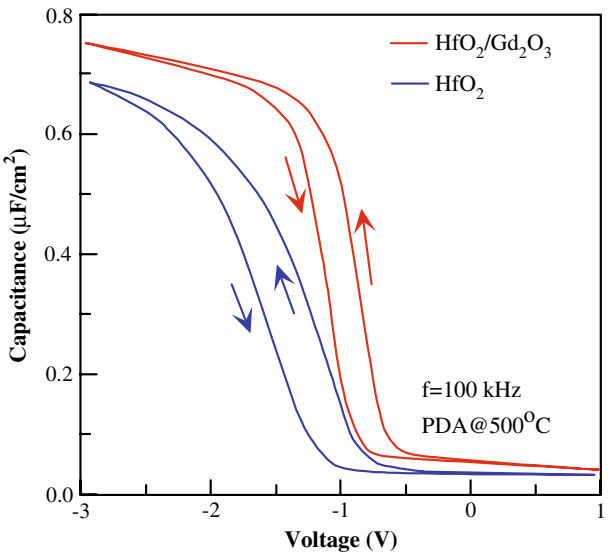

Fig. 36 C–V characteristics of GaAs MOS capacitor at 100 kHz for HfO_2 and HfO_2/Gd_2O_3 gate stacks on *p*-GaAs [164]

frequency. Based on the in situ deposition method [163], the *n*- and *p*-type inversion-channel enhancement mode, *n*-channel depletion-mode $Ga_2O_3(Gd_2O_3)$/GaAs, and *n*-channel enhancement-mode $Ga_2O_3(Gd_2O_3)/In_{0.53}Ga_{0.47}As$ MOSFETs have been fabricated. It should be mentioned that prior to the dielectric deposition, the sample was placed into the MBE chamber to get rid of the native oxide on the GaAs surface. The depletion-mode GaAs MOSFET with $Ga_2O_3(Gd_2O_3)$ gates had a smaller gate leakage current compared to conventional GaAs MESFET. No hysteresis and drain-current drifting has been found in the $In_{0.53}Ga_{0.47}As$ MOSFETs.

In addition to the native oxide, high-κ dielectric materials developed for Si MOSFET have also been applied to GaAs FETs. Tong et al. [164] reported the high-κ dielectric integration on a *p*-GaAs substrates. Four types of high-κ dielectric materials (Al_2O_3, HfO_2, and HfAlO deposited by atomic layer deposition (ALD) and Gd_2O_3) deposited by DC sputtering were investigated and evaluated as far as the reliability and performance of the GaAs MOSFETs are concerned. In contrast to the case of Ga_2O_3 the other high-κ dielectrics on GaAs show a large frequency dispersion and hysteresis. In addition, diffusion of Ga and As atoms into the high-κ layer has been observed which exacerbates the interface quality between the high-κ dielectric and GaAs. The frequency dispersion for various dielectric materials investigated is shown in the Fig. 35. Among them, HfAlO on *p*-GaAs shows the lowest frequency dispersion and interface trap density, D_{it}, without Ga–O bonds at the interface compared with the Al_2O_3 and HfO_2 dielectric layers. Moreover, HfAlO on *p*-type GaAs shows the best electrical properties after post deposition annealing (PDA) at 500 °C (PDA at above 500 °C causes a significant Ga and As atomic diffusion to the interface). Insertion of a thin layer of Gd_2O_3 between HfO_2 and GaAs can efficiently decrease the formation of Ga–O bonds and has been shown to reduce the interface state density. Compared with the C–V characteristics of GaAs MOS capacitors with HfO_2, the HfO_2/Gd_2O_3 gate dielectrics, shown in Fig. 36, have higher accumulation capacitance, less frequency dispersion, and a smaller hysteresis voltage.

The performance of the GaAs MOSFETs has been dramatically improved as a result of research on the gate dielectric interfaces. Kim et al. [165] fabricated *n*-channel depletion and enhancement GaAs MOSFETs by using the MBE to deposit a 20 nm-thick $Ga_2O_3(Gd_2O_3)$ as the gate dielectric layer. The enhancement mode MOSFET with 2 μm gate length showed a peak transconductance of 40 mS/mm. Wang et al. [166] deposited a $Ga_2O_3(Gd_2O_3)$

gate dielectric layer in an ultrahigh vacuum (UHV) e-beam evaporation system connected with the GaAs-based MBE chamber. The 0.8 μm gate length GaAs MOSFETs so fabricated showed a maximum drain current density of 450 mA/mm and a peak extrinsic transconductance of 130 mS/mm. The long-term drain current drift of the GaAs MOSFET is <1.5% during operation for a period of over 150 h. Wu et al. [167] used the liquid phase chemical enhanced oxidation (LPCEO) method near room temperature to grow the $Ga_2O_3(Gd_2O_3)$ gate. The resultant 0.8 μm gate length N-channel depletion-mode GaAs MOSFETs based on this kind oxide gate (35 nm) showed a transconductance larger than 80 mS/mm and the maximum drain current density of 380 mA/mm. Ye et al. [168] applied the ALD method to the dielectric layer deposition on GaAs. Si-doped depletion-mode *n*-channel GaAs MOSFETs having a 0.65 μm gate-length and a 16 nm Al_2O_3 gate oxide were fabricated and showed a gate leakage current density of $<10^{-4}$ A/cm^2 and a maximum transconductance of 130 mS/mm.

Morkoç and colleagues have undertaken comprehensive investigations of SiN as a gate dielectric for GaAs with Si interlayers [169]. Compared to SiO_2, Si_3N_4 is expected to have a lower pinhole density. Besides, the Si_3N_4 is a good barrier to prevent the out-diffusion of Ga and As atoms because of its lack of O and reaction with the GaAs surface. The downside is the bandgap of Si_3N_4 which is relatively small (~5.0 eV). Due to the Fermi level pinning near the midgap of GaAs, caused by oxidation of the surface of GaAs, the MIS structure on GaAs normally has high interface density [170]. A method to prevent the surface oxidation of GaAs is to deposit a few monolayers of Si. However, the atomically thin Si layer must be protected from oxidation as well which necessitates the employment of in situ depositions methods for GaAs, Si, and dielectric layers. Considering the lattice mismatch between Si and GaAs, the Si layer can be made only about 15–20 Å thick without introducing structural defects [171]. In addition, the remote RF plasma was deemed needed to clean and passivate the GaAs surface before the Si deposition [172].

Nominally, a 10 Å thick layer of Si is deposited by using an electron cyclotron resonance (ECR) source generated N_2–He plasma assisted nitridation of a Si layer deposited on a GaAs substrate [173], followed by the deposition of a 300–400 Å thick Si_3N_4 layer using the same ECR source with N_2 gas as the source of nitrogen. The layer is then patterned with variable size dots for either thermal Al or Au evaporation to form the top metal contact. The resultant Si_3N_4/Si/*n*-GaAs structures were shown to have a minimum interface density of 4×10^{11} eV^{-1} cm^{-2} with a hysteresis of <100 meV. Furthermore, by adding atomic hydrogen during the Si deposition on GaAs, the interface quality could be improved and made reproducible under the same conditions [174]. Doing so resulted in a minimum interface state density of as low as 3×10^{10} eV^{-1} cm^{-2}. However, compared to the Si_3N_4 deposited directly on Si/GaAs with the dielectric breakdown field more than 10 MV/cm, the breakdown field for the Si_3N_4/Si/*n*-GaAs structure is 7–8 MV/cm. The current-voltage characteristics at high fields could be explained by Fowler Nordheim tunneling (FNT) conduction mechanism. It was found that the interface trap densities are related to the nitridation temperature during ECR growth [175]. The interface trap densities with a minimum of 3.0×10^{11} eV^{-1} cm^{-2} can be achieved when nitrided at 150 °C. At 400 °C nitridation produced a relatively poor quality interface, which resulted either from the higher temperature or from nitridation of all of the Si, leaving Si_3N_4 in direct contact with GaAs. As can be seen in Fig. 37, the interface density of 3.0×10^{11} eV^{-1} cm^2 for the 150 °C nitridation sample is mainly distributed around the center of the GaAs bandgap.

The thermal stability of the SiN/Si/GaAs stack has also been investigated in an effort to gauge the reliability of an MIS structure. Park et al. [176] found that a 10 Å Si interlayer cannot fully prevent Ga atom diffusion after a post-annealing at the temperature higher than 750 °C. The angle-resolved XPS core-level spectra, shown in Fig. 38, taken after a post-annealing at 600 °C show no obvious change in the structure. However, after 800 °C annealing

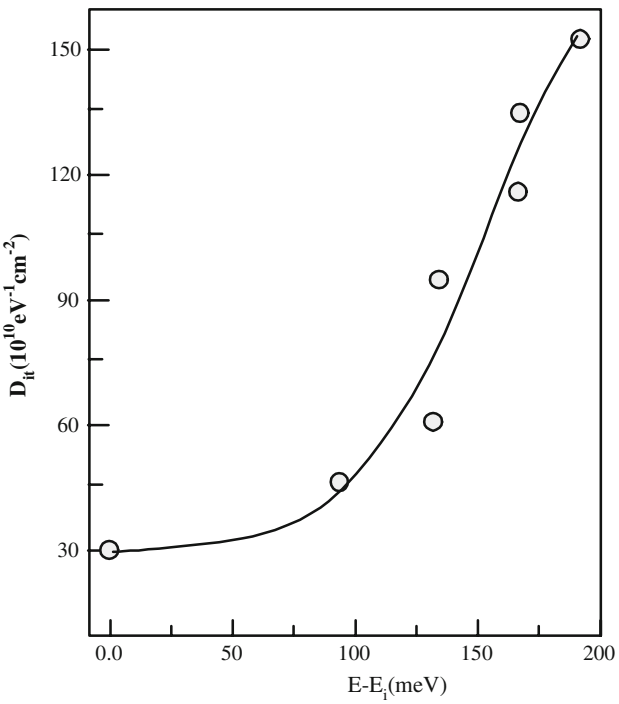

Fig. 37 Interface state density distribution across the GaAs band gap for a sample nitrided at low temperature. The solid curve is a Gaussian function fitted to these points [175]

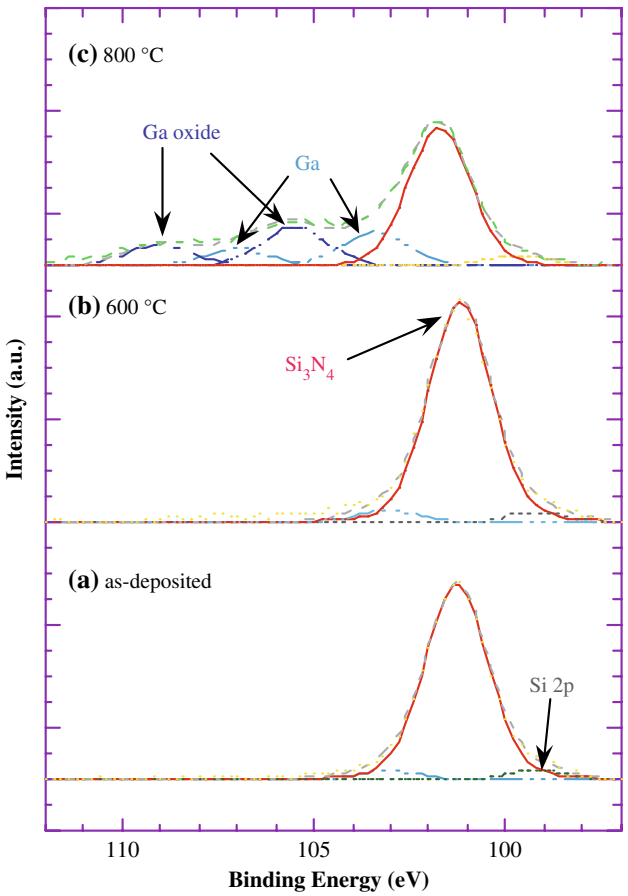

Fig. 38 A multiplex spectra of Ga 2p and Si 2p peaks on Si3N4 (20 Å)/Si(10 Å)/*p*-GaAs structure with (**a**) as-deposited, (**b**) RTA of 600 °C, and (**c**) RTA of 800 °C [176]

Ga oxide and pure Ga spectra were identified in the spectra. It is likely that the Ga atoms diffuse out from the GaAs layer after annealing above 750 °C. It was found that the sample annealed at 750 °C shows the obvious degradation and a distinct shift of the C–V curves of GaAs MIS diode from QS C–V and 100 kHz curves, as shown in Fig. 39. The increased capacitance of the MIS structure investigated indicates that the effective Si_3N_4 layer becomes thinner after having been subjected to the degrading annealing conditions. For this sample, there is a hysteresis of about 50 mV under a field excursion of 1.5 MV/cm, with a fixed charge density of 1.2×10^{11} cm^{-2} near the interface. By comparison, the hysteresis associated with the sample annealed at 800 °C increased to 350 mV.

Besides the Si interlayer, Si/Ge interlayers have also been applied on the SiN/GaAs MIS structure [177], and has been shown to improve the depletion mode performance of GaAs MISFETs. A GaAs MISFET with Si(<10 Å)/Ge(20 Å) interlayer showed a much smaller response time of minority carriers due to the smaller band gap and higher intrinsic carrier concentration of Ge. The SiN/Si/InGaAs

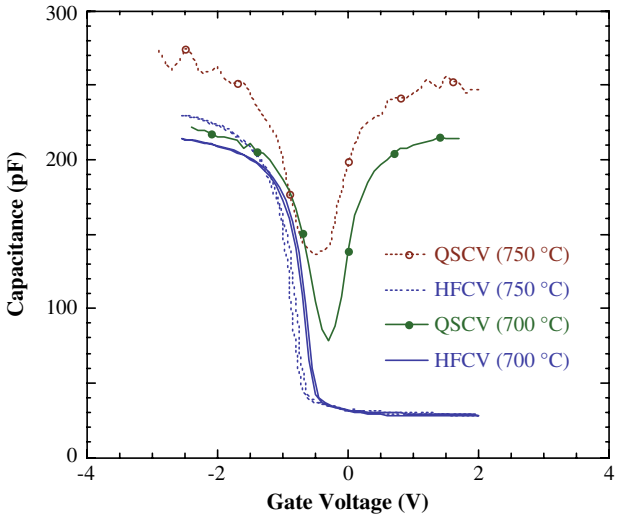

Fig. 39 The C–V characteristics of the Si_3N_4/Si/*p*-GaAs capacitors as a function of rapid thermal annealing (RTA) temperature. The features of high frequency (HF)/low frequency (LF) C–V profiles of the sample annealed at 700 °C and 750 °C are compared at 100 kHz and quasi-static, respectively [176]

interlayer MIS structure was another attempt to improve the performance of GaAs MISFET. A 150 Å thick $In_{0.05}Ga_{0.95}As$ interlayer between Si and GaAs was shown to increase the minority carrier recombination rate in the InGaAs channel 4–5 orders of magnitude higher than in the GaAs channel [178]. It has been argued that a quantum well is formed in the InGaAs layer due to the smaller band gap as compared that of GaAs.

Confinement of electrons in this quantum well together with a higher doping level in $In_{0.05}Ga_{0.95}As$ makes the minority carrier recombination time shorter than that of the GaAs channel. With the incorporation of InGaAs channel into the conventional GaAs FET structure, MISFETs with gate length of 3.0 μm operating in depletion mode with a transconductance of 170 mS/mm have been realized. The incorporation of InGaAs into the GaAs channel shows increasing of channel electron density and the drain current. The MIS structures with InGaAs channels represent a milestone for GaAs MOSFETs and pave the way for the applications of the high mobility GaAs MOSFETs.

In the ensuing years, GaAs MOSFETs and MISFETs with InGaAs channel have been comprehensively studied and their performance has been again verified to be much better than the conventional GaAs MOSFETs. Rajagopalan et al. [179] realized 1 μm gate-length enhancement mode InGaAs *n*-channel GaAs MOSFETs which show transconductances exceeding 250 ms/mm. By using an InGaAs channel and amorphous $Ga_2O_3/(Gd_xGa_{1-x})_2O_3$ gate dielectric layer, the channel mobility was shown to reach to 5500 cm^2/V s. Tsai et al. [180] demonstrated depletion-mode GaAs-based MOSFETs with a $Ga_2O_3(Gd_2O_3)$ gate

oxide stack and $In_{0.15}Ga_{0.85}As$ channel. Comparing with the MOSFETs without InGaAs channels, the $In_{0.15}Ga_{0.85}As$ channel 1.6 μm gate-length GaAs MOSFETs showed a larger current density of 510 mA/mm. Recently, Hill et al. [181] fabricated 180 nm gate InGaAs channel GaAs MOSFETs with transconductances of over 425 mS per mm of gate width which is much higher than the results reported before.

7 Outlook

As the microelectronics industry continues to scale down the dimensions of MOSFETs and the associated layer structures, new approaches must be developed to fulfill the need for increased chip speed and gate leakage current and reduced power dissipation. In order to decrease gate leakage current, which is exacerbated by decreasing gate stack thickness, high-κ dielectric materials are being explored rather comprehensively to replace the venerable SiO_2 gate dielectric. To increase the chip speed, higher mobility channels, initially by applying strain to Si but ultimately other semiconductors must be explored. The strained Si channel has already been incorporated in commercial CMOS circuits. However, the next step might involve semiconductors such as Ge and GaAs owing to their high hole mobility and high electron mobility, respectively. However, there are many problems which must be successfully addressed before these materials, which would have only a few decades ago been considered radical approaches, to be used in commercial CMOS. Critical issues such as dislocations in the channel layer resulting from heteroepitaxy, process integration compatibility, and the choice of gate dielectric materials must be thoroughly investigated and gotten under control. If the past is a reflection on the future, innovations will continue to rule the landscape and new concepts will find their way into CMOS circuits.

8 Conclusions

We discussed the critical issues dealing with some aspects Si device scaling including high-κ dielectric and potential channel materials along with the new requirements brought about by the new channel materials. As clearly delineated by the Si industry roadmap, scaling is imperative for improving the speed of Si-based integrated circuits. With channel length scaling and associated gate dielectric thickness reduction, the gate current leakage becomes increasingly intolerable which necessitates exploration of high-κ dielectric materials having tolerably large physical thicknesses but with equivalent oxide thicknesses consistent with scaling. In order to prevent what would be the gate leakage current caused by defects in the high-κ films, the high-κ layer should be either perfect single crystal or amorphous and remain amorphous during subsequent processing. The structural mismatch between Si and high-κ materials prevents one from obtaining nearly defect free single crystalline dielectric material. In contrast, amorphous high-κ materials with good glass-like network can function as a barrier to prevent gate leakage current. Thus, nearly all of the high-κ related investigations have focused on amorphous films. A variety of deposition methods has been used for the high-κ deposition. It appears that the atomic layer deposition (ALD) method is the most widely used technique despite the fact that other methods also led to attractive results. However, the choice of a precursor for the ALD growth is one of the most crucial issue as impurities and defects are introduced by the precursors. The process integration is another important issue for the high-κ materials. In order to improve the interface quality and reduce the defects density in high-κ films, some other elements are introduced into the pure high-κ layers. Among them are Al and Si that are added to the high-κ layers have been shown capable causing the interface to be sharp and reduce scattering channel carriers by high-κ gate layers. Moreover, adding N and F atoms to the high-κ layers can effectively prevent the gate current leakage. Etching is another important process for the device fabrication. Comes with wet etching and dry etching are the advantages and disadvantages of various high-κ dielectric layers and stacks. The challenges faced by the CMOS community in this respect have also been treated in this review. Also important regarding the high-κ materials is the choice of the gate electrode as poly Si is most likely not the proper one. The poly-silicon gate electrode used exclusively in the conventional SiO_2 based CMOS cannot fulfill both *n*- and *p*-type MOSFETs' needs in conjunction with high-κ gate dielectrics. If the different metal gate electrodes are to be chosen for the *n*- and *p*-type respectively, the process integration capability must be systematically investigated. Despite the challenges mentioned above and the dominance of SiO_2, great strides have been made in Hf-based gate oxides and carried forward to production. For example, Hf-based high-κ materials have already been implemented in commercial products such as the Intel 45 nm Penryn processor which utilizes Hf-based high-κ /dual metal gate CMOS technology. Additionally, NEC is marketing a poly-Si/Hf-based high-κ low-power technology. As always, other companies are following suite by announcing high-κ products for the near future.

From the channel material perspective germane to scaling engineering is the channel mobility enhancement. The conventional Si channel can be viewed as having reached or about to reach its limit in terms or the mobility

of Si for the higher speed integration circuits. In response, the industry already incorporated strained Si channels while considering Ge, and (In,Ga)As channels for the longer term. Strained Si has higher carrier mobility due to the band structure modifications caused by strain. The critical issue faced is how to obtain high quality and reliable strained Si channels. By using the SiGe buffer layer growth, strain can be introduced, but the associated defect density is still too high for commercial CMOS. Instead process induced strain has been used to strain the Si channels. The other issue of importance is to attain as high a mobility enhancement as possible. As mentioned already, the choice of the gate electrode is also a problem for the strained Si. The conventional polysilicon gate subjects the channel carriers to additional scattering making the case for metal gate electrodes.

To improve the *p*-MOSFET mobility beyond that provided by strained Si, the Ge channel devices have been investigated reasonably comprehensively. The gate oxide integration with the Ge channel, mobility enhancement, and the leakage current reduction have also been discussed in detail. The GaAs based channel is a candidate for the *n*-MOSFET due to the much higher electron mobility of GaAs compared with Si. However, large lattice mismatch makes it difficult to integrate the GaAs with Si substrate unless small area selective epitaxy is used. Many investigations have been carried out on GaAs deposition on Si substrates. An associated problem is the gate oxide with GaAs channel. In order to improve the electron confinement and increase the channel mobility, the InGaAs channel in place of GaAs has been introduced. The oxide materials such as Si_3N_4, HfO_2, ZrO_2, and Gd_2O_3 have been tried for GaAs channels.

Overall, the scaling engineering undertaken by the Si industry is a rather ambitious and in someway colossal step (consistent with the size of Si CMOS industry) for the future of the Si MOSFET based integrated circuits. There are many aspects that must be addressed and conquered simultaneously. In the upcoming years, a plethora of techniques will undoubtedly explored at the research level which will be following by insertion by the industry in the Si CMOS circuits making the devices smaller, faster and less expensive.

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