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The influence of temperature hysteresis at metal-semiconductor phase transition on current-voltage characteristic of VO_2–based ceramics

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The current-voltage characteristics of ceramics (wt%) $80VO_2$-15VPG-5Cu and $45VO_2$-15VPG-5Cu-$35SnO_2$ were investigated (VPG—vanadium phosphate glass). After switching to high electric current, these characteristics show a hysteresis loop in the electric current increase-decrease cycle. The cause of hysteresis is the different phase transition temperatures in VO_2 crystallites for transition from semiconductor phase to metallic phase and for the reverse transition. The distinction of phase transition temperatures leads to the different equilibrium temperatures in the filament of the metallic VO_2 phase, when 'electric current increases and decreases. As the result, different power dissipated by electric current in ceramics sample is necessary for ensuring thermal equilibrium in the filament. This is the reason why current-voltage characteristic registered at electric current increase do not coincide with characteristic registered at electric current decrease.

1. Introduction

Scientific and practical interest in vanadium dioxide (VO_2) is caused by metal-semiconductor phase transition (MSPT) at the temperature $T_t = 68°C$. This transition is accompanied by abrupt change of conductivity and other properties [1, 2]. On basis of VO_2 the ceramic materials are created [3, 4]. Such materials have electrical resistance change up to 2–3 orders of magnitude near the temperature T_t and show the phenomenon of threshold switching. After switching into high-conductivity state, VO_2-based ceramics can conduct electric current up to several amperes [5]. Therefore such ceramics can find an application in electric current inrush limiters [6] and switching devices [7].

The reason of switching in VO_2 and VO_2-based materials is the heating of the sample by electric current up to the phase transition temperature T_t. The filament of metallic VO_2 phase is formed in a sample at switching [8–10] and defines its current-voltage characteristic (CVC) after the switching [5, 8]. Semiconductor VO_2 phase is located outside this filament. Therefore the filament border is the interphase border. This border relocates when electric current changes. This relocation is accompanied by phase transition in VO_2 located near the interphase border.

The different temperatures for transition from semiconductor state to metallic state and for reverse transition from metallic state to semiconductor state are the peculiarity of metal-semiconductor phase transition [8]. This leads to hysteresis, which is typical for temperature dependences of conductivity and optical parameters of VO_2 monocrystals and films [8, 11]. The hysteresis of CVC for vanadium dioxide and VO_2-based materials practically is not investigated, while the temperature hysteresis at MSPT can take effect in CVC, because the moving of filament border is accompanied by phase transition in vanadium dioxide.

The purpose of this research is to study the influence of temperature hysteresis at metal-semiconductor phase transition on current-voltage characteristics of VO_2-based ceramics.

2. Experimental procedures

Ceramics (wt%): $80VO_2$-15VPG-5Cu and $45VO_2$-15VPG-5Cu-$35SnO_2$ are the object of this investigation. Initial components: VO_2 crystal powder, produced by technology described in [12], vanadium phosphate glass (VPG) of composition (mol%) $80V_2O_5$-$20P_2O_5$, the additives of Cu and SnO_2 were mixed in the given proportion. After homogenization the mixture was pressed and then was heated up to $(950 \pm 10)\,°C$ in argon with subsequent cooling up to room temperature.

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The ceramics $80VO_2$-15VPG-5Cu has density 3.01 g·cm^{-3} and porosity ~29%. The density of ceramics $45VO_2$-15VPG-5Cu-$35SnO_2$ is 3.66 g·cm^{-3} and porosity is ~24%. Ceramics samples had diameter of 10 mm and thickness of 1.6–2 mm. Ohmic contacts to the samples were created by copper electrodeposition. For that we used the procedure described in [13]. The sandwich geometry for electrodes on the sample was used. Copper electrodes had thickness of 10 microns and diameter of 8 mm.

The current-voltage characteristics have been measured at the temperature of (20 ± 0.5) °C. For limitation of electric current at CVC registration, 20 Ohm resistor was connected sequentially with the sample. The electrical current has been determined by measurement of voltage drop on the resistor of (1 ± 0.001) Ohm, which was connected sequentially with the sample. Voltage on resistor and the ceramics sample has been measured by digital voltmeter with relative error no more than 0.5%. When measuring CVC the stable magnitudes of electric current and voltage have been registered. These magnitudes are corresponding to thermal balance for investigated sample.

Conductivity temperature dependences have been measured at change of temperature with the speed no more than 0.8 °C/min. Electrical resistance of the ceramics samples has been measured by the bridge method with relative error ±0.1%. When registering the temperature the absolute error was ±0.25 °C.

3. Results and discussion

The current-voltage characteristics for VO_2-based ceramics are represented in Fig. 1. These characteristics were measured, when electric current was increasing at first and then decreasing. Current-voltage characteristics of VO_2-based ceramics show the threshold switching which is typical for VO_2 crystals and films [7, 9, 10]. Arrows in Fig. 1 show directions for the switching between the regions of CVC with low and high electric current. Dashed lines join the points between which the switching takes place. For CVC region of high electric current the negative differential resistance (NDR) is typical.

As it follows from data of Fig. 1, the CVC branches measured at electric current increase and decrease do not coincide. For CVC region with NDR the branch registered at electric current decrease is shifted to low electric intensity. The branches, measured at electric current increase and decrease, coincide for low current region of CVC in ceramics $45VO_2$-15VPG-$35SnO_2$-5Cu. For ceramics $80VO_2$-15VPG-5Cu in this region of CVC the branch measured at current decrease is shifted to higher electric intensity. Such behavior shows increase of electric resistance of the sample. Notice, that all VO_2 crystallites in the ceramic sample are in semiconductor phase before threshold switching. Therefore the temperature hysteresis at MSPT cannot be the reason, why the branches of current-voltage characteristics for low current region do not coincide in ceramics $80VO_2$-15VPG-5Cu.

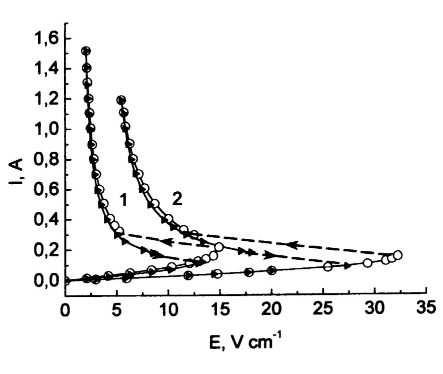

Figure 1 Current-voltage characteristics, measured at the electric current increase (circles) and decrease (triangles) for ceramics $80VO_2$-15VPG-5Cu (1) and $45VO_2$-15VPG-5Cu-$35SnO_2$ (2).

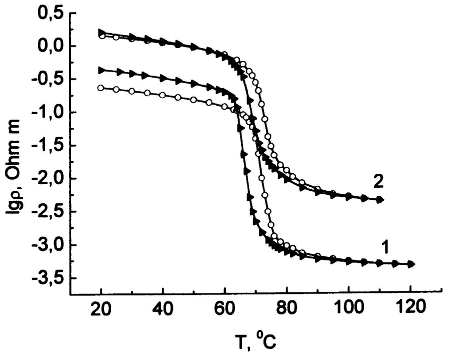

Figure 2 Temperature dependences of specific electric resistance, measured at the temperature increase (circles) and decrease (triangles) for ceramics $80VO_2$-15VPG-5Cu (1) and $45VO_2$-15VPG-5Cu-$35SnO_2$ (2).

This reason may be understood from Fig. 2, where the temperature dependences of specific electric resistance are shown. These dependences were measured in temperature increase-decrease cycle. After thermocycle the specific electric resistance increases for ceramics $80VO_2$-15VPG-5Cu and practically does not change for ceramics $45VO_2$-15VPG-5Cu-$35SnO_2$. The irreversible decrease of vanadium oxides conductivity at thermocycling through MSPT temperature is caused by microcrack formation [14, 15]. The reason for microcrack formation is the strong mechanical stresses in the region of interphase border [8]. Tin dioxide has the stabilizing effect. Therefore conductivity of ceramics $45VO_2$-15VPG-5Cu-$35SnO_2$ at the cycle of heating-cooling through MSPT temperature practically does not show changes (Fig. 2). It explains the coincidence of branches for low current region of CVC in ceramics $45VO_2$-15VPG-5Cu-$35SnO_2$. Similar behavior of this CVC region takes place in ceramics $80VO_2$-15VPG-5Cu, when the voltage does not exceed the threshold voltage. In this case the switching and consequently phase transition in VO_2 crystallites of ceramics does not occur.

Thus, one can expect influence of temperature hysteresis at metal-semiconductor phase transition in VO_2 for the high current region of CVC. The hysteresis loop for this CVC region is represented in Fig. 3. The hysteresis loop was measured in two consecutive cycles of electric current increase-decrease for ceramics $45VO_2$-15VPG-5Cu-$35SnO_2$.

To explain this phenomenon it is necessary to take into account that the filament of metallic VO_2 phase was formed at switching [8–10]. Such filament contains VO_2 crystallites in metallic phase and controls

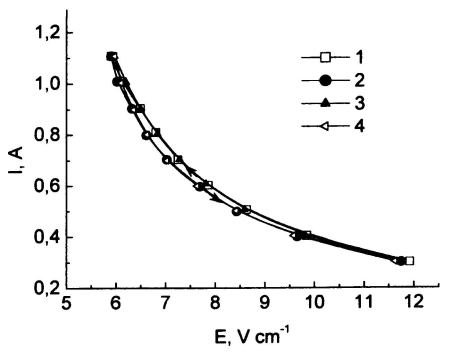

Figure 3 Hysteresis loop of CVC at two consecutive electric current increase-decrease cycles for ceramics $45VO_2$-15VPG-5Cu-$35SnO_2$: 1.3-current increase; 2.4-current decrease.

the current-voltage characteristics of VO_2-based ceramics after switching [5]. The filament border separates regions of the ceramics sample with different VO_2 phases. At thermodynamic equilibrium the temperature established on this border is equal to the temperature of metal-semiconductor phase transition T_t. With current increasing, an additional power dissipated in a sample leads to filament expansion, due to transition from semiconductor to metallic phase in VO_2 crystallites located near the filament border. With current decreasing, the decrease of dissipated power gives the narrowing of filament, as the result of reverse transition (from metallic phase to semiconductor phase) in VO_2 crystallites.

According to the existing opinions [8] the metal-semiconductor phase transition in VO_2 has martensite character. At such phase transition the mechanical stresses caused by transformation in crystal lattice have a significant role. From energy reasons such stresses are not advantageous for the coexistence of two VO_2 phases. Therefore, for formation of new phase nuclei and their growth, the deflection from energy of phase thermodynamic equilibrium is required. It gives a deviation from the equilibrium temperature of phase transition T_{t0} and leads to the temperature hysteresis of conductivity (Fig. 2).

For the description of temperature hysteresis at MSPT the coercive temperature ΔT may be introduced [8]. This temperature shows as far as it is necessary to deviate from the temperature of phase equilibrium T_{t0} for intensive development of phase transition. The temperature of transition from semiconductor to metallic state in VO_2 can be defined as $T_{t1} = T_{t0} + \Delta T_+$, in the reverse direction (from metallic to semiconductor state) as $T_{t2} = T_{t0} - \Delta T_-$ [8]. Generally the coercive temperatures for direct transition ΔT_+ and for the reverse transition ΔT_- are not equal. Only when hysteresis loop is symmetric, the equality $\Delta T_+ = \Delta T_- = \Delta$ T takes place. Expansion of the filament with electric current increasing is caused by transition in VO_2 from semiconductor to metallic state. The phase transition in VO_2 has reverse direction with electric current decreasing and this leads to narrowing of the filament. Because $T_{t1} > T_{t2}$ the temperature on filament border will be higher in the first case, than in the second case. Therefore to maintain the temperature T_{t1} more intensive power of electric current is required than it is required for the temperature T_{t2}. It explains the shift of CVC region with NDR to the higher electric intensity, when this region was registered at electric current increase (Fig. 1).

As shown in [5], when the threshold switching took place the current-voltage characteristic of VO_2-based ceramics may be described by dependence:

$$I = \frac{2\pi\lambda_S \Delta T_t E}{E^2 - E_0^2}, \tag{1}$$

where I and E are the electric current and the electric intensity, accordingly; $\Delta T_t = T_t$ -Q (T_t is the temperature of MSPT, Q is the ambient temperature); λ_S is the effective thermal conduction of ceramics material below T_t. The value E_0 in (1) is determined by expression:

$$E_0 = [6H\Delta T_t/(l\sigma_m)]^{1/2}, \tag{2}$$

where l is the thickness of the sample; H is the specific coefficient of a thermal dispelling; σ_m is the effective conductivity of VO_2-based ceramics above T_t. The expression (1) is correct, when the filament radius satisfies the condition $R \ll (2l\lambda_m/H)$ (where λ_m is the effective thermal conduction of ceramics material above T_t).

As it follows from expression (1) the electric current is proportional to ΔT_t at given E. Because $\Delta T_{t1} = T_{t1} - Q > \Delta T_{t2} = T_{t2} - Q$, the expression (1) explains the shift of CVC branch measured at electric current increase to higher values of current in comparison with CVC branch measured at electric current decrease (Figs. 1 and 3).

For the temperature dependences of conductivity and the radiant reflection of VO_2 films wider hysteresis loops (~15–20 K), than for VO_2 monocrystals (~2 K) take place [8, 11]. The reason of this is statistical distribution for equilibrium temperatures of phase transition T_{t0} and coercive temperatures ΔT of VO_2 crystallites from which the film consists. From the Fig. 2 it follows, that the hysteresis loop for temperature dependence of conductivity in VO_2-based ceramics is symmetrical and has width no more than 5–6 K. This magnitude is not much more than hysteresis loop width in VO_2 monocrystals. It testifies about a narrow enough distribution of the phase transition temperatures T_t for VO_2 crystallites in ceramics. Therefore in the first approximation it is possible to accept identical phase transition temperature T_0 and the coercive temperature T_c for all VO_2 crystallites in ceramics.

The relationship between T_0, T_c and parameters of CVC hysteresis may be determined if to write down the expression (1) as:

$$E^2 = E_0^2 + 2\pi\lambda_S \Delta T_t E/I\ . \tag{3}$$

Whence it follows, that the CVC high current region must be linear in coordinates $E^2 \sim E/I$. The line slope $k = \Delta(E^2)/\Delta(E/I) = 2\pi\lambda_S(T_t - Q)$ linearly depends from temperature T_t. If we take into account, that magnitudes k for the CVC branches, which are measured at electric current increase and decrease are equal $k_1 = 2\pi\lambda_S(T_0 + T_c - Q)$ and $k_2 = 2\pi\lambda_S(T_0 - T_c - Q)$,

TABLE I Parameters of the temperature hysteresis loop in VO_2-based ceramics

	Are calculated from current-voltage characteristic						Are defined from conductivity temperature dependence		
Ceramics composition (wt%)	k_1 (V·A·cm^{-1})	k_2 (V·A·cm^{-1})	$T_k/(T_0-Q)$	T_k (°C)	δT_t (°C)	T_0 (°C)	T_{t1} (°C)	δT_t (°C)	T_0 (°C)
$80VO_2$-15VPG-5Cu	1.55	1.37	$6.2\cdot10^{-2}$	3.1	6.2	68.9	72	5	70
$45VO_2$-15VPG-5Cu-$35SnO_2$	3.49	3.19	$4.5\cdot10^{-2}$	2.3	4.6	70.7	73	4	71

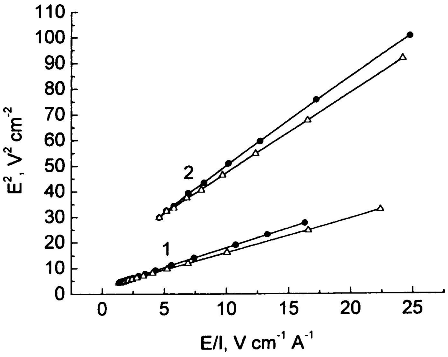

Figure 4 CVC high current regions in $E^2 \sim E/I$ coordinates for ceramics $80VO_2$-15VPG-5Cu (1) and $45VO_2$-15VPG-5Cu-$35SnO_2$ (2): points at current increase, triangles at current decrease.

accordingly, then we can find the ratio $T_c/(T_0 - Q)$ as:

$$\frac{T_c}{T_0 - Q} = \frac{k_1 - k_2}{k_1 + k_2}. \tag{4}$$

The doubled magnitude of this ratio defines the relative width of symmetric temperature hysteresis loop.

In coordinates $E^2 \sim E/I$ the high current regions of CVC are represented in Fig. 4. The linear character of dependencies takes place. It justifies the assumptions made above concerning temperatures T_0 and T_c. As one would expect, the slope of line in coordinates $E^2 \sim$ E/I for CVC branch registered at electric current increase is more than for branch registered at electric current decrease. The temperatures T_0 and T_c can be defined from CVC if the Equation 4 is used together with the equation $T_{t1} = T_0 + T_c$. The experimental magnitude of T_{t1} can be defined from the temperature dependences of specific electric resistance (Fig. 2). The branch of this dependence measured at temperature increase should be used in this case. Then from the expression (4) and the expression for T_{t1} we shall obtain:

$$T_c = \frac{1}{2}\left(1 - \frac{k_2}{k_1}\right)(T_{t1} - Q),$$

$$T_0 = \frac{1}{2}(T_{t1} + Q) + \frac{k_1}{2k_2}(T_{t1} - Q). \tag{5}$$

The temperatures T_{t1}, T_0 and the hysteresis loop width δT_t, which are determined from the temperature dependences of specific electric resistance (Fig. 2) are represented in the Table 1. The magnitudes of T_c, $\delta T_t = 2T_c$ and T_0 calculated from CVC, when the equations 5 was used are shown in the Table 1 also. The magnitude T_{t1} is defined from the temperature dependences of specific electric resistance in the average point of resistance jump. In the region of this point the temperature hysteresis loop width δT_t is determined. The magnitude of T_0 has been found as the temperature corresponding to the middle of the hysteresis loop.

Satisfactory conformity between the parameters, which are calculated from the current-voltage characteristic and which are found from the conductivity temperature dependences, takes place. It confirms, that the reason of hysteresis for CVC high current region in VO_2-based ceramics is the temperature hysteresis at metal-semiconductor phase transition in VO_2 crystallites.

4. Conclusions

After switching to high electric current, hysteresis of current-voltage characteristic in VO_2-based ceramics takes place. The hysteresis loop can be measured in electric current increase-decrease cycle.

The different temperatures for phase transition from semiconductor to metallic state and for the reverse phase transition are the reason for CVC hysteresis. Hysteresis appears after threshold switching, when both VO_2 phases coexist in the ceramics sample. VO_2 crystallites in metallic phase are located in the electric current filament. This filament is surrounded by VO_2 crystallites in semiconductor phase. When electric current increases the equilibrium temperature on the filament border is defined by transition from semiconductor to metallic phase of VO_2. This temperature is higher than the temperature of reverse transition from metallic to semiconductor phase. Such temperature is being established on the filament border when electric current decrease. In the first case to maintain the thermal equilibrium, higher power of electric current is required than in the second case. It is the reason of CVC region shift measured at electric current increase to higher electric intensity in comparison with the similar CVC region measured at electric current decrease.

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