J Mater Sci (2018) 53:15549–15558

Electronic materials

Design of electrical probe memory with TiN capping layer

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Received: 23 May 2018
Accepted: 13 July 2018
Published online: 17 July 2018

ABSTRACT

The concept of electrical probe memory using phase-change media has recently received considerable attention due to its promising potential for next-generation data storage device. However, the physical performances of the conventional electrical probe memory are strongly limited by its diamond-like carbon capping layer ascribed to its large contact resistance and sharp difference between the theoretically optimized properties values and the experimentally measured values. Therefore, the diamond-like carbon capping layer is replaced by a titanium nitride layer here, and the modified device architecture is re-optimized by a newly developed three-dimensional model, resulting in a media stack consisting of a 2-nm $Ge_2Sb_2Te_5$ layer sandwiched by 2-nm titanium nitride layer with an electrical conductivity of $2 \times 10^5\ \Omega^{-1}\ m^{-1}$ and a thermal conductivity of 12 W m^{-1} K^{-1}, and a 40-nm titanium nitride bottom layer with an electrical conductivity of $2 \times 10^6\ \Omega^{-1}\ m^{-1}$ and a thermal conductivity of 12 W m^{-1} K^{-1}. The advantageous features of such a device on the writing of both crystalline and amorphous bits are also demonstrated according to the developed model.

Introduction

Electrical probe memory that makes use of a nanoscale conductive probe as the recording tool and a thin chalcogenide (e.g., $Ge_2Sb_2Te_5$) layer as the recorded media, has received extensive attention due to its prospective potential for next-generation mass storage device [1]. The recording process is achieved by injecting a write current via the conductive probe into the chalcogenide layer that is either heated to the crystalline temperature to form crystallization, or to the melting temperature followed by a rapid quench to generate amorphization. The replay process is realized by applying a write voltage to the chalcogenide layer to detect the resulting current difference arising from the large resistivity contrast between crystalline and amorphous phases. Such principles are schematically shown in Fig. 1.

As the focused region of write current on the chalcogenide layer is restricted by the conductive probe, the size of the recorded bit that represents the areal density of the device is closely related to the diameter of the probe tip, meaning that use of an ultra-small probe tip would possibly enable ultra-

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https://doi.org/10.1007/s10853-018-2707-4

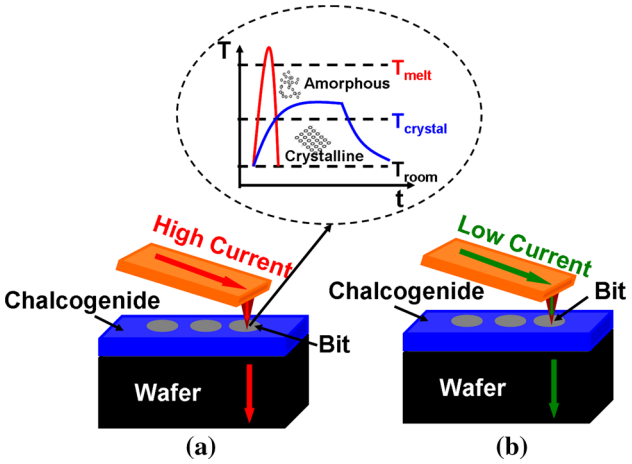

Figure 1 Electrical probe memory using chalcogenide alloy operated in **a** write mode and **b** read mode. The inset shows the phase-transformation principle of the chalcogenide alloy between amorphous and crystalline phases where T, t, T_{melt}, $T_{crystal}$, and T_{room} indicate temperature, time, melting temperature, crystalline temperature, and room temperature, respectively.

high recording density. Additionally, inherent characters of the chalcogenide alloy (e.g., fast switching speed, great stability at room temperature, and relatively low crystalline temperature) endow electrical probe memory with several advantageous performances such as high data rate, long data retention time, and low energy consumption. Because of the above reasons, considerable research effort in perspective of either simulation or experiment is dedicated to the design and optimization of the layered geometry and electrothermal properties of the electrical probe memory [2–5]. The current consensus is that an optimized storage media stack is made up of a $\sim$ 10-nm $Ge_2Sb_2Te_5$ (GST) layer sandwiched by a $\sim$ 2-nm diamond-like carbon (DLC) capping layer with an electrical conductivity of $\sim$ 100 Ω^{-1} m^{-1} and a thermal conductivity of $\sim$ 0.5 W m^{-1} K^{-1}, and a $\sim$ 40-nm titanium nitride (TiN) bottom layer with an electrical conductivity $\sim 5 \times 10^6$ Ω^{-1} m^{-1} and a thermal conductivity of $\sim$ 12 W m^{-1} K^{-1}, deposited on silicon (Si) wafer, while a silicon dioxide (SiO_2) encapsulated Si tip with platinum silicide (PtSi) with an electrical conductivity of $\sim 3.3 \times 10^6$ Ω^{-1} m^{-1} at the tip apex is adopted as the conductive probe, as illustrated in Fig. 2.

It was previously reported that capping layer not only can protect GST layer from wear and oxidation, but also serves as a conductive bridge to connect the probe and the GST layer [3]. As a result, the electrical conductivity of the capping layer is required to be relatively high so as to reduce the whole device resistance and thus to lower the energy consumption per bit, whereas its thermal conductivity needs to be low in order to maintain sufficient Joule heating inside the GST layer. Thanks to this, DLC thin film with aforementioned geometrical and electrothermal properties seems to be an appropriate choice and has been extensively implemented in both theoretical simulations and practical fabrications. However, recent experimental evidences reveal that the electrical conductivity of the DLC thin film is approximately proportional to its thickness [6], clearly suggesting that the optimized electrical conductivity of $\sim$ 100 Ω^{-1} m^{-1} can only be achieved with a thickness exceeding 30 nm that cannot be adopted in practice due to its large resistance [7, 8]. Besides, the previous optimization design ignored the existence of the electric contact resistance between the conductive probe and the DLC capping layer, which depends on the electrical resistivity of the interfacial materials (PtSi and DLC here) as well as the contact area, given by [9]:

$$R_{con} = \frac{\rho_{tip} + \rho_{cap}}{4r_{con}} \quad (1)$$

where R_{con} is the contact resistance at tip–capping interface; ρ_{tip} and ρ_{cap} are the resistivities of the conductive probe and the capping layer, respectively; r_{con} is the contact radius that strongly pertains to the applied force, Young's modulus, and the tip apex [9]. Therefore, combining the aforementioned electrical conductivities values with a tip apex of $\sim$ 10 nm targeted for multi-Tbit/in^2 density gives rise to a contact resistance of $\sim$ 80 kΩ [3]. Such contact resistance would drastically increase the device resistance and consequently cause much more energy consumption per bit when compared with the device with low contact resistance. As the probe tip needs to be highly conductive, the sole approach to reduce the contact resistance is to take advantage of a capping media whose electrical conductivity value is close to that of the probe tip (note that in order to sustain ultra-high density, it is not desiring to increase the tip apex). Owing to above factors, the requirement to search for an optimum capping media simultaneously having high electrical conductivity and thin thickness becomes imperative.

As TiN has been considered as an optimum material for bottom electrode of the electrical probe

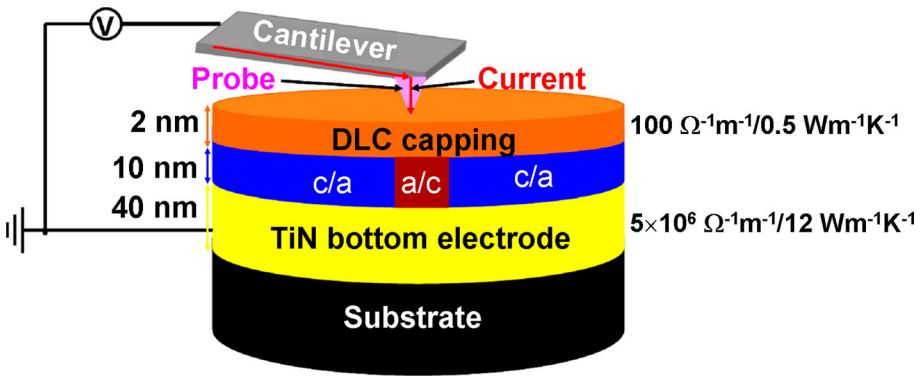

Figure 2 The design of an optimized electrical probe memory.

memory [6], it is natural to conceive the possibility of using TiN for the capping material. According to its electrothermal properties, TiN media exhibit an ultra-high electrical conductivity comparable to that of the PtSi tip, and a fairly low thermal conductivity, which thus allows for ultra-low contact resistance at tip–capping interface, and to possibly sustain adequate Joule heating inside the GST layer for a low electric excitation. Additionally, good adhesion between GST and TiN has been observed at the atomic scale [10], and no evidence of a reaction between TiN and GST has been reported to date. More importantly, the feasibility of using TiN as the top electrode to electrically switch the GST cell with a TiN/GST/TiN structure has already been demonstrated [11]. In this case, the role of the TiN capping material in determining the write/read performance of the electrical probe memory becomes very intriguing and is worth detailed investigation.

Model

A previously developed pseudo-3D model [2] was expanded to full 3D here to imitate the electrical, thermal, and phase-change processes of the GST media inside the electrical probe memory when subjected to external electric stimulus. The designed geometry consists of a SiO_2 encapsulated Si tip with PtSi at tip apex of $\sim$ 10 nm, and a trilayer stack comprising a 10-nm GST layer sandwiched by a TiN capping and a TiN bottom layers, deposited on Si substrate. The resultant geometrical mesh with free tetrahedral shape is created in a so-called swept manner, giving rise to a total number of 184996 elements. Such a model consists of a set of coupled equations including the Laplace equation [12], heat conduction equation [13], and rate equation [14] to calculate current density (or electric field), temperature, and phase transformation extent, respectively, defined by:

$$\nabla \cdot (\sigma \cdot \nabla V) = 0, \tag{2}$$

$$\rho C_{\mathrm{p}} \frac{\partial T}{\partial t} - k \cdot \nabla^2 T = \sigma |E|^2, \tag{3}$$

$$\frac{\partial \chi}{\partial t} = A_{\mathrm{c}} (1-\chi)^n \exp\left(\frac{-E_{\mathrm{c}}}{k_{\mathrm{B}} T}\right), \tag{4}$$

where V is the electric potential, σ is the electrical conductivity, ρ is the density, C_{p} is the heat capacity, T is the temperature, k is the thermal conductivity, E is the electric field, χ is the crystal fraction, A_{c} is the pre-factor, n is the reaction order, E_{c} is the height of the energy barrier for crystallization, and k_{B} is the Boltzmann's constant. It should be noticed that the critical electric field for the well-known threshold switching and the electrical conductivity of the amorphous GST that were previously defined by an empirical model [2, 3] are re-described here based on multiple trapping transport together with 3D Poole–Frenkel emission from a two-center Coulomb potential, given by [15]:

$$E_t = \frac{\beta^2}{(es)^2}, \tag{5}$$

$$\sigma_{LE} \approx \frac{2K\mu k_{\mathrm{B}} T}{Es} \exp\left(\frac{-E_a}{k_{\mathrm{B}} T}\right) \sinh\left(\frac{eEs}{2k_{\mathrm{B}} T}\right), \tag{6}$$

$$\sigma_{HE} \approx K\mu e \frac{k_{\mathrm{B}} T}{\beta E^{1/2}} \left(1 - \frac{k_{\mathrm{B}} T}{\beta E^{1/2}}\right) \exp\left(-\frac{E_a - \beta E^{1/2} + \frac{\beta^2}{es}}{k_{\mathrm{B}} T}\right), \tag{7}$$

where E_t is the critical electric field for threshold switching; $\beta = e^2/\sqrt{e\pi\varepsilon_{\mathrm{r}}\varepsilon_0}$ is the Pool–Frenkel constant with ε_0 as the vacuum permittivity, e as the electronic charge and ε_{r} as the relative high-frequency

dielectric constant; σ_{LE} is the electrical conductivity of the amorphous GST when $E < E_t$; K is a pre-factor; $\mu = \mu_0/\sqrt{1+(\mu_0 E/v_{sat})^2}$ is the free carrier mobility with μ_0 as the low-field mobility and v_{sat} as the saturation velocity; σ_{HE} is the electrical conductivity of the amorphous GST when $E \geq E_t$; E_a is the low-field temperature-dependent activation energy, given by [16]:

$$E_a = E_{a_0} - \frac{aT^2}{b+T}, \tag{8}$$

where E_{a0}, a, and b are constant values obtained from dedicated measurements in the ohmic regime. Accordingly, the electrical conductivity of the amorphous GST (σ_{am}) in the modified model is defined by:

$$\sigma_{am} = \sigma_{LE}(E < E_t) + \sigma_{HE}(E \geq E_t), \tag{9}$$

The electrical conductivity of the crystalline GST is defined in a similar manner to the previous model, given by:

$$\sigma_{cryst} \approx \sigma_{0cryst} \exp\left(-\frac{E_C}{k_B T}\right), \tag{10}$$

where σ_{0cryst} is a pre-factor and E_c is the activation energy for crystallization. Based on the above descriptions, the spatial distribution of the electrical conductivity in the GST layer during crystallization is described by:

$$\sigma_{GST} = \sigma_{cryst} \cdot \chi + \sigma_{am} \cdot (1-\chi), \tag{11}$$

The thermal conductivity of the GST during the crystallization also depends on the crystallization extent and is given by:

$$K_{GST} = K_{cryst} \cdot \chi + K_{am} \cdot (1-\chi), \tag{12}$$

In order to achieve amorphization, the GST needs to be heated above melting temperature ($\sim$ 620°C), followed by a rapid cooling (cooling rate $\geq$ 37°C/ns). Therefore, during the simulation the GST region where the two aforementioned conditions are simultaneously fulfilled will be assumed to be amorphized. Accordingly, the electrical conductivity and the thermal conductivity of the GST region during the amorphization are depicted, respectively, by:

$$\sigma_{GST} = \sigma_{am} \cdot (T \geq 620\,^\circ\mathrm{C}) \cdot (T_t \geq 37\,^\circ\mathrm{C/ns}) + \sigma_{cryst} \cdot ((T < 620\,^\circ\mathrm{C}) \| (T_t < 37^\circ\mathrm{C/ns})), \tag{13}$$

$$K_{GST} = K_{am} \cdot (T \geq 620\,^\circ\mathrm{C}) \cdot (T_t \geq 37\,^\circ\mathrm{C/ns}) + K_{cryst} \cdot ((T < 620\,^\circ\mathrm{C}) \| (T_t < 37^\circ\mathrm{C/ns})), \tag{14}$$

where T_t is the cooling rate.

To mimic the phase-transformation process, the Laplace equation is solved to provide the electric field and the current density that are considered as the heat source terms inside the heat conduction equation that aims to offer temperature distribution inside the GST layer. The consequent temperature is subsequent implemented to calculate the crystallization/amorphization extent based on the rate equation. It should be kept in mind that as the electrothermal properties of the GST media strongly depend on its electric field, temperature, and phase-transformation extent, Eqs. (2)–(14) need to be solved simultaneously in order to accurately describe the phase-transformation mechanisms of the GST alloy. During the simulation, an electric excitation is applied to the top boundary of the tip, whereas the bottom boundary of the TiN bottom electrode is ground. These two boundaries also remain at room temperature, while other boundaries are set to be electrically or thermally insulated. The time period for each simulation is set the same as their respective pulse width, and a time-dependent directive solver is used to ensure model convergence. All the calculations were performed using COMSOL MULTIPHYSICS™ based on finite-element method.

Results

To accurately assess the role of the TiN capping layer in the writing and readout performances of the electrical probe memory, the range of the possible values of the geometrical and electrothermal properties of the thin TiN layer obtained from different deposition techniques needs to be established. It was previously reported that (DC) magnetron sputtering method or ion-beam-assisted method is responsible for fairly thick TiN films [17–20], while atomic layer deposition (ALD) approach is usually employed to fabricate an ultra-thin TiN layer with a thickness down to 0.65 nm [21]. Within the aforementioned thickness range, the electrical conductivity of the TiN layer was found to vary strongly as a function of the deposition methods and the layer thickness, resulting in Fig. 3.

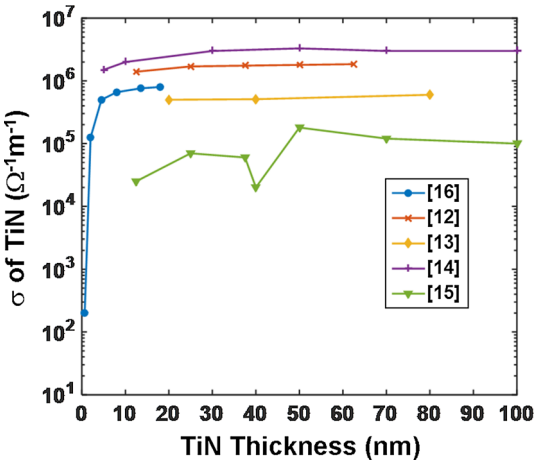

Figure 3 The electrical conductivity of TiN films with respect to its thickness for different deposition techniques.

As clearly shown in Fig. 3, the TiN layer with a thickness ≥ 2 nm exhibits an electrical conductivity ranging from 2×10^4 to $2 \times 10^6\ \Omega^{-1}\ m^{-1}$, while its electrical conductivity suddenly decreases to $200\ \Omega^{-1}\ m^{-1}$ when its thickness is below 2 nm. Such a drastic drop for resistivity of the TiN layer < 2 nm may arise from the increasing role of grain boundary and interface scattering effects [21]. Compared with the electrical conductivity, the thermal conductivity of the TiN layer is almost independent of its thickness and the deposition methods, which was experimentally measured to be $\sim 12\ W\ m^{-1}\ K^{-1}$ [22].

Based on the geometrical/physical properties shown above, the influence of the TiN capping layer on the writing performance of the electrical probe memory is investigated by calculating the maximum temperature inside the GST layer without accounting for phase transformation as a function of the thickness and the electrical/thermal conductivities of the TiN capping layer attained from Fig. 3 for cases of both crystallization and amorphization, giving rise to Fig. 4.

It should be noticed that for accessing crystallization temperature, the initial phase of the GST layer is considered amorphous with an electrical conductivity given by Eq. (9) and a thermal conductivity of $0.2\ KW^{-1}\ m^{-1}$, while for calculating amorphization temperature, Eq. (11) and $0.58\ W\ m^{-1}\ K^{-1}$ are introduced to represent the electrical conductivity and the thermal conductivity of the crystalline GST. Note that the TiN layer with a thickness < 2 nm shows a similar electrical conductivity to that of the DLC capping, thus inducing a high contact resistance. Additionally, due to its fairly large thickness, the TiN layer with a thickness > 10 nm also generates a large material resistance. These two extreme cases are therefore not taken into account here, and the contact resistance between tip and TiN capping layer, calculated by Eq. (1), is introduced into simulations to more closely mimic the practical setup, which varies from 53 Ω to 3.3 kΩ with a tip force of 300 nN (typical for that applied during writing) and an effective Young's modulus of 115 GPa. Tables 1 and 2 summarize the characteristic parameters and modeling parameters used, respectively.

As can be seen from Fig. 4, the maximum temperature inside the GST layer during crystallization (*located at the top of the GST layer and directly under the tip*) varies from 350 to 650 °C by changing the electrical conductivity of the TiN capping from 2×10^4 to $2 \times 10^6\ \Omega^{-1}\ m^{-1}$, and the thickness from 2 nm to 10 nm. It is obvious that for a given electrical conductivity, the use of a thicker capping layer results in a decrease in the maximum temperature inside the GST layer, which is expected that the thicker layer causes a larger device resistance and thus reduces the Joule heating. In spite of this undesired finding, the required crystallization temperature within nanosecond regime ($\sim$ 400 °C) can be achieved even using a 9-nm-thick TiN capping, which cannot be reproduced by the previous DLC capping with the same thickness [2]. This is because, in addition to the thickness, the resistance of the TiN capping is also strongly governed by its electrical conductivity. As a result, the designed architecture with a fairly thick TiN capping still enables a low device resistance due to its super-high electrical conductivity and consequently generates sufficient Joule heating for the required phase transformation. Moreover, for a given capping layer thickness, varying the electrical conductivity of the TiN capping has a negligible effect on the maximum temperature inside the GST layer. This arises from a fact that within the aforementioned electrical conductivity range, the resistance of the TiN capping is much smaller than that of the amorphous GST layer that thus dominates the whole device resistance as well as the writing energy.

Similar to the crystallization case, the maximum temperature inside the GST layer during amorphization changes from 500 to 1000 °C with a thickness and an electrical conductivity of the capping layer from 2 to 10 nm and from 2×10^4 to $2 \times 10^6\ \Omega^{-1}\ m^{-1}$, respectively. Additionally, the use

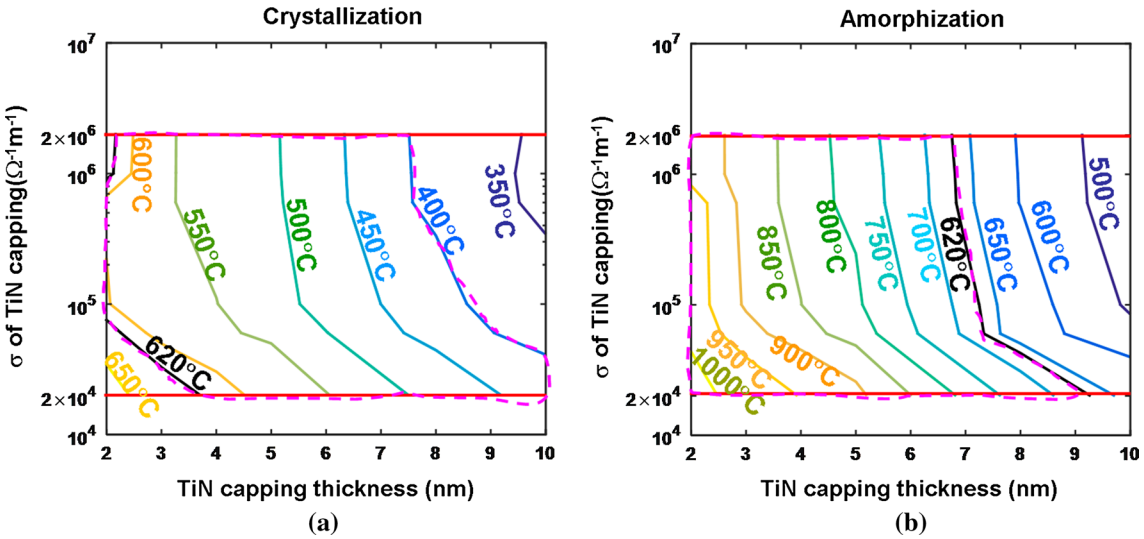

Figure 4 Maximum temperature inside the GST layer as a function of the electrical conductivities and thickness of the TiN capping layer for **a** crystallization and **b** amorphization. The applied pulses are set to be a 5.5 V of 180 ns for crystallization and a 6.5 V of 150 ns for amorphization, respectively; the thickness of the GST layer is 10 nm, while the electrical conductivity and the thickness of the TiN bottom layer are chosen to be $2 \times 10^6\ \Omega^{-1}\ m^{-1}$ and 40 nm, respectively. The investigated electrical conductivity range of the TiN capping layer is bounded by two red lines, while the resulting optimized regions are encompassed by the violet dashes.

Table 1 Characteristic parameters used in simulations

Parameter	Tip	TiN capping	GST	TiN bottom	Si
Thickness (nm)	10	2–10	2–30	10–50	1000
ρ (Kg m^{-3})	12400	5400	6150	5400	2330
C_p (J Kg^{-1} m^{-3})	250	2.2×10^6	210	2.2×10^6	720
K (W m^{-1} K^{-1})	25	12	Eq. (14)	12	149
σ (Ω^{-1} m^{-1})	3.3×10^6	2×10^4–2×10^6	Eq. (13)	2×10^4–2×10^6	N/A

Table 2 Modeling parameters used in simulations

Material	s (nm)	E_{a0} (eV)	K μ_0 (m^{-1} V^{-1} s^{-1})	σ_{0cryst} (Ω^{-1} m^{-1})
GST	8.3	0.343	2.6×10^{22}	1.5×10^4

of a thicker TiN capping layer results in a lower maximum temperature inside the GST layer, and the resulting maximum temperature is almost independent of the electrical conductivity of the capping layer for a given thickness, both matching the previous observations for the crystallization case. It is informative to notice that the designed probe device should be suitable for the writing of both crystalline and amorphous bits. To achieve crystallization within nanosecond regime, the temperature inside the GST layer must exceed ~ 400 °C, while lower than ~ 620 °C to avoid re-amorphization. Such a temperature range can be realized, according to Fig. 4a, by selecting the thickness and the electrical conductivity of the TiN capping layer from 2 to 9 nm, and from 10^5 to $2 \times 10^6\ \Omega^{-1}\ m^{-1}$, respectively. For amorphization, the temperature inside the GST layer needs to be heated up to ~ 620 °C within the nanosecond regime, which can be accomplished using a thickness and an electrical conductivity of the TiN capping layer from 2 to 9 nm, and from 2×10^4 to $2 \times 10^6\ \Omega^{-1}\ m^{-1}$, respectively, as reflected from Fig. 4b. As a result, the architecture configurations with a thickness and an electrical conductivity of the TiN capping layer from 2 to 9 nm, and from 10^5 to $2 \times 10^6\ \Omega^{-1}\ m^{-1}$, respectively, seem to meet temperature requirements for both crystallization and amorphization. However, a thin TiN capping layer is

always preferable in order to significantly lower the resulting energy consumption. Considering this demand in conjunction with the practical electrothermal properties of the TiN thin film depicted in Fig. 3, the thickness, the thermal conductivity, and the electrical conductivity of the TiN capping layer are optimized here to be 2 nm, 12 W m^{-1} K^{-1}, and 2×10^5 Ω^{-1} m^{-1}, respectively.

As the thickness of the GST layer determines the required threshold voltage that heavily affects the energy consumption, it also plays a critical role in the maximum temperature induced in the GST layer, which was rarely studied in previous literature. Therefore, we here re-investigate the maximum temperature inside the GST layer by varying its thickness from 2 nm (the minimum thickness obtained experimentally to date) [23] to 30 nm (the optimized thickness in the previous literature [2]) for different crystallization and amorphization pulses. It should be kept in mind that the resulting crystalline bit is required to extend through the whole GST thickness to generate discernible readout signal. Thanks to this, the maximum temperature at the top (point A in the inset of Fig. 5) and the bottom of the GST layer (point B in the inset of Fig. 5) that is directly underneath the tip is calculated during the pulses periods, as clearly indicated in Fig. 5. According to Fig. 5a, higher pulse magnitudes lead to an enhancement of the maximum temperature at both point A and point B for a given GST thickness, obviously owing to the increase in the writing energy. Additionally, for a fixed pulse magnitude, the maximum temperature at point A is approximately independent of the thickness of the GST layer, whereas a thicker GST layer can dramatically reduce the maximum temperature at point B. It is evident that point A coincides with the location where the maximum temperature in the device occurs due to the small interface between tip and TiN capping that allows for the highest current density in the device; in this case, variation of the GST layer thickness can slightly affect the consequent current density at the interfacial region and therefore has negligible effect on the maximum temperature at point A. However, increasing the thickness of the GST layer would strongly attenuate the heat penetration depth, whereby the bottom of the GST layer where point B is located can not be heated sufficiently, thus resulting in a decrease in the maximum temperature at point B.

The maximum temperature at A and B during amorphization, as illustrated in Fig. 5b, shows a similar dependence on the GST layer thickness and the adopted write pulse to the crystallization case. For a given pulse magnitude, a slight increase in the maximum temperature at A was found when using a thicker GST layer, which is expected that the thicker layer further separates point A from the substrate that is commonly considered as a heat sink, thus

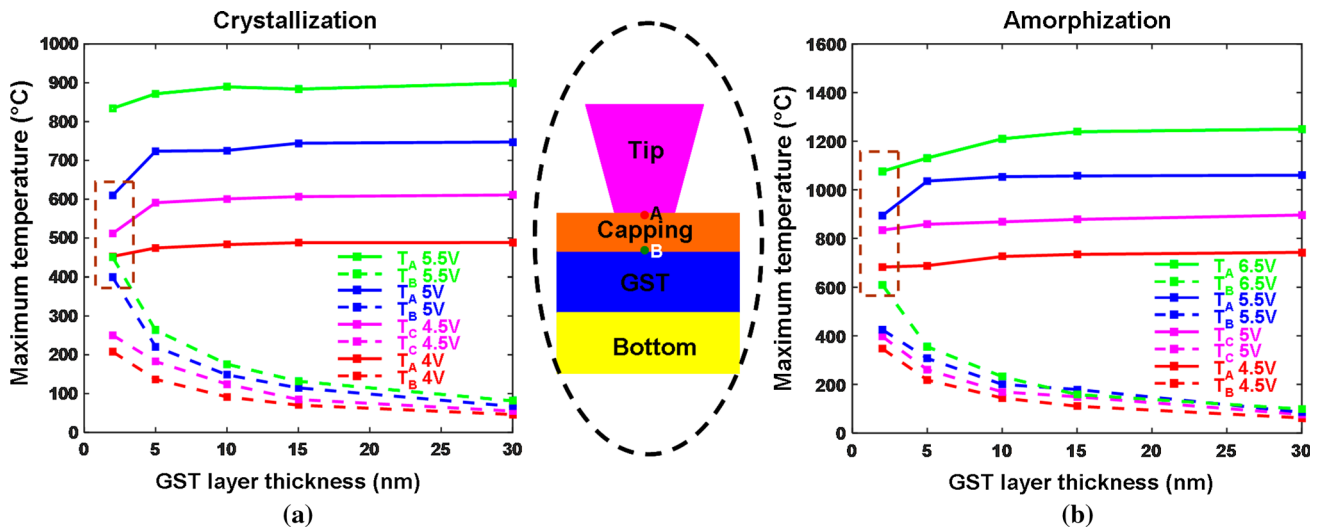

Figure 5 Maximum temperature at points A and B as a function of the applied pulse and thickness of the GST layer for **a** crystallization and **b** amorphization. The electrical conductivity and the thickness of the TiN capping and TiN bottom layers are fixed to be 2×10^5 Ω^{-1} m^{-1}, 2 nm, and 2×10^6 Ω^{-1} m^{-1}, 40 nm, respectively. The inset shows the cross section of the modeled geometry where points A and B are defined, and the optimized regions are bounded by the dark red dashes.

heavily suppressing the possible heat dissipation toward the substrate. In contrast to point A, the maximum temperature at point B is strongly reduced by increasing the thickness of the GST layer due to the weakening of the heat penetration effect. Based on the results presented so far, the configuration with a 2-nm GST layer and a crystallization pulse of 5.5 V is the only option that enables a crystalline bit extending through the whole thickness. (The temperature at A and B meets the aforementioned requirements for crystallization.) Besides, the use of a 2-nm-thick GST layer associated with an amorphization pulse of 6.5 V also leads to an amorphous bit through the whole GST layer. (But it is not compulsorily needed [24].) As a result, the thickness of the GST layer here is optimized to be 2 nm, and the writing pulses for crystallization and amorphization are chosen to be 5.5 and 6.5 V, respectively.

In addition to capping and GST layers discussed above, the TiN bottom electrode is mainly served to collect the write current and is therefore likely to affect the write performances of the designed device. Hence, we vary the thickness of the TiN bottom electrode from 10 to 50 nm and calculate the corresponding maximum temperature at points A and B for both crystallization and amorphization, resulting in Fig. 6.

Note that the electrical conductivities of the TiN bottom layer for different thicknesses were adapted from [19], and other characteristic parameters such as

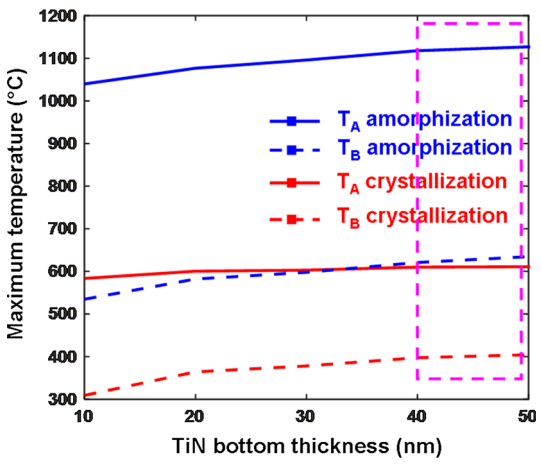

Figure 6 Maximum temperature at points A and B as a function of the thickness of the TiN bottom layer. The electrical conductivity and the thickness of the TiN capping layer are set to be $2 \times 10^5\ \Omega^{-1}\ m^{-1}$, 2 nm, and a 2-nm-thick GST layer is adopted here. The optimized region is bounded by the violet dash.

the geometric and electrothermal properties of the TiN capping, the thickness of the GST layer, and the employed write pulses are directly secured from the aforementioned optimization study. According to Fig. 6, the resulting maximum temperature at points A and B during either crystallization or amorphization slightly rises up by increasing the thickness of the TiN bottom layer, readily owing to the further division of the GST layer from the Si substrate. However, such a temperature variation is not as pronounced as that caused by the capping layer, which is expected that the resistance of the TiN bottom layer is much smaller than that of the GST media and thus has a minor influence on the whole device resistance as well as on the consequent Joule heating. For the above reasons, the optimized thickness of the TiN bottom layer is still designed to be 40 nm here.

Discussions

Based on the above descriptions, the designed electrical probe memory with an introduction of the TiN capping layer comprises a 2-nm GST layer sandwiched by a 2-nm TiN capping layer with an electrical conductivity of $2 \times 10^5\ \Omega^{-1}\ m^{-1}$ and a thermal conductivity of $12\ W\ m^{-1}\ K^{-1}$, and a 40-nm TiN bottom layer with an electrical conductivity of $2 \times 10^6\ \Omega^{-1}\ m^{-1}$ and a thermal conductivity of $12\ W\ m^{-1}\ K^{-1}$, all of which are deposited on Si wafer. To investigate its write performances, the feasibility of using such a device to write either crystalline bits or amorphous bits is assessed here by means of the aforementioned 3D computational model. The correlated write pulses for crystallization and amorphization are set to be a 5 V of 180 ns (40-ns rising edge, 100-ns plateau, and 40-ns trailing edge), and a 6.5 V of 150 ns (40-ns rising edge, 90-ns plateau, and 20-ns trailing edge), respectively, while the contact resistance introduced at the tip–capping interface is calculated to be $\sim$ 350 Ω with mechanical properties introduced above, which can be ignored when compared with the whole device resistance. The formed crystalline bit with a diameter of $\sim$ 10 nm, as illustrated in Fig. 7a, exhibits a cylindrical shape that extends through the whole GST thickness, thereby allowing for a noticeable readout signal with $\sim$ 10 Terabit/inch^2 areal density. Additionally, the presence of the low contact resistance enables the formation of a crystalline bit by a write

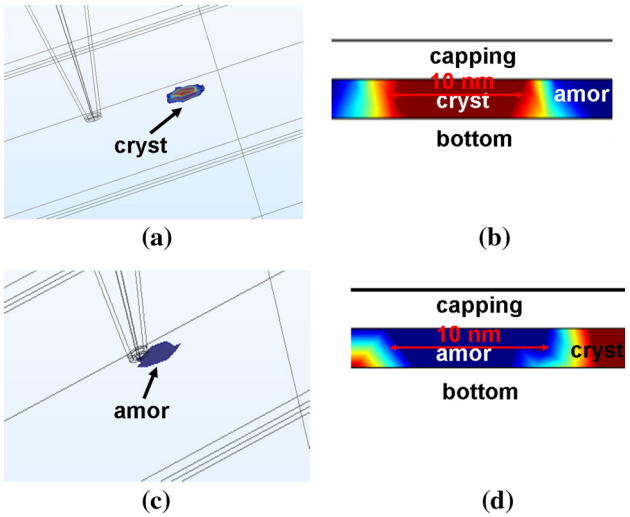

Figure 7 The resulting crystalline bit in its **a** 3D view, and **b** cross-sectional view, and the resulting amorphous bit in its **c** 3D view, and **d** cross-sectional view, from the newly devised structure with TiN capping layer.

energy of ~ 0.12 pJ within a pulse duration of 180 ns, corresponding to an ultra-high date rate of 10^7 bit s^{-1} per tip and an ultra-low energy consumption within fJ regime. The formed amorphous bit that also extends through the whole GST thickness is found to have an elliptical shape and a diameter of ~ 10 nm, attractively providing ultra-high density recording capability. Although the resulting write energy per amorphous bit is somewhat higher (~ 0.2 pJ per bit) than the crystallization case due to the applied amorphization pulse, this newly devised architecture with TiN capping layer is able to write amorphous bit within ns regime, while at the expense of much lower write energy than the counterpart with DLC capping layer [3], thus making it greatly suitable for the next-generation data storage device.

Conclusions

A physical-realistic pure 3D numerical model was developed to assess the phase-transformation temperature of the electrical probe device having a TiN capping layer by tailoring the geometrical and electrothermal properties of each layered stack. The designed device is therefore optimized to comprise a 2-nm GST layer sandwiched by a 2-nm TiN capping layer with an electrical conductivity of $2 \times 10^5\ \Omega^{-1}\ m^{-1}$ and a thermal conductivity of 12 W m^{-1} K^{-1}, and a 40-nm TiN bottom layer with an electrical conductivity of $2 \times 10^6\ \Omega^{-1}\ m^{-1}$ and a thermal conductivity of 12 W m^{-1} K^{-1}, deposited on Si substrate. The capability of using such a device to provide ~ 10 Tbit/in^2 density, ~ ns data rate, ~ fJ write energy, and ultra-low interfacial contact resistance for both crystallization and amorphization processes was also demonstrated according to the correlated simulations.

Acknowledgements

We gratefully acknowledge the financial supports of the Natural Science Foundation of Jiangxi Science and Technology Department (Grant No. 20151BAB217003) and the Foundation of Jiangxi Education Department (Grant No. GJJ170598).

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