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Low-Power Area-Efficient Fault Tolerant Adder in Current Mode Multi Valued Logic Using Berger Codes

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Abstract
In this paper, we propose a low-power yet area-efficient fault tolerant adder by using Berger codes. The proposed Berger code checker is designed by using the current mode multi-valued logic (CM-MVL) circuits. The proposed structure, which is more area and power efficient than state-of-the-art fault tolerant adders, is able to detect all single and multi-bit unidirectional faults. The efficiency of the proposed fault tolerant adder is evaluated by comparing its characteristics to those of two state-of-the-art fault detection schemes in adders as well as the conventional duplex and parity bit checkers in a 90 nm technology. The results reveal that the proposed 64-bit Berger code checker for adders imposes up to 6.7% and 27.2% delay and area penalties, respectively with a cost of static power dissipation. In the proposed scheme, in sub threshold regime, the power penalty is just 1%, while its area overhead is only 31%. The drawback of using this scheme in sub threshold regime is that delay time introduced to the circuit is unacceptable. So, depending on the application, we should choose one of the above-mentioned schemes.

Keywords Fault tolerant adder, Berger code checker, Current mode, Multi-valued logic

1 Introduction

With the advancement and development of VLSI circuits by shrinking the device feature sizes, an increase in the number of faults is observed. This is because smaller technologies are more susceptible to defects and smaller particles like cosmic rays. So, as technology scales, fault tolerance is becoming a key concern especially in critical applications.

This paper intends to propose an area-efficient checker circuit to detect faulty states in adders. In the proposed scheme, Berger codes are used to detect a faulty state. Although the theory of using Berger codes for adders has been already investigated, however an efficient and practical scheme has not been yet proposed. Berger code is a unidirectional error detecting code which is introduced by J. M. Berger [2]. This coding scheme is basically introduced and used in telecommunication, but later, it was used as error detection mechanism in the arithmetic circuits and other digital circuits [9, 10]. Recently, a fault tolerant FIR filter using Berger codes [16, 18] and a Berger code based self-testing processors have been introduced in [1]. More details can be found in [1, 2, 9, 16]. In this paper, by using the simple current mirrors and a differential topology which are similar to current mode multi valued logic, a novel Berger code checker circuit is presented for "adders".

Multi valued logic (MVL) has a long and rich history, and it has had a great influence on developments of many circuits and systems [4] [19]. In current-mode MVL, current is used to represent logical levels which is an integer multiple of a reference current [3]. The first studies of Current-mode MVL was carried out in the 1960s [6, 14], and in references [12, 20] it is used for fault detection purposes.

The main contributions of this paper can be summarized as follows: •A very low power Berger code checker for adders has been proposed in sub-threshold regime. •The proposed scheme using the pseudo differential structure automatically tolerates the current mirrors errors. •In comparison with the latest work for fault detection in adder circuits, in 64-bit adder, approximately 30% area overhead and for sub-threshold deign 1% power penalty has been achieved.

The rest of this paper is organized as follows. The structure of the proposed fault tolerant adder is described in Section 2. The efficiency of the proposed adder and the results are

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discussed in Section 3. Finally, this paper is concluded in Section 4.

1.1 Proposed Scheme

The basic structure of a Berger checker is depicted in Fig. 1. In this architecture, the main building block is the 1's counter unit which is replicated four times. The major portion of the area is occupied by this block, for 9-bit data, as illustrated in [15], seven full adders (FA) are required to calculate the Berger codes. This means that a conventional Berger checker for an 8-bit adder requires 28 FAs in the Berger code generators, i.e. 1's counter unit. Moreover, a 4-bit adder and comparator are also needed to detect a faulty state. While, for an 8-bit adder just eight full adders are required, when the arithmetic operation is simple like an addition, Berger codes for error detection purposes are inefficient. When a sophisticated digital system such as an arithmetic and logical unit (ALU) [9] or a processor [10] is used, since the building blocks are shared, the area penalty will be negligible. Also, a modified Berger code for DRAM Repair methods provides an acceptable result [15]. The original works to implement a Berger checker are given in [13, 17], [5]. The checker given in [5] has this advantage that it requires less area and higher speed feature than the checkers proposed in [13, 17]. However, as stated in [8], checkers proposed in [5] have static power consumption. The scheme proposed in [8], has significantly lower power consumption than the checkers given in [5]. Main challenge is the 1's counter unit, which sums up the '1' bits in the operands. In contrast to binary logic, in which the add operation requires some logical resources such as half adders and full adders, the linear summation in the current mode MVL can be performed simply by wiring without using any active device. This attractive feature of CM-MVL logic circuits is the main motivation to propose a novel Berger checker circuit for small operations such as additions. However, the static power issue in the current mode logic, its design complexities, especially in the ultra-sub-micron technologies and mixed analog digital design are the main challenges. An initial structure of fault tolerant adder based on Berger codes using the current mode MVL is proposed in Fig. 2. It should be noted that some blocks of this architecture will be modified in the following subsections due to design considerations.

As shown in Fig. 3, first the binary values are converted into a current-mode output by the V-I converters. Then, just by wiring, the resultant current which represents the number of 1's, i.e. the Berger code, is created. Since the subtraction operation in current mode MVL has more challenges than the add operation. So, by a minor rearrangement in the basic Berger equation, the subtraction is converted into an add operation. To detect the faulty state, inequality in (1) is considered as a criterion. A current mode inequality comparator has been placed in the initial proposed scheme.

$$S_c + C_c + c_{out} = X_c + Y_c + c_{in} \quad (1)$$

1.1.1 Binary to Current Convertors

The binary bits of given X and Y operands, the resultant sum, and the carry bits are converted into current signals by a circuit which is depicted in Fig. 4. The reference current value, in Fig. 3, depends on the design requirements. Clearly smaller reference currents provide better conditions for power consumption, while the delay time and the correct operation may be degraded. Again, by increasing the W/L ratio of the transistors, a better characteristic in the current mirror is achievable, but in order to minimize the area penalty, we choose the $\{W/L\}_p = 2$ and $\{W/L\}_n = 1$.

1.1.2 Summation Blocks

By wiring only and without using any active device, the linear summation can be performed directly.

As depicted in Fig. 5, the resultant sum is applied to the inequality comparator. So, following the summation node, an NMOS current mirror block is placed as shown in the figure. Two copies of the resultant current are mirrored in this block as it is required in the comparator block. The summation block is the first unit in which an accurate current mirror is required. According to the simple current mirror structure, I_{out}/I_{ref} is equal to $((W/L)_2(1 + \lambda V_{DS2}))/((W/L)_1(1 + \lambda V_{DS1}))$. As the technology is scaled down, the channel-length modulation λ cannot be neglected. The error ratio in current mirrors affects the summation result, so a simple current mirror with the minimum scale, i.e. W/L = 1, may be an unsuitable choice for the

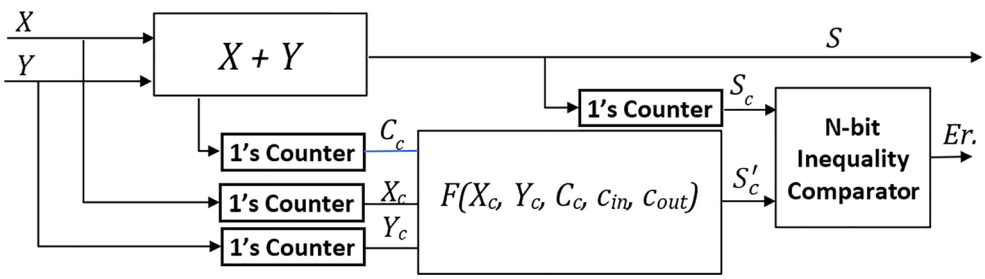

Fig. 1 Basic structure for a Berger checker

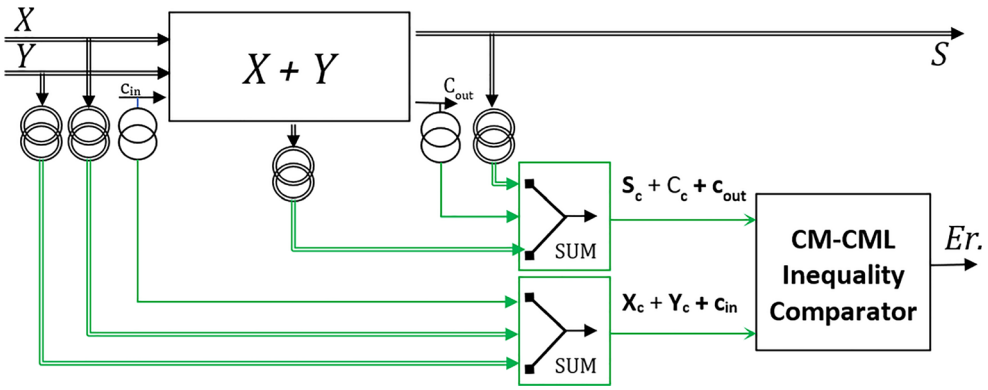

Fig. 2 Initial structure of the proposed scheme

summation unit. On the other hand, by increasing the transistor size, an unacceptable area overhead is imposed. It seems the only possible solution is that the drain-source (V_{DS}) voltages to be equal. Due to the varying state on the summation node, the binary values will be randomly changed; so, it will be very hard to achieve the voltage equality by a simple current mirror. This issue will be discussed later in the design challenges subsection.

1.1.3 Current Mode Inequality Comparator

The final stage in the proposed scheme compares the resultant currents which are delivered from the summation blocks. Figure 5 illustrates details of the proposed Current Mode Inequality Comparator (CMIC). First the difference currents, i.e. I_2-I_1 and $I_1 - I_2$, are computed. Then, as described in the preliminary section, the current mode subtract unit returns zero ampere if the first current is less than the second one. In cases that the first current is greater than the second one, the output will be equal to the difference value. In our proposed scheme, if I_1 and I_2 are equal, the subtract units return approximately zero. In an unequal state, one of them returns zero, while the other one returns the difference between the two currents. The minimum difference current value is related to a state in which at least a single bit error has been occurred. For an ideal design, single bit error will cause a difference current to be equal to I_{ref}. So, by using a threshold gate, in which the threshold value is adjusted to 0.5 I_{ref}, the faulty state will be detected by the following logic circuit. It should be pointed out that, the threshold operator is a main building block for current mode MVL logic. Suppose x and y are the input currents to this circuit, the output will be equal to (x-y) if x is greater than y, otherwise it is equal to 0 (Fig. 6).

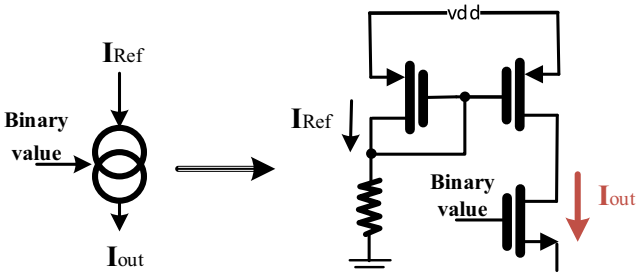

Fig. 3 Structure of the binary to current convertor

The simplified transistor level schematic of the proposed scheme for an n-bit adder is illustrated in Fig. 7 and Fig. 8. In a fault-free state, by assuming ideal current mirrors, the reflected current from MP1-MP2 are equal to the current value in the MN1 drain (refer Fig. 8 transistors). So, in this condition the inverters' inputs will be in an unknown state. To address this, a non-zero current source should be placed in node x, shown in Fig. 8. Its value should be smaller than the minimum faulty state current which is equal to I_{ref}. However, for a practical current mirror, as illustrated in the subsequent section, the intrinsic mismatch in current mirrors resolves this issue. So, this reference current is not required. In the digital part, an inverter chain is placed to provide a sharp transfer characteristic to detect a mismatch condition. Finally, an XOR gate is used over both faulty states, i.e. $I_1 > I_2$ and $I_1 < I_2$.

1.1.4 Design Challenges

The first challenge is related to $0.5I_{ref}$ current sources in Fig. 5. In the current mode logic, it is common that just one source is used and through the current mirroring the required current of all blocks is provided. Due to the high error ratio in area efficient current mirrors, four exact current sources are used in the proposed scheme: a current source for input operands, i.e. A, B, and C_{in}, one source for the result and carry bits; two others for current sources are dedicated for the inequality comparator block to supply the $0.5I_{ref}$. Initial simulations and investigations show that using four current sources with an inexact current mirror provide a better result than one source plus four accurate current mirrors. As mentioned through the intrinsic mismatch in the practical current mirrors, the $0.5I_{ref}$ sources have been removed, just two self-biased or bootstrap current references are used [11].

The second challenge, as the most challenging section in this scheme, relates to the differential current calculation units for I_2-I_1 and I_1-I_2 and their voltages, node x in Fig. 8, in the inverter chain input. This challenge has been described in the

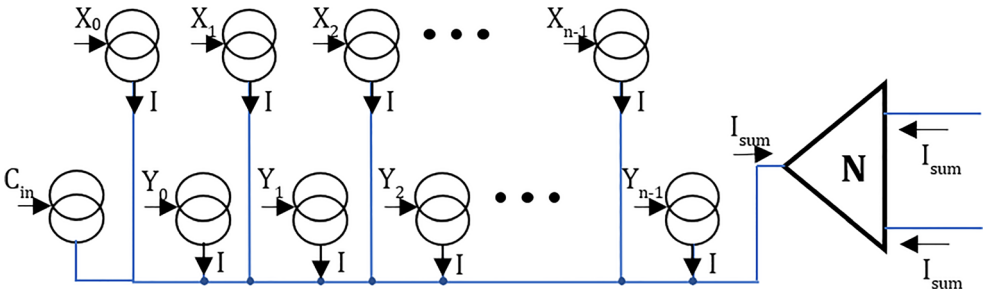

Fig. 4 Structure of the summation block in current mode MVL

following in details. To solve this issue, following the evaluating the upper and lower boundaries of voltage values in the node x for all possible cases, the inverter chain VTC, i.e. voltage transfer characteristic, is modified by changing the transistor dimensions. The differential current calculation units have the same structure, which will be investigated in more details as follows: The current subtraction unit receives two currents I_1 and I_2, and based on their difference a logical level is asserted in the output. If the referenced current is denoted as I_{ref}, and the number of '1's in the summation unit is supposed to be . In a non-faulty condition, we will have the equation as $I_1 = I_2 = I_{ref}$. It should be noted that for an n-bit adder the maximum value for is equal to $_{max} = 2n + 1$, in which n is the number of bits for operand A, n bits for operand B and 1 bit for the input carry. In a faulty condition, it is assumed that m bits in the summation block are faulty. This condition will cause inequality in currents, as for instance $I_1 = (\ + m)\ I_{ref}$ and $I_2 = I_{ref}$. For the cases in which I_2 is greater than I_1, the $(I_2 - I_1)$ subtraction unit will detect the faulty state. The current subtraction units must cover all possible faulty and non-faulty states. In a non-faulty condition, we suppose that the output logic level remains in a low state. This means that the voltage at the inverter input, which is called as node x, must be greater than the inverter switching voltage. Similarly, for faulty states, it is expected that the output logic will be in a high state, which means that the voltage in node x must be smaller than the switching voltage.

The upper and lower voltage boundary values in node x, for all faulty and non-faulty states and the inverter switching voltage are discussed in the following. The input voltage in the inverter, node x, faulty and non-faulty conditions have different requirements. For a specified reference current, I_{ref}, in non-faulty condition, i.e. m = 0, the I_1 is approximately equal to I_2. In this condition, I_2 when is mirrored by PMOS transistors, imposes an unwanted positive error σ. So, the current flowing into the node x is (I_{ref} + σ) and the current I_{ref} leaves the node. Due to the positive algebraic sum, the parasitic capacitor in node x is charged and a positive voltage in node x is generated. When the voltage in node x is increased, the mirrored current in PMOS current mirrors is decreased. Finally, in the steady state condition, the voltage in node x is fixed at a certain value. This voltage corresponds to the minimum input voltage V_{IHmin}. For a faulty state, through the PMOS current mirror, (I_{ref} + σ) flows into the node x, while (+ m)Iref flows out of the node. In this condition, (σ - mI_{ref}) feeds the parasitic capacitor and the voltage in node x is determined. In a faulty state, it is expected that the design parameters are selected so that the voltage in node x is placed under the inverter switching voltage. By increasing the number of faults, i.e. m value, or increasing the reference current I_{ref}, the voltage condition in node x is improved. Also, an accurate current mirror, which imposes less σ, provides a better condition in a faulty state. In a faulty state, the voltage levels are related to the maximum input voltage V_{ILmax} for the inverter chain. Simulation results show that in the minimum faulty state, i.e. m = 1, we have the worst case for tuning the switching voltage in the inverter chain. In Fig. 6, the maximum and minimum threshold voltages for different is depicted while m is supposed 1. Based on these results the inverter switching voltage is set.

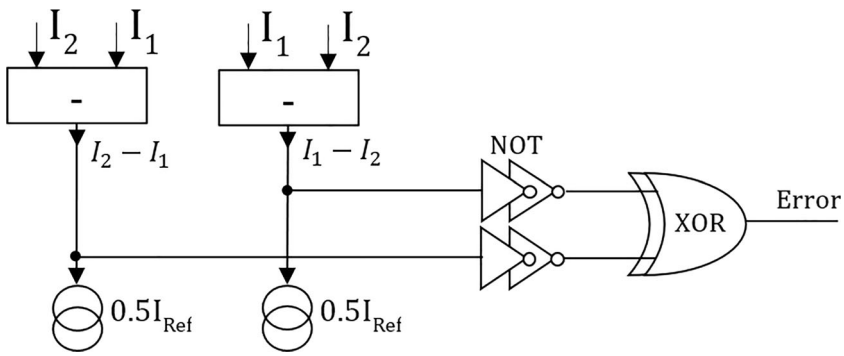

Fig. 5 An inequality comparator in the current mode MVL

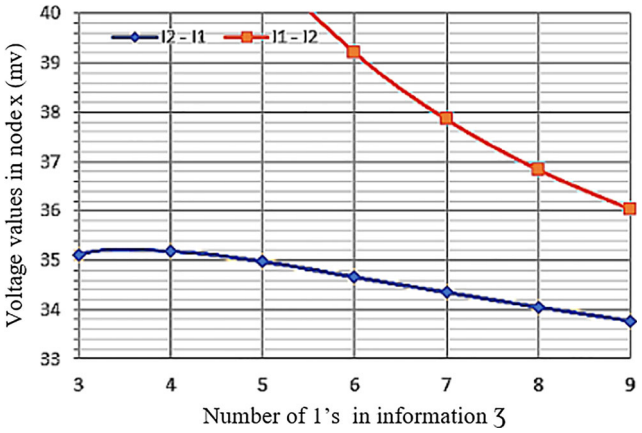

Fig. 6 Node x voltage values vs. number on 1's, , with m = 1

1.1.5 A Low Power Sub-Threshold Solution

In order to decrease the power consumption, the first idea is that the reference current is minimized as much as possible. It is almost impossible to find the minimum acceptable reference current analytically. This is because the proposed scheme is also able to work even when the FET is in the triode or ohmic region. Therefore, the simulation approach is the only solution to find the minimum reference current in which all faulty and non-faulty states can provide a correct error signal. As a second approach to decrease the required power, the sub-threshold regime can be used for the proposed current mode Berger code checker. The proposed scheme is immune against the current mirror inaccuracy. So, it is expected that in the sub-threshold region, the proposed scheme is able to work properly. In sub-threshold, the supply voltage is decreased to 0.2 V. By decreasing the supply voltage, the reference current can be decreased much more than its nominal value.

As shown in Fig. 9, the supply voltage for the blue highlighted section, i.e. the proposed Berger code checker circuit, is equal to 0.2 V. The main adder circuit and a level shifter are supplied with the nominal 1 V. The maximum output voltage level of the checker circuit is equal to 0.2 V. To translate the error signal from the sub-threshold voltage to a binary logic level, a level shifter is required. Various circuits have been introduced in the literature, one of the newest ones is proposed in [7] which is being used in our proposed scheme.

2 Results and Discussion

To verify the efficiency of the proposed Berger code checker for adders, the proposed structure and also the conventional structures, i.e. duplex and parity check, have been simulated at the transistor level in a 90 nm CMOS technology. All circuits have been designed in the minimum feature size for VDDH = 1 V, VDDL = 0.2 V and the input frequency of adders are assumed to be 10-MHz. In order to have a fair comparison among the structures, just operands X and Y are assumed as the system inputs. All other required signals, like the parity of the input operands which is needed in the parity checker, are computed in the checker. A sample layout of the proposed level shifter is illustrated in Fig. 10. The active area occupied by the circuit is reported in Table 1. The following simulation results are related to the post-layout analysis. The simulation results have been compared in Table 2. In Table 1, the plain structure is the adder circuit without any fault detection mechanism. Its design parameters include power, delay, area and power-delay product (PDP) which have been reported for different data sizes: 8-bit, 16-bit, 32-bit and 64-bit. The aforementioned parameters are also reported for the traditional duplex structure, the dual rail carry with parity checker and for the proposed current mode Berger checkers in Table 1. In the reported data for traditional and the proposed structures, just the checker circuit parameters have been presented. To provide a better illustration, in Table 2, the area, delay and power overhead percentages

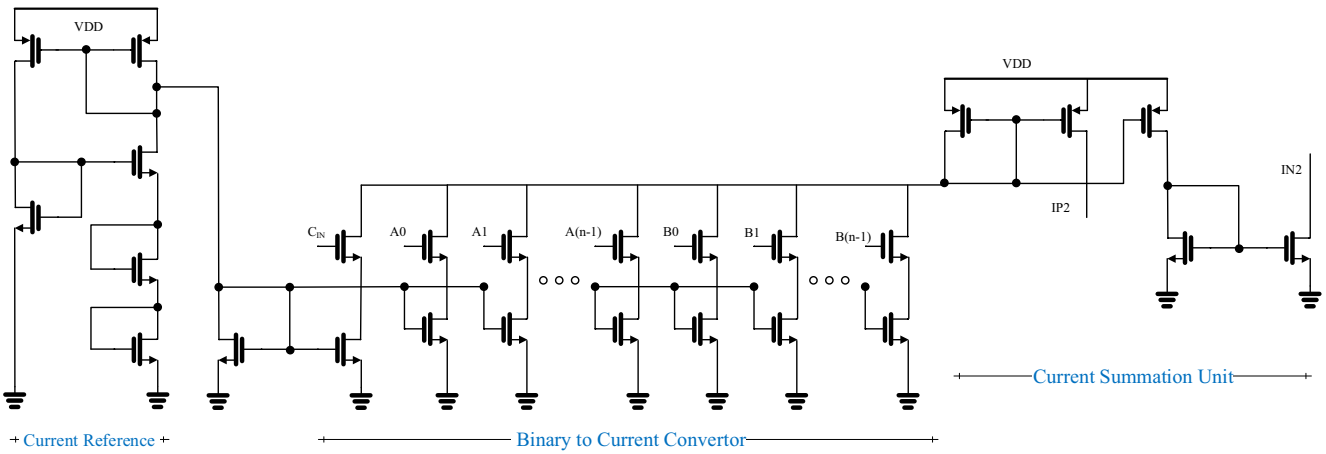

Fig. 7 Transistor level schematic of the proposed scheme MVL convertor and summation unit

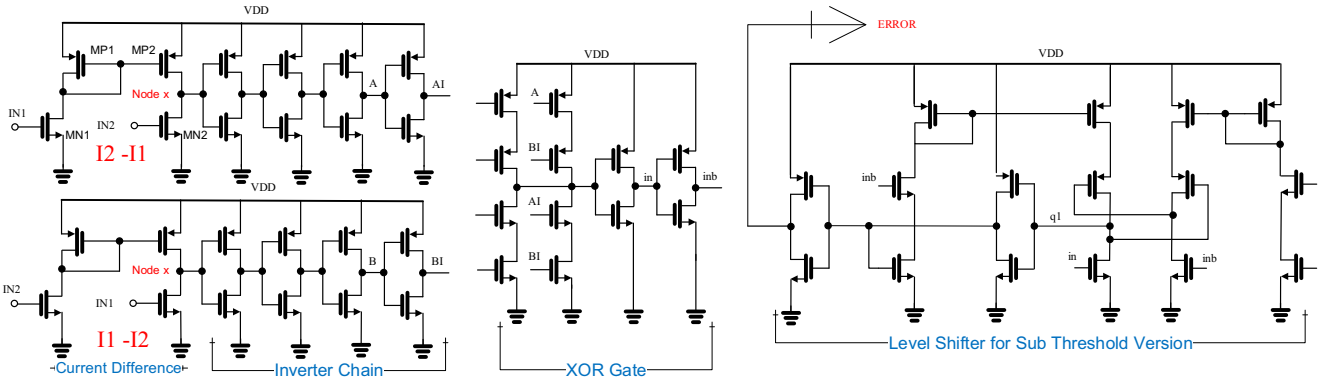

Fig. 8 Current subtraction scheme (I1 – I2) in transistor level

have been summarized for different data sizes. The average overhead is also calculated for all approaches.

The results reveal that the proposed structures impose much less area overhead than the conventional Berger checkers. On average the proposed structures have the minimum area penalty among the investigated architectures. However, in the proposed structures one of the parameters, the power or delay, is unacceptable in comparison with other structures. The present study confirms previous studies wherein stated that the current-mode MVL requires more power compared to the binary logic.

The power consumption problem can be solved by the proposed subthreshold structure, but, as expected for subthreshold circuits, the proposed architecture imposes much more delay time. The proposed ultra-low power checker circuit can be used in some special applications such as nodes in the internet of things (IOT), in which power issue is more critical than real-time fault detection capability. The main motivation to design the Berger checker in the current mode MVL logic is related to the fact that the sum of 1's or 0's, which is required in Berger checker, can be realized with a minimum number of transistors. The reported results verify that the area overhead in the proposed structures is reasonable.

Another promising finding is that although the theory of Berger code for adder circuits has been thoroughly investigated, but its realization is more challenging. Besides the conventional Berger checker in the binary logic, two novel Berger checker architectures have been studied in this paper. In all cases, the Berger checker for adder circuits imposes unacceptable penalties at least in one of the following parameters: delay, power and area. The conventional Berger checker using the binary logic is totally refused. In comparison with the duplex circuit, as a straightforward method, all its design parameters are unacceptable. The proposed architectures in the current mode MVL have a desirable area, while a tradeoff between power and delay is required.

The proposed architectures effectiveness depends on the application. If the power consumption or delay time is negligible in a special application, the proposed architectures will be beneficial in adder circuits. It should be pointed out that the adder circuits are the smallest digital circuits. When we evaluate the effectiveness of the proposed Berger checker architectures based on the duplicated adder circuits, the results may not be very illuminative. Certainly, in complicated circuits, the proposed architectures will provide more interesting results.

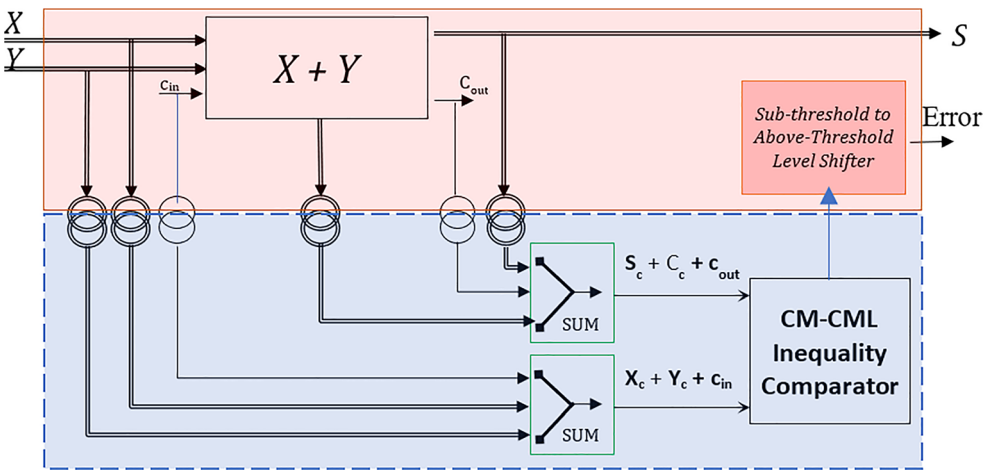

Fig. 9 Proposed Berger checker in the sub-threshold regime

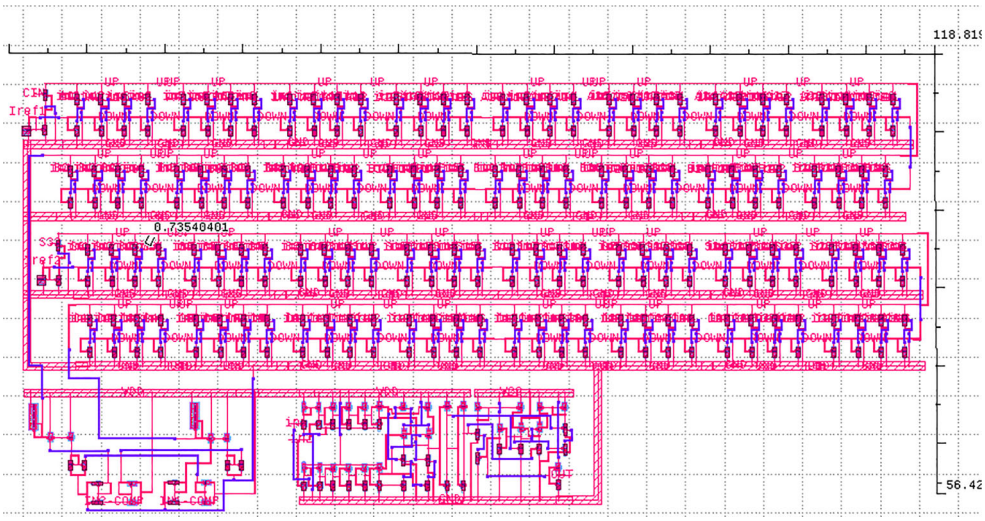

Fig. 10 Layout of the proposed Berger code checker for 32bit adder

3 Conclusion

A Berger code checker for adder circuits has been fully investigated in this paper. Since adders are among the smallest combinational digital circuits, the area penalty is a major concern to design the fault checker circuit. The conventional binary Berger checkers are not able to fulfil area requirements. So, innovative approaches are needed, especially when the main circuit is small. Current mode MVL can be an appropriate candidate to address this problem. However, by technology down scaling, the current mirror as the main element in current mode logic, imposes an unacceptable error ratio. By increasing the transistor feature size and using some novel approaches to design the current mirrors, the error ratio can

Table 1 Post layout simulation results

Structure	adder	Area (μm^2)	Delay (ns)	Power (uw)	PDP (aJ)
Plain	8	4021	1.12	3.69	4.13
	16	8251	2.23	7.38	16.45
	32	17,200	4.68	17.11	80.02
	64	34,765	9.56	41.20	393.8
Duplex Checker	8	5057	0.17	4.48	0.76
	16	10,471	0.22	9.09	2.07
	32	21,788	0.28	20.63	5.88
	64	44,237	0.34	48.49	16.58
Dual rail carries with Parity Checker	8	2591	0.28	2.20	0.62
	16	2888	0.34	4.40	1.50
	32	6023	0.39	9.63	3.84
	64	12,168	0.45	21.71	9.90
Conventional Berger Checker	8	20,546.4	1.79	18.78	17.92
	16	37,782.8	2.63	34.58	47.51
	32	71,103.2	3.53	65.13	120.5
	64	136,591	4.65	125.2	301.8
Proposed Current Mode Berger Checker	8	1843	0.31	19.52	6.09
	16	2973	0.38	29.29	11.247
	32	4989	0.44	31.18	13.74
	64	9471	0.64	33.45	21.54
Proposed Sub-threshold Current Mode Berger Checker	8	1723	51.6	0.126	6.501
	16	3725	52.1	0.156	8.127
	32	6380	49.1	0.162	7.954
	64	10,796	65.8	0.375	24.675

Table 2 Area overhead, power and delay penalties

Structure	adder	Area %	Delay %	Power %
Duplex Checker	8	125.76	15.26	121.62
	16	126.90	10.22	123.17
	32	126.67	6.08	120.66
	64	127.24	3.57	117.70
	avg.	126.64	8.78	120.78
Dual rail carries with Parity Checker	8	64.44	25.44	59.71
	16	35.01	15.33	59.71
	32	35.02	8.52	56.33
	64	35.01	4.76	52.70
	avg.	42.37	13.51	57.11
Conventional Berger Checker	8	510.97	160.17	508.94
	16	457.91	118.11	468.56
	32	413.39	75.44	380.65
	64	392.89	48.65	303.90
	avg.	443.79	100.59	415.51
Proposed Current Mode Berger Checker	8	45.82	27.85	528.99
	16	36.03	17.21	396.88
	32	29.01	9.41	182.37
	64	27.24	6.73	81.20
	avg.	34.52	15.3	297.36
Proposed Sub-threshold Current Mode Berger Checker	8	42.84	4607.14	3.41
	16	45.14	2336.32	2.11
	32	37.09	1049.14	0.94
	64	31.05	688.28	0.91
	avg.	39.03	2170.22	1.84

be improved. At the meantime, these methods also impose more area overhead when compared with the adders. This paper presents a novel area-efficient current mode Berger code checker for adders. The proposed scheme is a symmetric structure in which each current mirror has its own corresponding mirror. So, the current mirror error is compensated for its corresponding mirror. This attribute allows the designer to use simple current mirrors with the minimum feature size. Moreover, the proposed scheme is able to operate in the sub-threshold regime with very minor modifications. Post layout simulation results using a 90 nm CMOS technology confirm the efficiency of the proposed Berger code checker for adders.

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