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The Fundamental Primitives with Fault-Tolerance in Quantum-Dot Cellular Automata

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Abstract
Since conventional CMOS technology has met its development bottleneck, an alternative technology, quantum-dot cellular automata (QCA), attracted researchers' attention and was studied extensively. The manufacturing process of QCA, however, is immature for commercial production because of the high defect rate. Seeking for designs that display excellent performance shows significant potentials for practical realizations. In the paper we propose a 5 × 5 module, which not only can implement three-input majority gate but also can realize five-input majority gate by adding another two inputs. A comprehensive analysis is made in terms of area, number of cells, energy dissipation and fault tolerance against single-cell omission defects. In order to testify the superiority of the proposed designs, preexisting related designs are tested and compared. Weighing up above four kinds of factors and technical feasibility, proposed majority gates perform fairly well. Further, we take full adders and multi-bit adders as illustrations to display the practical application of proposed majority gates. The detailed comparisons with previous adders reveal that proposed 5 × 5 module behaves well in circuits, especially the high degree of fault tolerance and the relatively small area, complexity and QCA cost, thereby making it more suitable for practical realizations in large circuit designs.

Keywords Quantum-dot cellular automata · Three and five-input majority gates · Adder · Fault tolerance

1 Introduction

Conventional CMOS technology has encountered some challenges, such as physical scalability limits, leakage power consumption, and short channel effects [18]. Under the circumstance, a large amount of research on nano-scale has been done extensively. Quantum-dot cellular automata (QCA), a promising alternative technology with potential advantages of fast speed, high density and ultra-low power consumption [27, 32], offers a new method of computation and information transmission. QCA was first proposed by Lent et al. in 1993 [27], and was developed rapidly in recent years. Some experimental devices have been fabricated and tested [4, 25, 46]. To date, the implementation for multi-layer circuits has not been reported [5, 14], while coplanar circuit have already been fabricated [32].

The most distinct feature of QCA is that interaction between cells is absolute Columbic repulsion. Thus there is no current in circuits, which has a potential for extremely low energy dissipation, even makes it lower than traditional k_BT in the most optimistic condition [39, 40]. Nevertheless, as an emerging technology, it is necessary to characterize all aspects of QCA. Due to the small size and the fact that electrons actually involve in computation, power consumption is an important parameter. Analogous to conventional CMOS designs, power loss in clocked QCA circuit can be categorized into two types that are commonly used in circuit theory: switching power and leakage power [39]. Switching power which depends on input combinations happens at the time when the cell is changing its state. Leakage power which has nothing to do with input states occurs when the clock goes up or falls down so as to 'depolarize' or 'polarize' a cell. The proportion of the two in total power dissipation relates

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strongly to the clock energy. To solve the power consumption in QCA circuits, various estimation models have been proposed, of which two representatives are the accurate power dissipation model and the upper bound power dissipation model, proposed by John Timler et al. and Saket Srivastava et al., respectively [39, 41]. Power dissipation of QCA devices and circuits can be estimated using these models so that we can pick out the superior. QCAPro based on the upper bound power model can be used to assess the performance of QCA designs under power analysis attack, including average, maximum, and minimum power dissipation [40].

Yet QCA technology has not been put into production heavily. One principal limitation is the high fault rate in manufacturing, particularly for molecular QCA, since it is difficult to be high precision within nanoscale. The fault rate has been predicted as high as 50% of the devices [17, 48]. Any defect could result in possible invalidation of device functions. Thus a device with fault tolerance appears to be particularly significant in practice. Robustness and fault tolerance properties have been investigated during the past few years [23, 34]. There are various types of defects that may occur in QCA devices during the fabrication, such as cell misalignment, cell displacement, cell omission, cell rotation and so on. Functionalities of a device may still exist when these defects happen, namely reliability. This is just the direction we are pursuing for. In this paper, we analyze the reliability of QCA designs in presence of single-cell omissions. The designs with the property of insensitiveness to cell omissions will show good prospects in further development.

The main aim of our work is to seek out a three and five-input majority gates with fault tolerance. In order to characterize the proposed majority gates, comparisons are made with their counterparts in terms of area, number of cells, energy dissipation and fault tolerance. By applying the proposed designs to practical circuits and comparing with relevant circuits, the functionality and practicability of them are verified.

The reminder of the paper is organized as follows: Section 2 presents QCA theoretical background and some basic devices. Elaborately selected and our proposed designs as well as their applications will be shown and discussed in Section 3. The simulation results of all circuits are displayed in Section 4. Finally, conclusions are given in Section 5.

2 QCA

The elementary units in QCA are cells. A quantum cell can be viewed as a square with four dots positioned at the corners of it [42]. The cell contains two extra mobile electrons which can quantum mechanically tunnel between dots within the cell but not cells. Due to Columbic repulsion, electrons always occupy the diagonal positions of square in the absence of any external influence. Thus, two possible polarization states, i.e. "$P=-1$" and "$P=+1$", can be used to represent logic "0" and logic "1" respectively, as shown in Fig. 1a [30]. There is another type of QCA cells, i.e. rotated cells, which are able to achieve the same result, as illustrated in Fig. 1b. The difference between these two types of cells is the way of information transmission according to Columbic repulsion of electrons. Two neighboring standard cells will achieve same polarization, while rotated cells will get reverse polarization. The rotated cells can be used to realize coplanar wire-crossing with standard cells.

Two fundamental building blocks utilized as critical elements in QCA circuits are inverters and majority gates [35]. Since every QCA circuit can be implemented only using majority gates and inverters, efficient constructions of them are of great importance [31]. Figure 2 shows two frequently-used inverters.

As depicted in Fig. 3a, a three-input majority gate is composed of five cells, with three input cells labeled as A, B, C, an output cell marked with F and the center one called device cell. The logic expression of it is $F = M(A, B, C) = AB + BC + AC$. The output of majority gate depends on the values of given inputs that occupy the major, just like a voter. Two-input "AND" gate or "OR" gate can be implemented by fixing a input into logic 0 or logic 1, respectively, as shown in Fig. 3b and c. The governing equations for "AND" and "OR" gates using 3-input majority gate are

$$F = M(A, B, 0) = AB \tag{1}$$

$$F = M(A, B, 1) = A + B \tag{2}$$

With "AND", "OR" and inverters, any logic function can be realized.

On account of the important role of 3-input majority gate in QCA, different designs have been investigated over last years. Even though the three-input majority gate in Fig. 3a is the simplest and the most elementary one, missing of any one cell could lead to defects. In Fig. 4 six formerly proposed types of 3-input majority gates with fault tolerance are shown. Seeking for high degree of fault tolerance, low power dissipation, small area and number of cells is beneficial to future realization. These layouts are designed to balance above factors.

The logic function of five-input majority gate can be presented as:

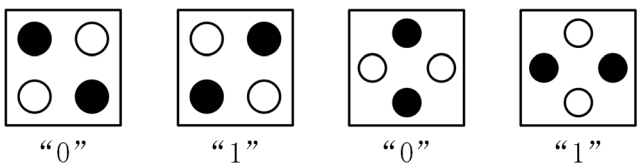

Fig. 1 **a** Standard cells representing logic "0" and "1". **b** Rotated cells representing logic "0" and "1"

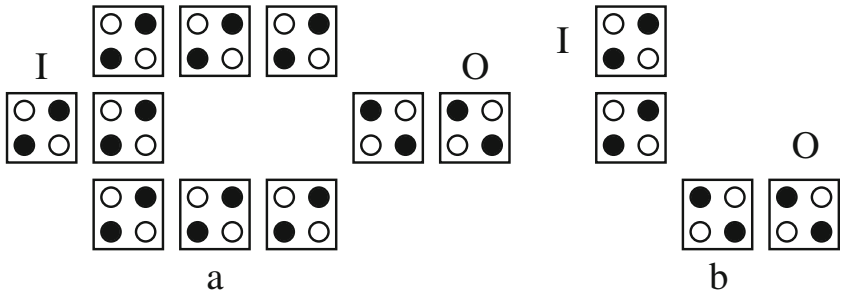

Fig. 2 Two typical inverters **a** Normal inverter. **b** Simplest inverter

$$F = M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (3)$$

where A, B, C, D and E are inputs and F is output.

Similar to 3-input majority gate, "AND" or "OR" gate can also be realized using 5-input majority gate. By forcing two of the five inputs' polarizations to −1 or + 1, a 3-input "AND" or "OR" gate is formed. As yet, several implementations of 5-input majority gate have been reported, as shown in Fig. 5.

To minimize the power dissipation and hold the stable state of a QCA system consistently, the adiabatic switching mechanism, which is achieved by an external electric field, was introduced to solve the disadvantages of abrupt switching. This method is absolutely different from the clocking mechanism represented by the levels of voltage in CMOS-based circuits [19, 26, 41]. During the adiabatic switching, QCA system can always not only remain in instantaneous ground state, but also gain the least amount of power consumption. As shown in Fig. 6, the QCA clocking mechanism has four clocking zones, each of which is shifted from the previous one by 90° and has four phases: switch, hold, release and relax [43]. At the beginning, the cells in a system stand at the relax state because the inter-dot tunnel barriers are controlled at the lowest level. With the gradually increased barriers over switch phase and peaking in hold state, the polarizations of the cells will encode the binary information. During the release phase the tunnel barriers decrease and then reach the lowest value at relax state, which results in the complete loses of polarization information in each cell and preparation for the next cycle [22].

The equation for the instantaneous total power for a single QCA cell is written as

$$P_{total} = \frac{dE}{dt} = \frac{\hbar}{2}\frac{d\vec{\Gamma}}{dt}\cdot\vec{\lambda} + \frac{\hbar}{2}\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt} = P_1 + P_2 \quad (4)$$

where $\vec{\Gamma}$ represents the real 3-D energy vector, $\vec{\lambda}$ is the coherence vector. The first term P_1 in above equation represents the difference (P_{in} - P_{out}) between power input (P_{in}) and power output (P_{out}) and the power (P_{clock}) transferred from clocking signal. The second term P_2 gives the dissipated power (P_{diss}) that is exactly our concerned. In a quasi-infinite QCA array, P_{in} achieved from left neighboring cell is equal to P_{out} released power to the right neighboring cell. Moreover, in switch phase, with the increasing of inter-dot barrier, an amount of energy transfers from clocking to cell. Afterwards, most of the energy returns to clocking over lowering phase of barrier, which leads to a trivial power dissipation just named P_{diss}.

3 Proposed Fault-Tolerant Designs and Applications

3.1 Proposed Designs

Fault-tolerant design in QCA is an essential subject for representation of suitable functionality of the circuits. Faults always occur without expectation during the

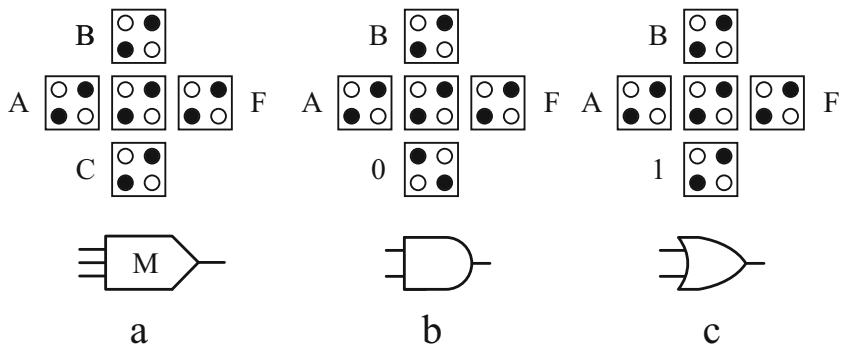

Fig. 3 Logic gates and schematics **a** Three-input majority logic gate. **b** AND gate. **c** OR gate

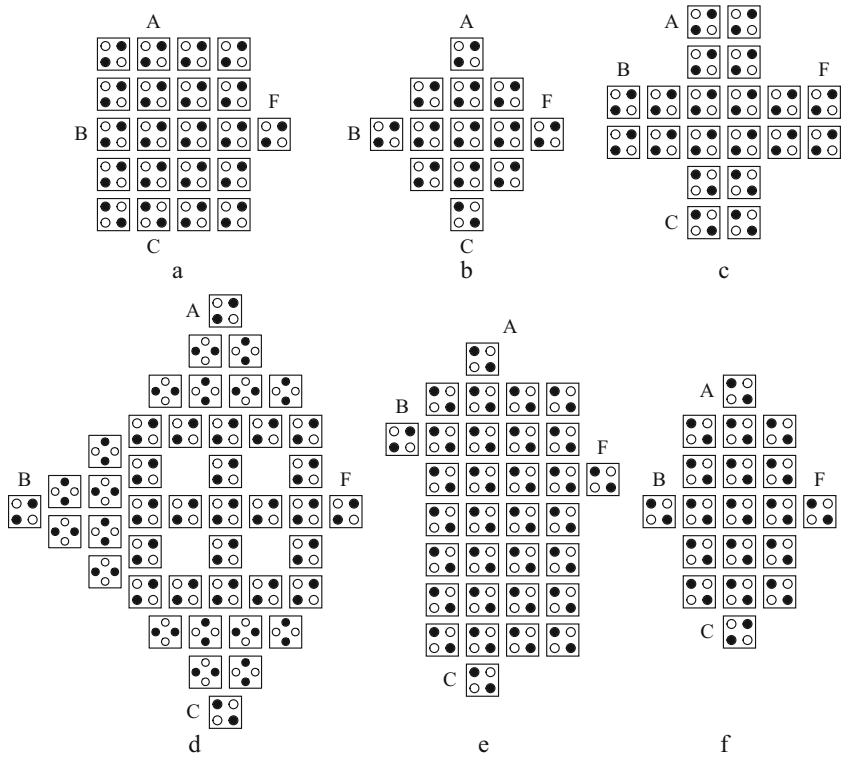

Fig. 4 Previous fault-tolerant three-input majority gates **a** In [9]. **b** In [7]. **c** In [24]. **d** In [38]. **e** In [3]. **f** In [8]

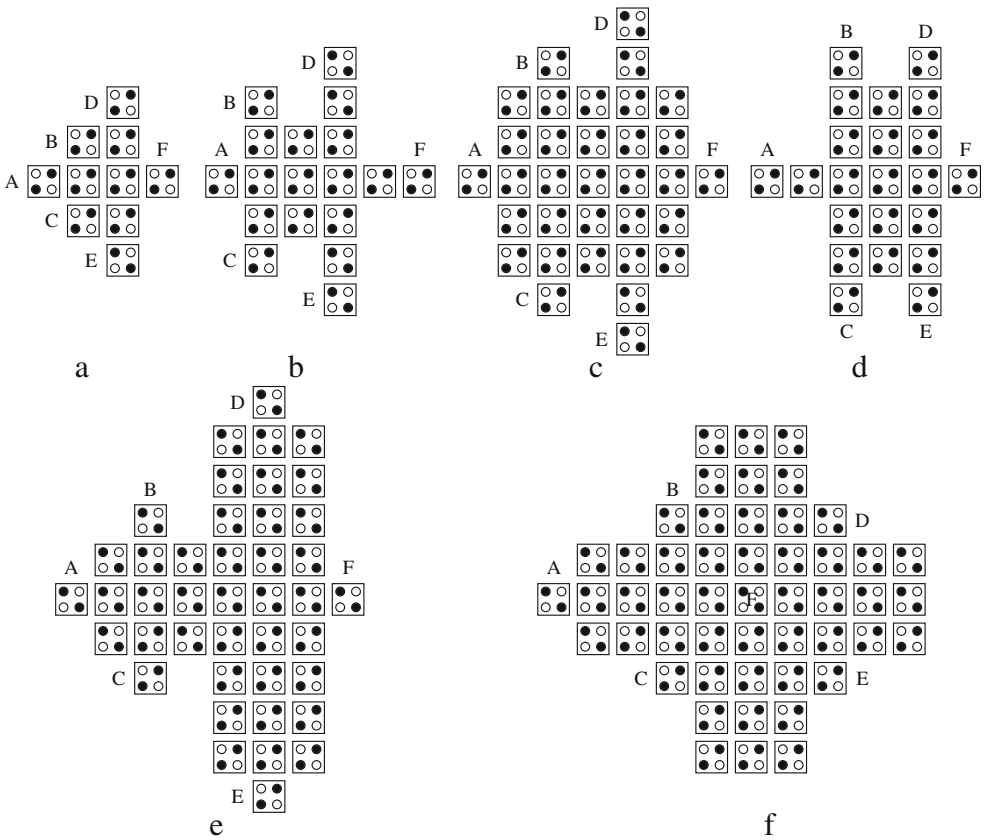

Fig. 5 Previous fault-tolerant five-input majority gates **a** In [31]. **b** In [1]. **c** In [1]. **d** In [8]. **e** In [13]. **f** In [10]

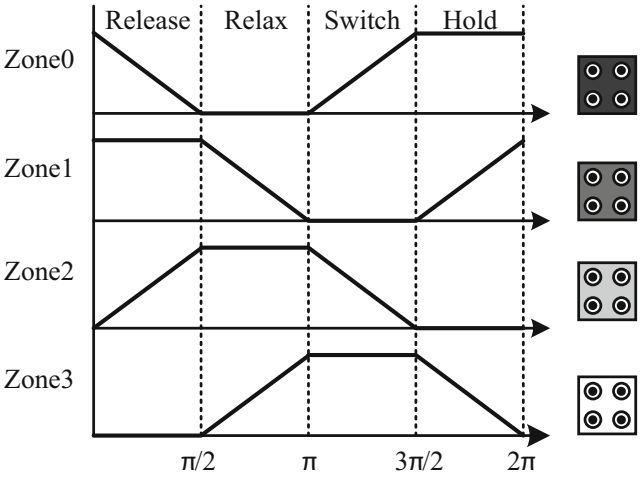

Fig. 6 QCA four clocking phases within clock zones

assembly of a circuit, such as "misalignment" cells (quantum cells are shifted from their intended locations), "missing" cells (a quantum cell or several quantum cells is or are missing), "dislocation" cells (quantum cells are rotated relative to other cells in the array), all of which may result in the termination of function of circuits. In the paper, we focus on the defects of cell omissions. We propose two kinds of novel designs with respect to majority gates including 3-input and 5-input. Three-input majority gate in Fig. 7a and five-input majority gate in Fig. 7b are both based on a 5 × 5 module. Three-input majority gate is added two more inputs to implement five-input majority gate, which is convenient to achieve the transformation between these two gates.

In order to authenticate the correctness and the functionality of our proposed designs as well as previously related designs, QCADesigner version 2.0.3 [44] with the bistable approximation engine setup summarized in Table 1 is used.

Table 1 Parameters of bistable approximation

Parameter	Value
Cell size	18.0 nm × 18.0 nm
Dot diameter	5.0000 nm
Cell-to-cell spacing	2.0 nm
Number of samples	102,400
Convergence tolerance	0.00001
Radius of effect	41.00000 nm
Relative permittivity	12.900000
Clock high	9.800000e-022
Clock low	3.800000e-023
Clock shift	0.000000e + 000
Clock amplitude factor	2.000000
Layer separation	11.500000
Maximum iterations per sample	10,000

3.2 Physical Proof for Five-Input Majority Gate with One Cell Omission

Since proposed five-input majority gate has 27 cells and any cell missing could lead to invalidation of the design, we should check all the faults that may occur in cells to verify the correctness of the scheme. Here, as shown in Fig. 8, we just prove one of the faults that occurs in the third row, forth column of the 5 × 5 module. Similarly, other faults can be proved as well. Five inputs of the majority gate are assumed to $A = C = E = 1$ and $B = D = 0$. Figure 8a and b denote two possible states of the output F, respectively. By calculating the total electrostatic energy of these two configurations, we can find the more stable one with lower kink energy level. The electrostatic energy between two electrons is calculated using Eq. (5).

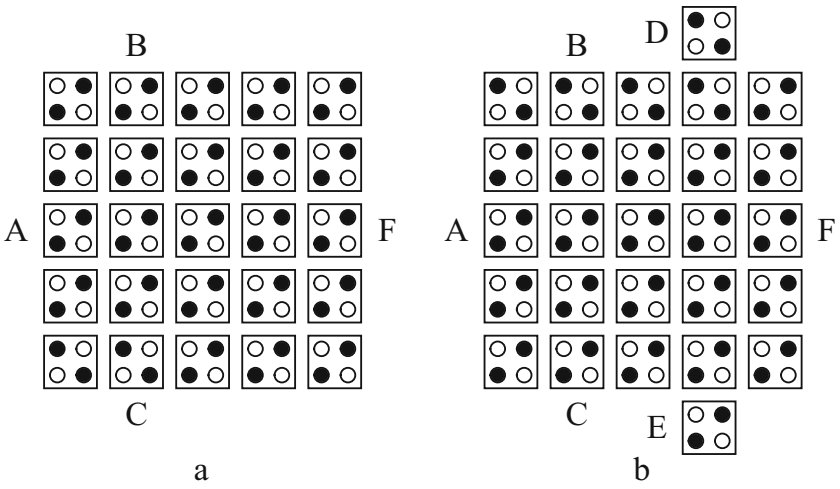

Fig. 7 Proposed fault-tolerant gates **a** Three-input majority gate. **b** Five-input majority gate

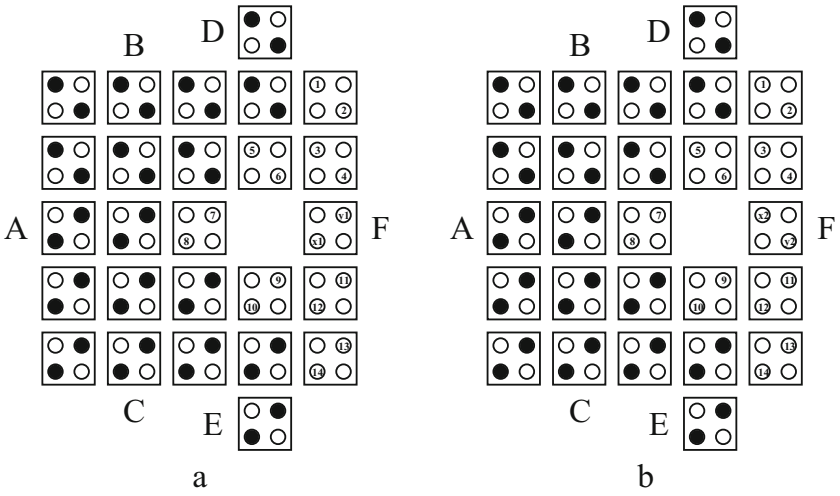

Fig. 8 Two configurations with one cell omission of **a** The one value for x1 and y1. **b** The zero value for x2 and y2

$$U = \frac{kq_1q_2}{r} \tag{5}$$

where U is electrostatic energy between two electrons, k is a constant, q_1 and q_2 are electron charges, and r is distance between these two electrons.

By computing the electrostatic energy between 14 electrons and x, y respectively, the total electrostatic energy can be achieved. Further detailed calculation is shown in Table 2. The eventual results ($U_{T_1} < U_{T_2}$) prove that the state in Fig. 8a is the more stable one. The functionality also can be verified using QCADesigner.

3.3 Application

As mentioned earlier, many QCA designs including adders, multipliers, multiplexers etc. can be implemented based on majority gates. Two novel one-bit full adders are displayed using three and five-input majority gates proposed, as shown in Fig. 9. Figure 9a displays a full-adder with three three-input majority gates. The other one shown in Fig. 9b is implemented using a three-input majority gate and a five-input majority gate. As illustrated in Fig. 10, the 4-bit carry flow adder, which has a 1.5 clock cycles, is

Table 2 Physical verification for radius of effect of 41 nm

Electron x	Electron y
$U_1 = \frac{A}{r_1} = \frac{A}{r_1} \approx 0.40 \times 10^{-20}\ (J)$	$U_1 = \frac{A}{r_1} = \frac{A}{r_1} \approx 0.53 \times 10^{-20}\ (J)$
$U_2 = \frac{A}{r_2} = \frac{A}{r_2} \approx 0.53 \times 10^{-20}\ (J)$	$U_2 = \frac{A}{r_2} = \frac{A}{r_2} \approx 1.05 \times 10^{-20}\ (J)$
$U_3 = \frac{A}{r_3} = \frac{A}{r_3} \approx 0.61 \times 10^{-20}\ (J)$	$U_3 = \frac{A}{r_3} = \frac{A}{r_3} \approx 0.86 \times 10^{-20}\ (J)$
$U_4 = \frac{A}{r_4} = \frac{A}{r_4} \approx 0.86 \times 10^{-20}\ (J)$	$U_4 = \frac{A}{r_4} = \frac{A}{r_4} \approx 11.52 \times 10^{-20}\ (J)$
$U_5 = \frac{A}{r_5} = \frac{A}{r_5} \approx 0.54 \times 10^{-20}\ (J)$	$U_5 = \frac{A}{r_5} = \frac{A}{r_5} \approx 0.54 \times 10^{-20}\ (J)$
$U_6 = \frac{A}{r_6} = \frac{A}{r_6} \approx 1.15 \times 10^{-20}\ (J)$	$U_6 = \frac{A}{r_6} = \frac{A}{r_6} \approx 1.15 \times 10^{-20}\ (J)$
$U_7 = \frac{A}{r_7} = \frac{A}{r_7} \approx 0.81 \times 10^{-20}\ (J)$	$U_7 = \frac{A}{r_7} = \frac{A}{r_7} \approx 0.58 \times 10^{-20}\ (J)$
$U_8 = \frac{A}{r_8} = \frac{A}{r_8} \approx 0.58 \times 10^{-20}\ (J)$	$U_8 = \frac{A}{r_8} = \frac{A}{r_8} \approx 0.38 \times 10^{-20}\ (J)$
$U_9 = \frac{A}{r_9} = \frac{A}{r_9} \approx 8.15 \times 10^{-20}\ (J)$	$U_9 = \frac{A}{r_9} = \frac{A}{r_9} \approx 0.81 \times 10^{-20}\ (J)$
$U_{10} = \frac{A}{r_{10}} = \frac{A}{r_{10}} \approx 0.81 \times 10^{-20}\ (J)$	$U_{10} = \frac{A}{r_{10}} = \frac{A}{r_{10}} \approx 0.43 \times 10^{-20}\ (J)$
$U_{11} = \frac{A}{r_{11}} = \frac{A}{r_{11}} \approx 1.27 \times 10^{-20}\ (J)$	$U_{11} = \frac{A}{r_{11}} = \frac{A}{r_{11}} \approx 1.15 \times 10^{-20}\ (J)$
$U_{12} = \frac{A}{r_{12}} = \frac{A}{r_{12}} \approx 1.15 \times 10^{-20}\ (J)$	$U_{12} = \frac{A}{r_{12}} = \frac{A}{r_{12}} \approx 0.55 \times 10^{-20}\ (J)$
$U_{13} = \frac{A}{r_{13}} = \frac{A}{r_{13}} \approx 0.81 \times 10^{-20}\ (J)$	$U_{13} = \frac{A}{r_{13}} = \frac{A}{r_{13}} \approx 0.58 \times 10^{-20}\ (J)$
$U_{14} = \frac{A}{r_{14}} = \frac{A}{r_{14}} \approx 0.58 \times 10^{-20}\ (J)$	$U_{14} = \frac{A}{r_{14}} = \frac{A}{r_{14}} \approx 0.38 \times 10^{-20}\ (J)$
$U_{T_{11}} = \sum_{i=1}^{14} U_i = 18.23 \times 10^{-20}\ (J)$	$U_{T_{12}} = \sum_{i=1}^{14} U_i = 20.49 \times 10^{-20}\ (J)$
$U_{T_1} = \sum_{i=1}^{2} U_{1i} = 38.71 \times 10^{-20}\ (J)$	
$U_{T_{21}} = \sum_{i=1}^{14} U_i = 18.41 \times 10^{-20}\ (J)$	$U_{T_{22}} = \sum_{i=1}^{14} U_i = 20.45 \times 10^{-20}\ (J)$
$U_{T_2} = \sum_{i=1}^{2} U_{2i} = 38.86 \times 10^{-20}\ (J)$	

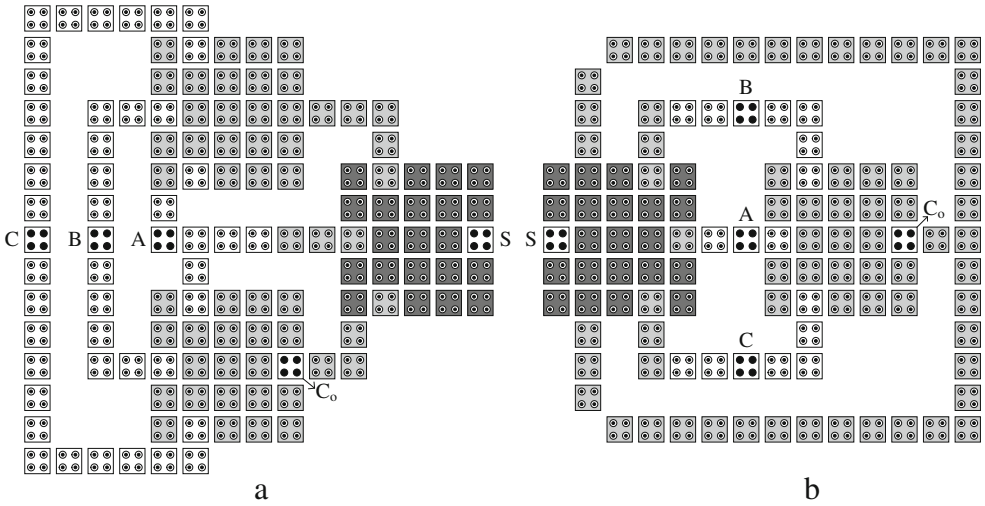

Fig. 9 Proposed full adders with **a** Three three-input majority gates. **b** A three-input majority gate and a five-input majority gate

implemented with coplanar crossovers in each unit. The *n*-bit carry flow adder can be constructed by cascading *n* proposed adders logically.

4 Simulation Results

4.1 Three-Input Majority Gate

Table 3 displays the physical properties of three-input majority gates from different references. P denotes the proposed 3-input majority gate. Figure 11 depicts the bar-graphs of these comparisons.

The gate in [26] has the smallest area, number of cells and energy dissipation in contrast with other gates. However, the design will lose its function when any one cell misses, namely the fault tolerance is 0, just as shown in Fig. 11c. P reaches 45.70% improvement in fault tolerance compared with [7] which can be viewed as a 3×3 tile. [38] is a grand design with largest area, maximum cell counts and highest average energy dissipation. The fault tolerance of it, 97.44%, is also the highest one. All the cases are correct except one on the left of the output cell *F* in the presence of single-cell omission. But limited by the manufacturing process of QCA technology, rotated cells used in the design are yet to come true, thereby making it unsuitable for practical realization. [3, 8] can be considered as a 4×7 module and a 3×5 module respectively. Fault tolerance of gate P leads to 25.91% and 34.92% improvements compared with that of them, respectively. The gate in [3], in terms of area, number of cells, energy dissipation and fault tolerance, always shows poorer performance in contrast with P. Fault tolerances of [9, 24] are almost equal to that of P. However, the superiority of gate P is that it can be extended into five-input majority gate by adding another two input cells as shown in Fig. 7b. Note that the structure of [9] is highly similar to that of P. But the simulation results with QCADesigner show erroneous outputs when adding two more inputs just like the way in Fig. 7.

Figure 11d-f illustrate the average energy, average leakage energy, average switching energy dissipation for the majority gates listed. Although the average energy dissipation of the proposed design is not the optimal,

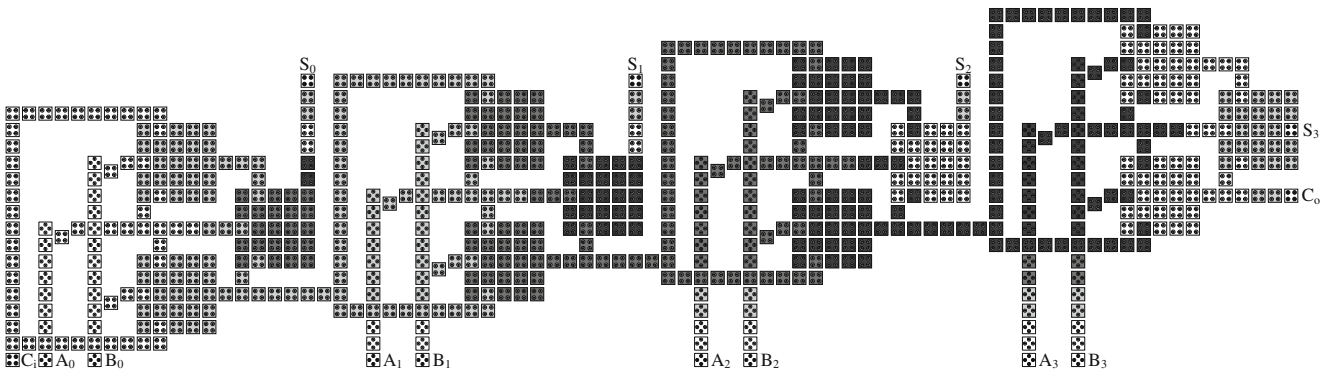

Fig. 10 Layout of the proposed 4-bit fault-tolerant adder with full adder P1

Table 3 Physical properties of different three-input majority gates

Gates	Area (μm^2)	Number of cells	Delay (clocks)	Fault tolerance (%)	Avg. energy diss. (meV)			Avg. leakage energy diss. (meV)			Avg. switching energy diss. (meV)		
					$0.5E_k$	E_k	$1.5E_k$	$0.5E_k$	E_k	$1.5E_k$	$0.5E_k$	E_k	$1.5E_k$
[26]	0.0034	5	0.25	0.00	3.64	4.49	5.60	0.64	2.02	3.58	3.00	2.47	2.02
[9]	0.0096	21	0.25	82.35	52.95	59.37	67.62	5.18	14.94	26.77	47.77	44.43	40.84
[7]	0.0096	13	0.50	55.56	33.83	37.26	41.39	2.61	8.26	15.44	31.22	29.00	26.48
[24]	0.0139	20	0.25	81.25	57.25	62.08	68.79	3.69	11.72	22.42	53.56	50.36	46.37
[38]	0.0388	43	0.25	97.44	85.62	116.49	152.86	26.26	68.65	113.96	59.36	47.85	38.90
[3]	0.0210	32	0.25	64.29	108.84	116.51	127.32	5.71	18.81	36.14	103.13	97.7	91.19
[8]	0.0135	19	0.25	60.00	53.44	58.43	65.03	4.00	11.77	21.74	49.44	46.66	43.29
P	0.0096	25	0.25	80.95	67.53	75.21	85.09	6.16	17.76	31.91	61.37	57.46	53.19

we can sum up that the three-input majority gate proposed in the paper displays significant practical value by comparisons and tradeoffs with previous proposed designs.

4.2 Five-Input Majority Gate

Table 4 displays the physical properties of different five-input majority gates. P is the proposed five-input majority gate. It is apparent that the fault tolerance of gate P is highest, achieving 47.62%, with relatively small area and number of cells. Figure 12 illustrate these characteristics lucidly. These characteristics make the design P a superior scheme. Although the structure of [31] is simplest, the fault tolerance of it is 0. Besides, the specificity of five inputs of design results in that the multi-layer structure must be needed if the design is employed to circuits. Analogous to above mentioned rotated cells, multi-layer structure is also a pitfall which has not been resolved so far. [1] in Fig. 5b, [1] in Fig. 5c and [8] can be regarded as a 3×3, 5×5 and 3×5 module respectively. As shown in Fig. 12c, the fault tolerance of [1] in Fig. 5b is 0. The structures of [1] in Fig. 5c and P are almost same apart from the positions of inputs and outputs. No matter from the view of

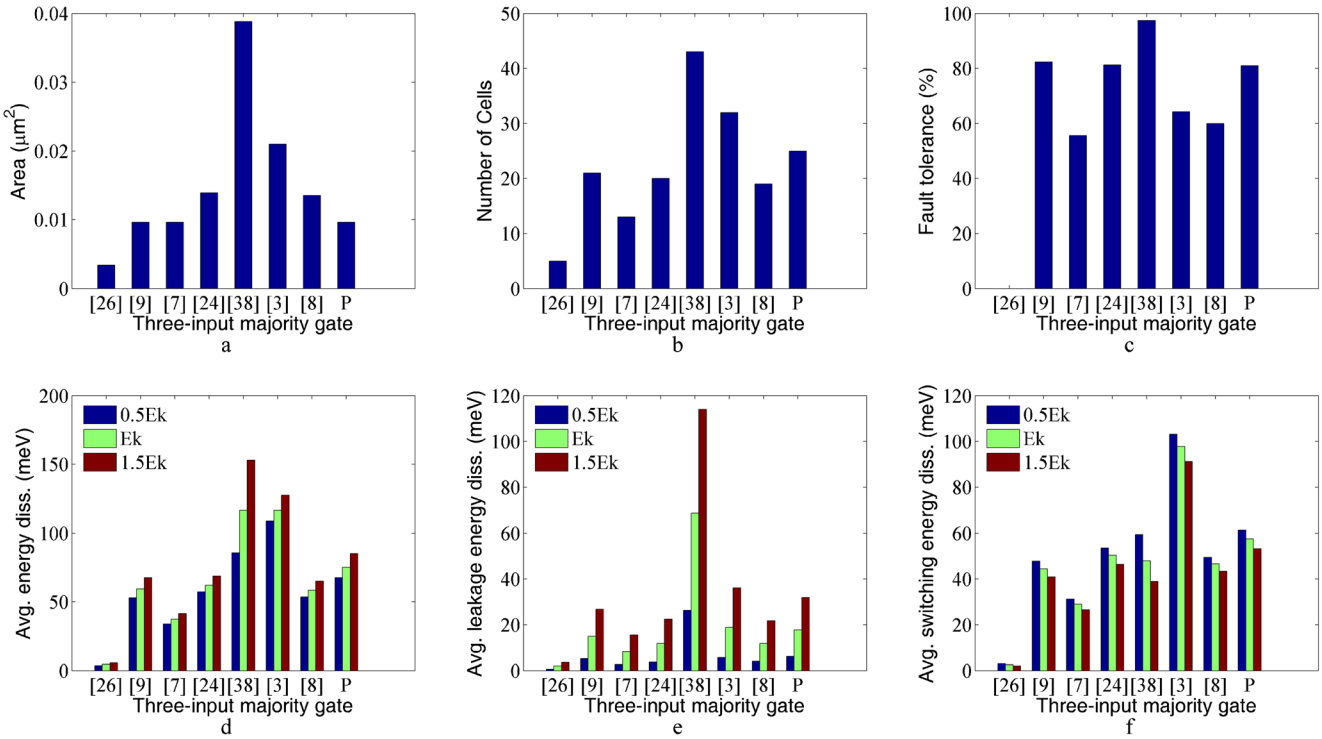

Fig. 11 Three-input majority gate properties **a** Area. **b** Number of cells. **c** Fault tolerance. **d** Average energy dissipation. **e** Average leakage energy dissipation. **f** Average switching energy dissipation

Table 4 Physical properties of different five-input majority gates

Gates	Area (μm^2)	Number of cells	Delay (clocks)	Fault tolerance (%)	Avg. energy diss. (meV)			Avg. leakage energy diss. (meV)			Avg. switching energy diss. (meV)		
					$0.5E_k$	E_k	$1.5E_k$	$0.5E_k$	E_k	$1.5E_k$	$0.5E_k$	E_k	$1.5E_k$
[31]	0.0076	10	0.25	0.00	12.81	14.51	16.85	1.28	4.14	7.69	11.53	10.37	9.16
[1]	0.0163	18	0.50	0.00	34.60	39.22	45.35	3.56	11.00	19.98	31.05	28.23	25.37
[1]	0.0246	33	0.25	18.52	93.10	101.49	113.02	6.36	20.34	38.18	86.74	81.15	74.84
[8]	0.0163	22	0.25	12.5	47.92	53.81	61.57	4.27	13.20	24.38	43.65	40.61	37.19
[13]	0.0344	42	0.25	44.44	133.96	144.17	158.40	7.67	24.91	47.43	126.29	119.26	110.97
[10]	0.0352	50	0.25	34.09	145.19	159.78	179.11	10.53	32.62	60.68	134.66	127.16	118.42
P	0.0135	27	0.25	47.62	63.02	70.87	81.05	6.24	18.40	33.08	56.78	52.47	47.97

area and number of cells or energy dissipation and fault tolerance, however, the design P surpasses the design in Fig. 5c. [8] has no significant difference compared with P in terms of area, number of cells and average energy dissipation. But the fault tolerance of it is far (35.12%) lower than that of P. [10, 13] both are magnificent structures with the bigger areas, the greater complexities, and the higher energy dissipations compared with other designs. However, neither [13] nor [10] can reach the same degree of fault tolerance of P, 3.17% and 13.53% lower than that of P respectively. Besides, the output cell of [10] is surrounded by other cells so that a multi-layer structure is needed to connect to circuits, which drastically reduces the feasibility of the scheme.

4.3 Proposed Multi-Bit Adders

The correct simulation results using QCADesigner verify the functional behaviors of the proposed full adders, as shown in Fig. 13a and b, respectively.

In order to judge the merits of the work, comparisons are made with other one-bit full adders with respect to area, delay and fault tolerance. Here, the reason why we don't involve energy dissipation is that QCAPro used in the

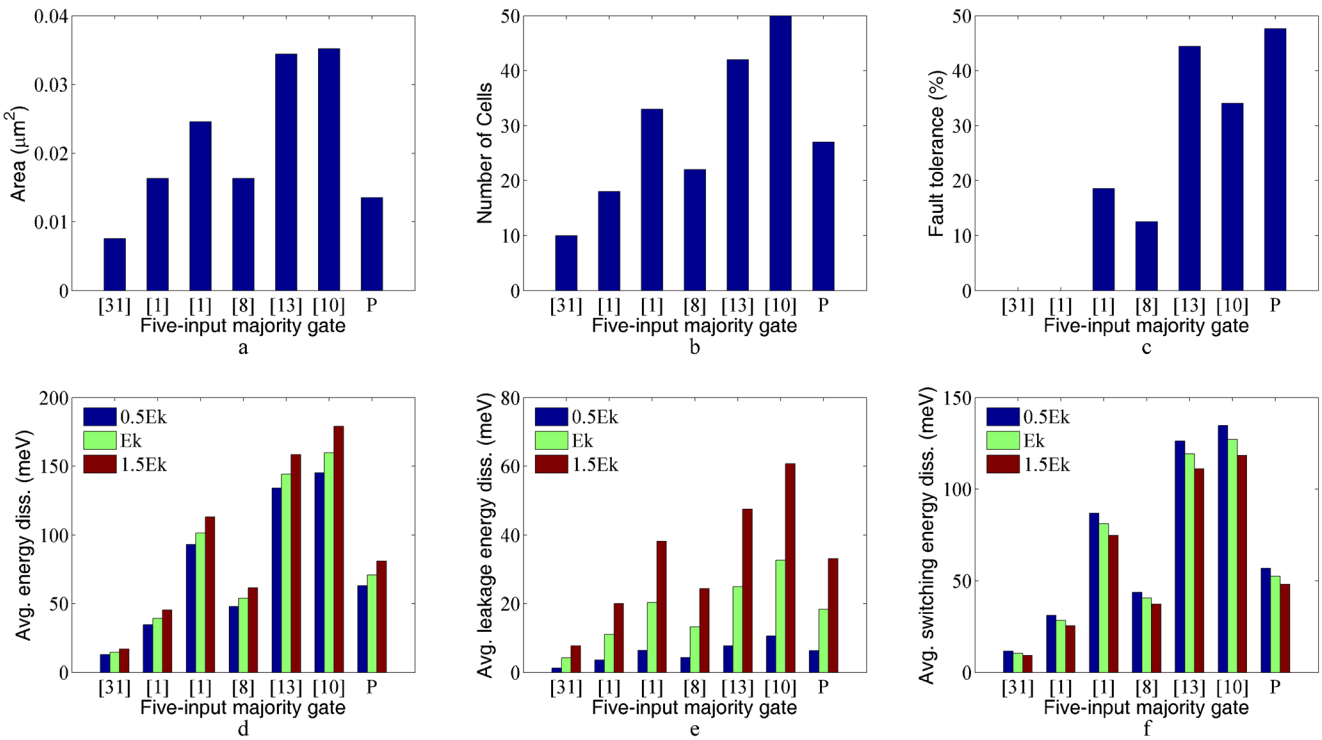

Fig. 12 Five-input majority gate properties **a** Area. **b** Number of cells. **c** Fault tolerance. **d** Average energy dissipation. **e** Average leakage energy dissipation. **f** Average switching energy dissipation

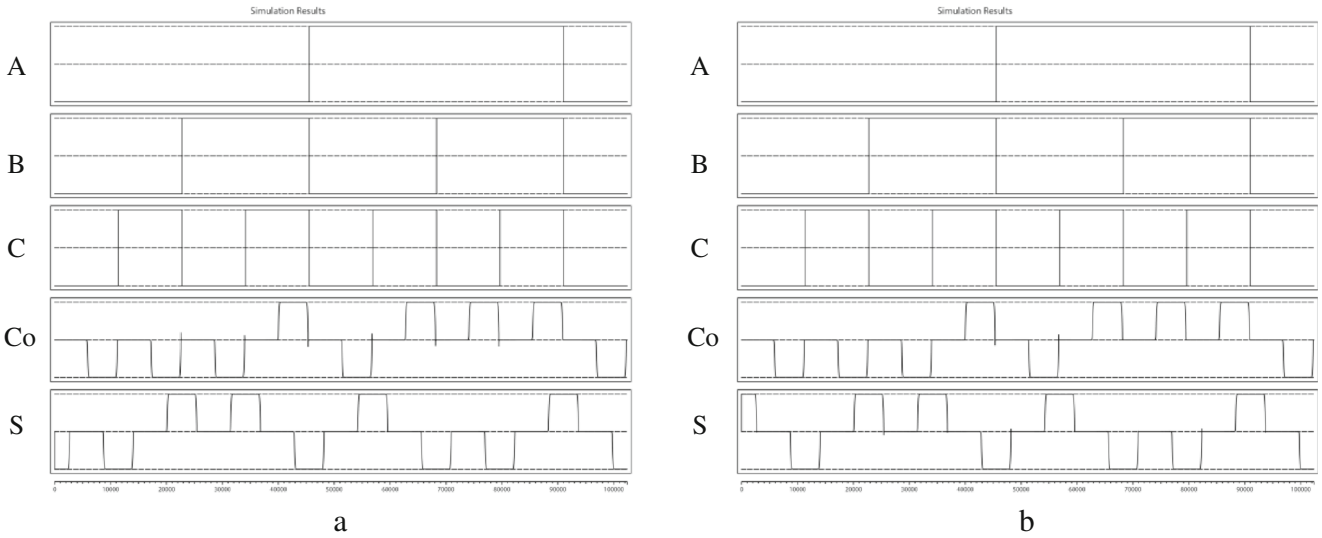

Fig. 13 Simulation results for full adders **a** P1. **b** P2

analysis of energy dissipation can be used for single-layer designs only, while most full adders are multi-layer constructions.

Table 5 presents the comparisons of full adders. Proposed one-bit full adders shown in Fig. 9a and b are labeled as P1 and P2 respectively. The areas of P1 and P2, shown in Fig. 14a, are in the middle position. P1 and P2 are both using three clock phases shown in Fig. 14b. The fault tolerance of carry of P1 and P2 is also high, achieving 85.12% and 93.58% respectively, which is at a higher level, as shown in Fig. 14c. What's more, as apparent from Fig. 14d, fault tolerance of sum of P1 and P2 is above all others, up to 59.5% and 41.28% respectively. Especially P1, the improvement of it is quite significant. Weighing up these factors, P1 and P2 are of great value.

Table 5 Physical properties of different full adders

Full adders	Area (μm^2)	Delay (clocks)	Fault tolerance-carry (%)			Fault tolerance-sum (%)			Crossing type
				Improvement (%)			Improvement (%)		
				P1	P2		P1	P2	
[20]	0.036	0.50	92.30	−7.78	1.39	17.94	231.66	130.10	Coplanar
[35]	0.010	0.75	72.22	17.86	29.58	22.22	167.78	85.78	Multilayer
[29]	0.025	0.75	87.88	−3.14	6.49	15.15	292.74	172.48	Multilayer
[16]	0.022	0.50	48.48	75.58	93.03	12.12	390.92	240.59	Multilayer
[21]	0.083	1.00	71.43	19.17	31.01	12.70	368.50	225.04	Coplanar
[42]	0.200	1.25	60.00	41.87	55.97	34.78	71.08	18.69	Coplanar
[6]	0.094	1.00	60.49	40.72	54.70	32.00	85.94	29	Multilayer
[37]	0.017	0.50	76.92	10.66	21.66	11.54	415.60	257.71	Multilayer
[2]	0.122	1.25	74.44	14.35	25.71	25.55	132.88	61.57	Coplanar
[8]	0.057	0.50	94.87	−10.28	−1.36	26.92	121.03	53.35	Multilayer
[36]	0.017	0.75	92.86	−8.34	0.78	17.86	233.15	131.13	Multilayer
[36]	0.014	0.75	88.89	−4.24	5.28	22.22	167.78	85.78	Multilayer
[31]	0.040	0.75	96.77	−12.04	−3.30	17.74	235.40	132.69	Multilayer
[49]	0.042	0.75	85.25	−0.15	9.77	39.34	51.25	4.93	Multilayer
[50]	0.050	0.75	75.38	12.92	24.14	33.85	75.78	21.95	Multilayer
P1	0.090	0.75	85.12	–	9.94	59.50	–	−30.62	Coplanar
P2	0.073	0.75	93.58	−9.04	–	41.28	44.14	–	Coplanar

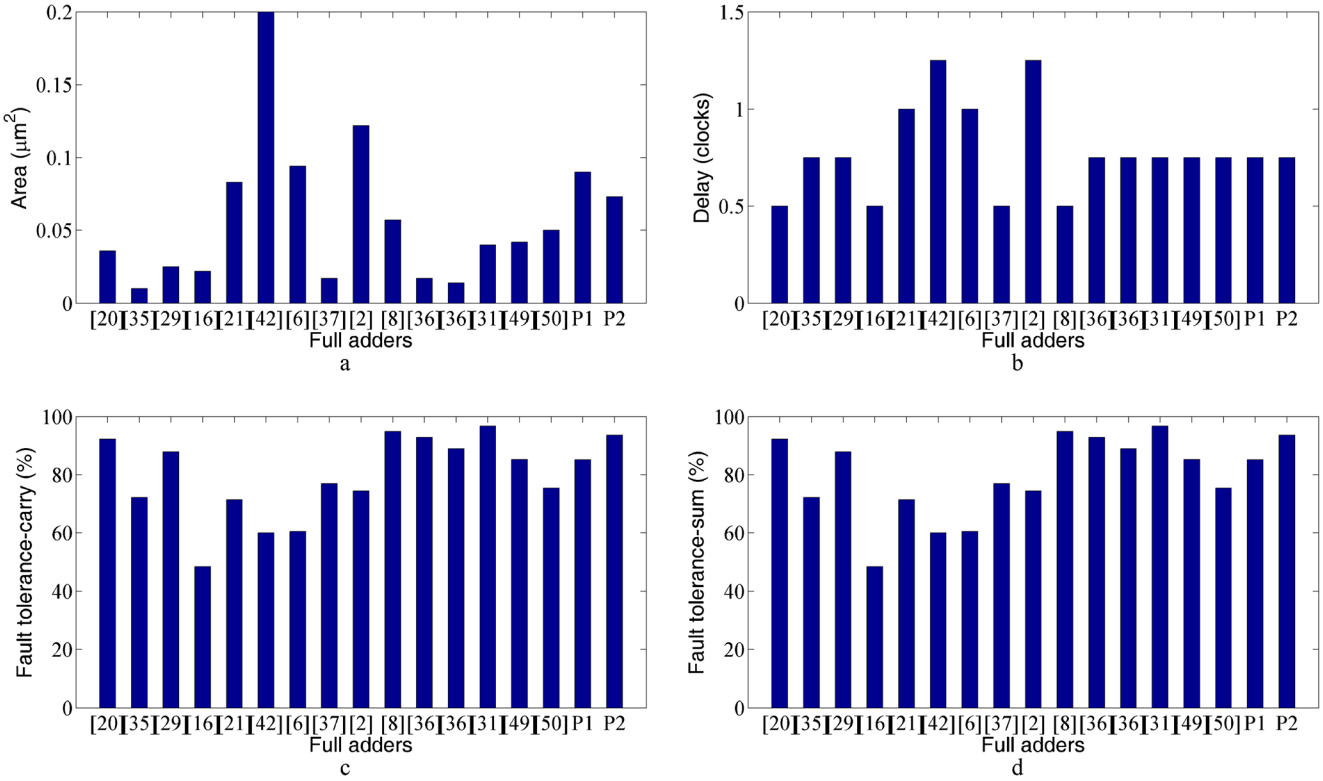

Fig. 14 Full adder properties **a** Area. **b** Delay. **c** Fault tolerance-carry. **d** Fault tolerance-sum

Table 6 lists the comparison for area of the multi-bit adders with several existing adders. To display the contrast effect of the area, the trend carves are made in Fig. 15a. Clock delay comparision is shown in Fig. 15b. Table 7 indicates the number of majority gates (MV), the number of inverters (INV), the number of crossings and the delay in various adders. The complexity of the adders is denoted as $M+I+C$, where M, I and C represent the number of majority gates, number of inverters, number of crossings, respectively, as demonstrated in Fig. 15c. Reference [28] described a criterion about the design of cost functions for QCA circuits as $Cost = (M^2 + I + C^2) \times T$, where T(clock cycles) is the delay of one circuit. Figure 15d illustrates the comparison of the QCA cost listed in Table 7. From the trend curves of 12 multi-adders in Fig. 15, it is found to be that P surpasses the huge majority adders, ranking the fifth in area, the fourth in complexity and cost. Only the multi-bit adders in [6, 37] are always superior to the proposed one in these three aspects. The multi-adders in [35] is also better than P in terms of area and cost but the complexity. The value of our proposed multi-adders, however, is the implementation of crossing with coplanar types while adders in [6, 35, 37] are multi-layer crossings. Although the multi-layer designs will be area-efficient, they bring the fabrication difficulty at the same time because the multi-layer crossovers require at least three layers to design the circuits. Note that P shows the best performance in the present of all the coplanar crossings. Combined with forementioned analysis, the proposed adders will be better alternatives.

Table 6 Area of multi-bit adders (μm^2)

Adders	4	8	16	32	64	128
[24]	1.0113	2.9838	9.8325	35.1453	132.2319	512.2486
[6]	0.4992	1.3312	3.9936	13.3120	47.9230	181.0400
[37]	0.1860	0.7810	3.2000	12.9540	52.1220	209.1010
[42]	4.532	19.0440	78.0200	315.7800	1270.532	5096.9640
[45]	4.5704	19.5688	80.9000	328.900	1326.25	5326.3500
[15]	0.986	3.5496	13.4096	52.0608	205.088	716.800
[47]	0.8976	3.536	14.0352	55.9232	223.258	506.412
[33]	0.6450	1.4980	3.5500	10.7700	31.2000	105.2800
[35]	0.177	0.7130	2.8600	11.4550	45.8500	183.450
[2]	0.9676	3.4748	13.0972	50.7740	199.8556	792.9308
[12]	0.7400	2.4600	8.8184	33.2088	128.684	506.412
P	0.7128	2.0212	6.2784	21.746	80.2332	307.4156

5 Conclusion

In this paper, we proposed a three-input majority gate based on a 5×5 module, the main method of module

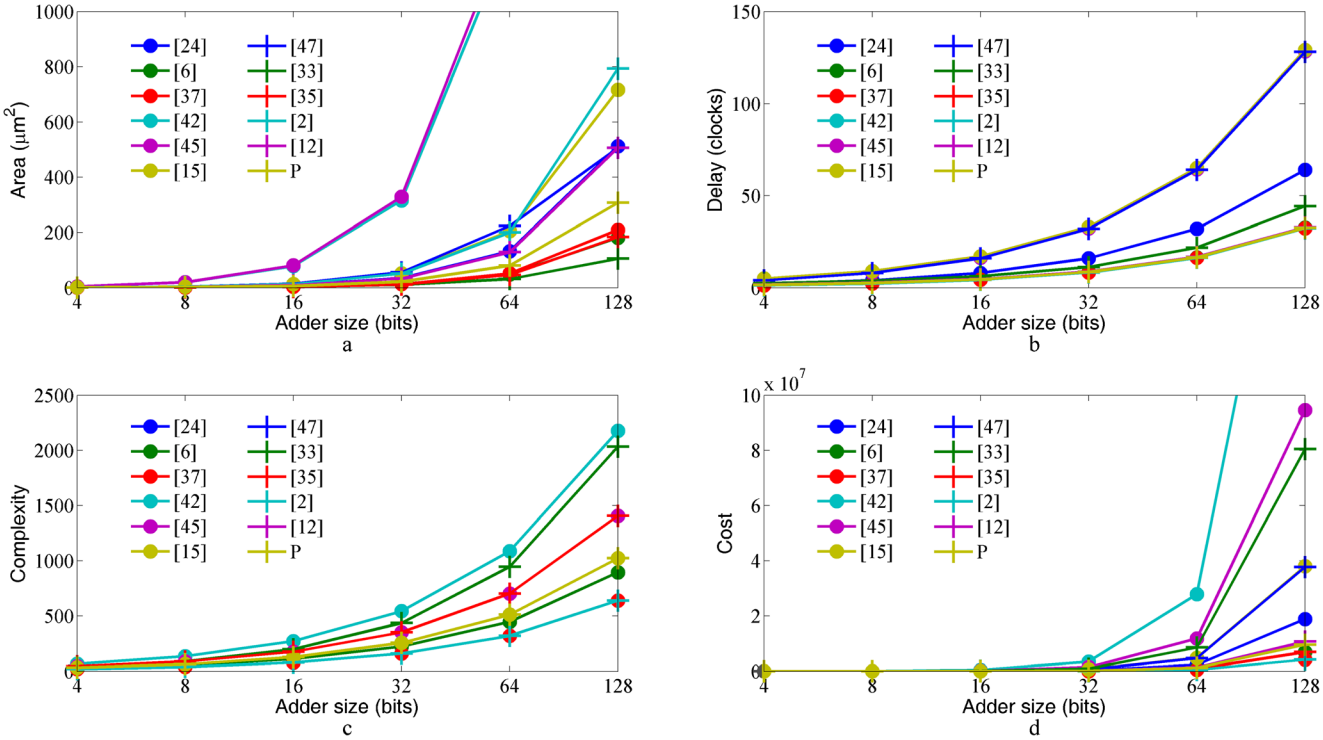

Fig. 15 Comparison of the proposed multi-bit adders to previous adders in terms of **a** Area. **b** Delay. **c** Complexity. **d** $Cost = (M^2 + I + C^2) \times T$

design methodology. Then a five-input majority gate was implemented with this gate by adding two more inputs on the basis of three-input majority gate, which distinguishes our designs from others. Both two designs showed better simulation results than prior work given area, number of cells, energy dissipation and fault tolerance into comprehensive consideration. Especially in fault tolerance, two designs are up to 80.95% and 47.62% respectively in the presence of one cell omission. One-bit full adders were implemented based on proposed three-input and five-input majority gates. Compared with existing designs, these two adders behave well, which verifies the practicability of the proposed majority gates at the same time. Moreover, to illustrate the applications of the proposed full adder and its scalability, the multi-bit designs were designed and also showed the better performance in terms of area, complexity and QCA cost in contrast to existing adders.

Table 7 Summary of n-bit adders

Adders	Number of MVs	Number of INVs	Number of crossings	Delay (Clock cycles)	Corssing type
[24]	$3n$	$2n$	$3n$	$(2n+3)/4$	Coplanar
[6]	$3n$	$2n$	$2n$	$(n+2)/4$	Multilayer
[37]	$2n$	n	$2n$	$(n+1)/4$	Multilayer
[42]	$5n$	$3n$	$9n$	$n+1/4$	Coplanar
[45]	$3n$	$2n$	$6n$	$n+1/4$	Coplanar
[15]	$3n$	$2n$	$3n$	$n+1$	Coplanar
[47]	$3n$	$2n$	$3n$	n	Multilayer
[33]	$8n-3log_2n-4$	n	$n(log_2n-3)+log_2n+3n+3$	$(2log_2n+3)/4+(n(log_2n+3))/32$	Multilayer
[35]	$2n$	$6n$	$3n$	$(n+2)/4$	Multilayer
[2]	$2n$	n	$2n$	$(n+1)/4$	Coplanar
[12]	$2n$	$2n$	$4n$	$(n+3)/4$	Multilayer
P	$3n$	$2n$	$3n$	$(n+2)/4$	Coplanar

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