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A New Capacitance-to-Frequency Converter for On-Chip Capacitance Measurement and Calibration in CMOS Technology

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Abstract In this paper, a new capacitance-to-frequency converter using a charge-based capacitance measurement (CBCM) circuit is proposed for on-chip capacitance measurement and calibration. As compared to conventional capacitor measurement circuits, the proposed technique is able to represent the capacitance in term of the frequency so that the variations can be easily handled in measurement or calibration circuits. Due to its simplicity, the proposed technique is able to achieve high accuracy and flexibility with small silicon area. Designed using standard 180 nm CMOS technology, the core circuit occupies less than 50 μm × 50 μm while consuming less than 60 μW at an input frequency of 10 MHz. Post-layout simulation shows that the circuit exhibits less than 3 % measurement errors for fF to pF capacitances while the functionality has been significantly improved.

Keywords Capacitance-to-frequency converter · Charge-based capacitance measurement · On-chip capacitance measurement and calibration · CMOS technology

1 Introduction

The process variations have always been one of the key issues in the robustness of CMOS integrated circuits especially in the mixed signal and RF circuits. For example, the variations of CMOS capacitances can be as large as 20 %. In the applications which heavily depend on capacitances accuracy, such as LC tank based voltage-controlled oscillator, the errors may introduce variations of operating frequency larger than 10 %, which is almost the tuning range of the oscillator in practice. Similar scenarios exist in the analogue-to-digital converters with high resolution, where well-matched capacitances are highly desired. Processing monitoring and calibration is hence of great interest to both microelectronics manufacturing and circuit designing [1–4]. The ring oscillator is a popular solution to track process variations, e.g., capacitance, in terms of frequency changes [4]. However, itself is very sensitive to many other variations, such as device sizes, supply voltage and temperature, etc.

It is not easy to extract the exact capacitance variations using a single kind of topology. To solve this issue, a new simple capacitance-to-frequency converter is proposed in this letter. It is able to transform the variations of capacitances in term of frequency changes with a considerably high accuracy, while maintaining a small silicon area and high flexibility in CMOS technology.

2 Design Considerations

The measurement of capacitance is an essential task in process characterisation. The CBCM technique has been a promising solution to measure on-chip capacitance for its high accuracy up to fF level. Figure 1 shows the topology of CBCM technique. Two non-overlap signals, V_p and V_n are applied to two inverters with and without load capacitors.

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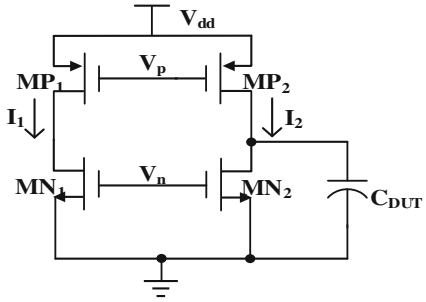

Fig. 1 The topology of CBCM

By comparing the current difference between the two inverters (with or without capacitor under measure), the load capacitance can be determined as:

$$C_{DUT} = \frac{I_2 - I_1}{V_{dd} f_{clk}} \tag{1}$$

where f_{clk} is the frequency of the square wave V_p and V_n.

However, this technique requires current meter in the measurement. Hence it is not suitable for on-chip calibration. Actually, the requirement for the on-chip capacitance variations measurement is quite different from conventional capacitance measurement. In such applications, no external current meter is available. However, only the variation of capacitance is required. For example, the percentage of variations over a reference capacitor is enough for the calibration of circuit performance. The simplest way to achieve this functionality is to use a ring oscillator to track the process variations. However, the oscillating frequency is highly dependent on other parameters, such as supply voltage, process corners of the transistors. Also, the operating frequency of the oscillator is never linear to the load capacitances due to non-linear effects of the circuits. These make the solution less attractive in the application of on-chip capacitance calibration.

It is observed that if the current difference in Eq. (1) can be replaced with some parameter that is easier to handle on-chip, such as frequency or period, the calibration of variations is possible. By combining the two above-mentioned solutions, a simple way for the capacitance variation monitoring can be performed in the following steps. By using the CBCM technique, the capacitance is calculated from the difference between the current of the two inverters. Then the current difference can be transformed into charge difference in reference capacitances, which subsequently results in the periodic difference in charging and discharging. Eventually, the capacitance is represented by differences in frequencies.

3 Proposed Design

A circuit can then be designed based on this idea. Figure 2 shows the topology of the proposed capacitor-to-frequency converter. In the capacitance measurement or calibration, each converter is loaded with different capacitances, and the differences in capacitance can be represented with different output period at V_{out}.

Compared with CBCM circuit in Fig. 1, by adding a tail MOS transistor MN_3, the current of the inverter is transformed into voltage. Then switches MP_3 and MN_4 are added to control the charge over capacitor C_{charge}. A comparator is used to compare the voltage at this capacitor with a threshold voltage V_{ref}. The operation of the circuit is described as follows. Initially, V_{ctrl} is low, the capacitor is being charged until the voltage of the capacitor, V_c increase to V_{ref}. The output of the comparator, V_{out} will consequently be logical high when V_c reaches V_{ref}. V_{out} is delayed as V_{ctrl} to control the switches which constitutes a feedback loop. In the delay time, V_{ctrl} keeps low and the capacitor keeps charging. When V_{ctrl} becomes high, the capacitor will be discharged immediately. Then the output of the comparator V_{out} and the output of the delay circuit V_{ctrl} will be low again, the circuit will come to the next period. Finally, the capacitor C_{charge} is charged and discharged to perform a periodical operation. Hence, the charging time, T is transformed to frequency, f_{out}. The current of the charging branch can be determined as:

$$I_c = \frac{V_{ref}}{T} C_{charge} \tag{2}$$

This relationship can be used to calculate or calibrate the capacitances. For example, two capacitors C_1 and C_2 are measured using two capacitance-to-frequency converters in Fig. 2. According to Eq. (2), we can get:

$$\Delta I_c = \frac{V_{ref}}{T_1} C_{charge} - \frac{V_{ref}}{T_2} C_{charge} \tag{3}$$

And the current difference ΔI is linear to ΔI_c:

$$\Delta I = \alpha \Delta I_c \tag{4}$$

Here, the coefficient α represents a linear relationship between ΔI and ΔI_c. It is a constant when the circuit parameters are all determined. Therefore

$$C_2 - C_1 = \frac{\Delta I}{V_{dd} f_{clk}} = \frac{\alpha \Delta I_c}{V_{dd} f_{clk}} \tag{5}$$

So by comparing the difference in period for the charging and discharging time among C_1 and C_2, the capacitance difference is now the time (or frequency) difference. The coefficient α in Eq. (4) varies with f_{clk}, C_{charge}, V_{ref} and device sizes of MP_2, MN_2, MN_3. It can be optimized to achieve high accuracy at desired range of measurement. Firstly, f_{clk} and component MP_2, MN_2, MN_3 determine the current consumption of the inverter. If the current consumption is too small, the V_c could not reach V_{ref}, leading to the failure of the circuit.

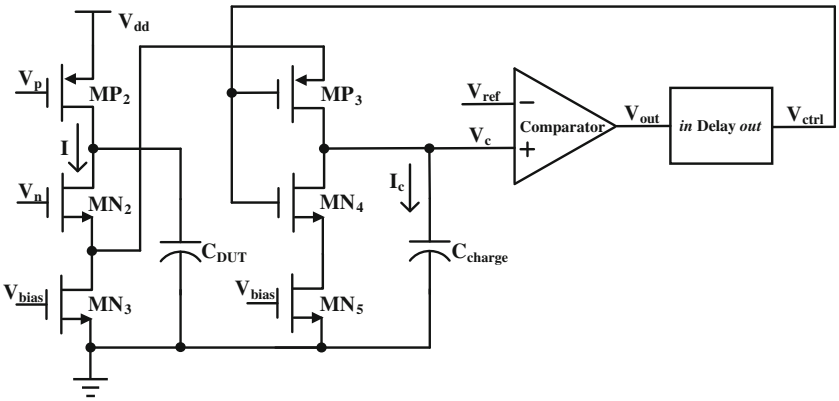

Fig. 2 The topology of the proposed capacitor-to-frequency converter

However, large current consumption leads to poor linearity. Secondly, V_{ref} and C_{charge} should be properly sized according to the range of capacitance under measure. Finally, the delay time is determined based on the discharged time of C_{charge}. It is important to make sure C_{charge} can be discharged to zero within the delay time.

4 Simulation Results

In the applications of mixed-signal and RF CMOS IC design, the typical capacitance is fF to pF. Hence the circuit in this work is optimized at such ranges. The circuit is implemented using a standard CMOS process. Only standard CMOS devices such as MOS transistors and capacitance are used in the circuit. It is optimized to measure fF to pF capacitance. For example, when V_{dd} = 1.8 V, f_{clk} = 10 MHz, C_1 = 302.5fF, C_2 = 1058.5fF, V_{ref} = 0.7 V, the delay time is 2us, the simulated V_{out} of the circuits with the two load capacitors are shown in Fig. 3. In this scenario, the circuit except the capacitance is less than 50 μm × 50 μm and consumes less than 60 μW.

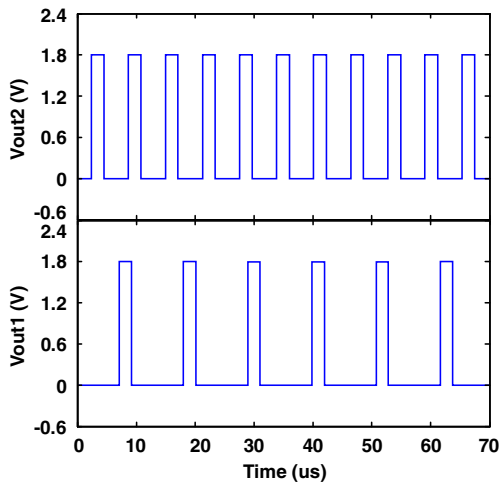

Fig. 3 The simulated V_{out} of the circuit

In Fig. 3, V_{out1} and V_{out2} exhibit obvious differences in phase and frequency. Based on this difference, the calibration can be performed on-chip using digital technique. Also, if the capacitance is measured, the proposed circuit can be used to calculate the capacitance like a conventional CBCM technique. In CBCM technique, the capacitance is calculated using current difference, while the frequency difference is used in the proposed circuit. According to the frequency of V_{out1} and V_{out2}, f_{out1} and f_{out2}, we can get different charging time T_1 and T_2. Using Eq. (3), the current difference ΔI_c can be calculated. Here we can get the linear relationship of ΔI_c and ΔI:

$$\alpha \approx 3.31 \tag{6}$$

We can compare with the conventional CBCM technique, here the measurement error of this circuit is 0.53 %. According to the range of capacitance under measure, we can modify f_{clk}, C_{charge}, V_{ref} and device sizes of MP_2, MN_2, MN_3 to obtain good linearity.

Several design considerations can be concluded as follows. The frequency of the clock signal and C_{charge} should be determined based on the considerations of operating speed and linearity of measurement results and the suitable range of the capacitance of C_{DUT}. As mentioned above, the increase of f_{clk} results in the increase of charging current I and consequently the decrease of the charging period of C_{charge}, which is preferred to the circuit speed. However, with high input frequency, f_{clk} and large capacitance, the measurement results of C_{DUT} exhibits a poor linearity. Therefore, f_{clk} and C_{charge} should be determined according to the range of capacitance under measure. For example, when the capacitance is around 10fF, we can increase f_{clk} to 100 MHz, which can be decreased to 5 MHz if the capacitance under measure is around 1 pF. The minimum reference frequency can be as low as 1 MHz if a lower speed operation is acceptable. Besides, the capacitance of C_{charge} can be set to 20 pF to keep a proper charging time difference. As for the design of comparator, the voltage reference and voltage offset should be considered based on the requirement of accuracy. In this design, V_{ref} is set to be

0.7 V considering the charging time of C_{charge} as well as the topology of the comparator. Since the accuracy of C_{DUT} is directly limited by the offsets of the comparator. In this work, simulations are carried out to ensure the robustness of this design. For example, we can manually add 5 mV offset voltage in the comparator, which is a typical value of offset in this kind of topology. The accuracy degrades by 0.7 %, which is quite acceptable in the proposed system. However, if the offset is increased to 15 mV, the accuracy can be degraded by more than 3 %, which is not acceptable. This ensures the proper operation of proposed system. As long as desired measurement range is determined, the circuit can be further optimized for smaller silicon area and higher accuracy. Post-layout simulations with process corners are performed to verify the functionality of the proposed circuit at a wide working range. The percentage of error in the circuits is summarized in Fig. 4. It is observed that the proposed circuit is able to provide a high accuracy (less than 2 % error) from fF to pF ranges.

Besides, according Eqs. (1)(3)(4), we can get:

$$\frac{1}{T_1}-\frac{1}{T_2}\propto C_{DUT} \tag{7}$$

where T_1 and T_2 can be directly calculated from f_{out1} and f_{out2}. Define the time reciprocal difference as delayed frequency difference (DFD). The linear relationship between this delayed frequency difference and capacitance under measure is also shown in Fig. 4. It is observed that the unified DFD exhibit a linear relationship with the capacitance under measure from fF to pF ranges. It suggests that the measurement or calibration can be performed on-chip precisely.

5 Conclusion

A capacitance-to-frequency converter is proposed. It can be used to measure the on-chip capacitance up to 1fF accuracy in term of output frequency measurement. More importantly, it is able to perform on-chip digital calibration regarding capacitance variations. The circuit is designed and simulated using a standard 180 nm CMOS technology, the core circuit occupies less than 50 μm × 50 μm and the building blocks of the circuits are standard CMOS circuits which can be easily configured for use at different operating frequencies, capacitance under measurement, and accuracy as well as for different CMOS technology nodes.

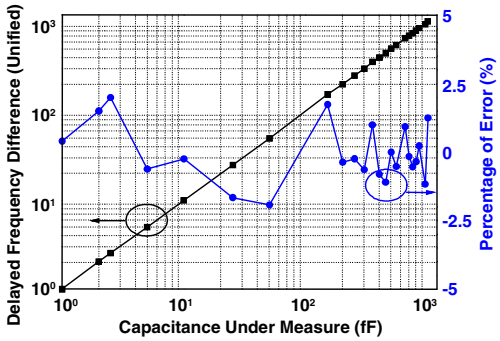

Fig. 4 Delayed frequency difference (unified) and percentage error

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