J Electron Test (2015) 31:43–52
DOI 10.1007/s10836-015-5507-7

A Power Efficient BIST TPG Method on Don't Care Bit Based 2-D Adjusting and Hamming Distance Based 2-D Reordering

Haiying Yuan · Kun Guo · Xun Sun · Jiaping Mei · Hongying Song

Received: 5 August 2014 / Accepted: 12 January 2015 / Published online: 17 February 2015

Abstract A power efficient BIST TPG method is proposed to reduce test power dissipation during scan testing. Before the test patterns are injected into scan chain, the test set adopts a series of preprocessed strategies including don't care bit based 2-D adjusting, Hamming Distance based 2-D reordering and test cube matrix based two transpose, all steps will be orderly executed in interspersed way. The six largest ISCAS'89 benchmark circuits verify the proposed method. Experimental results show that the switching activities are effectively reduced when the test set is loaded for on-chip scan testing. ASDFR with MT-filling scheme ensures high compression ratio, the scan-in test power dissipation is further decreased by don't care bit based 2-D adjusting and Hamming Distance 2-D reordering. In addition, the BIST TPG method with less test application time and smaller algorithm complexity can be widely applied to actual chip design without adding extra decoder area overhead.

Keywords Test data compression · Scan-in test power dissipation · Area overhead · Don't care bit adjusting · Hamming distance reordering

Responsible Editor: C. A. Papachristou

H. Yuan (✉) · K. Guo · J. Mei · H. Song
College of Electronic Information and Control Engineering, Beijing University of Technology, Beijing 100124, China
e-mail: yhyingcn@gmail.com

X. Sun
Department of Electronic Engineering, Tsinghua University, Beijing 100084, China

1 Introduction

New fabrication technologies and design complexities, multiple cores embedded are rapidly emerging in System-on-Chip (SoC) and Very Large Scale Integration (VLSI) [4]. Built-in self-test (BIST) is widely applied to the Design for Testability (DFT), Automatic Test Pattern Generation (ATPG) is important to these test technologies, which involves a series of thorny issues such as high test power dissipation, large test data volume and extra area overhead.

Generally, test data volumes can be reduced through three test compression techniques including linear decompression based scheme, broadcast scanbased scheme and code based scheme [13], which are directly applied to current test patterns and avoid any ATPG or fault simulation [15]. Among them, the code based scheme doesn't require circuit structural information and it is suitable for intellectual property cores, so it is preferred in test data compression. There includes Huffman coding [9], Golomb coding [3], Count Compatible Pattern Run-Length Coding (CCPRL) [16], Frequency-Directed Run-Length (FDR) coding [5], Alternating Run-Length (ARL) coding [6], Extended Frequency-Directed Run-Length (EFDR) coding [7], etc.

In addition, a circuit or system with increased more switching activities consumes more power dissipation in test mode than it does in normal mode [2], because there are some logic state transitions within each test pattern or between two consecutive test patterns. The surging scan-in test power dissipation caused by the instantaneous current in test mode may create enormous damages to circuit with excessively high switching activities. So two techniques have been developed to effectively reduce test power dissipation, One is to modify the conventional LFSR configurations, such as LP-TPG [1], DS-LFSR [14] and LT-TPG [12], etc. Another is to decrease the number of transitions during Circuit under Test (CUT) test

such as test patterns reordering, scan cells reordering and favorable X-filling schemes, etc. [2].

This paper proposed the power efficient BIST TPG method based on don't care bit based 2-D adjusting, Hamming Distance based 2-D reordering and ASDFR with MT-filling scheme. The six largest ISCAS'89 benchmark circuits verify the proposed method. It not only effectively decreased scanned-in test power dissipation, but also obtained a high compression ratio, consumed less test application time and avoided adding extra area overhead.

2 Background

Three concepts are involved in the proposed BIST TPG method.

2.1 Scan-in Test Power Dissipation Model

The test power dissipation caused by the switching activities can be effectively reduced by decreasing the number of logic state transitions of test set [2]. Scan-in test power dissipation is proportional to the switching activities of test pattern. In addition, other activities such as scan-in operation, scan-out operation and their transition operation between these two [11] all contribute to the number of logic state transition in test pattern and test power dissipation.

Scan-out response heavily relies on scan-in test pattern, so we only focus on scan-in operation. The weighted transition metric (WTM) model [4] is presented to estimate scan-in test power dissipation of a given test pattern, which depends on not only the number of logic state transitions but also their relative positions.

Considering a test set as $T=\{T_1,T_2,T_3,\cdots,T_m\}$, the length of each test pattern is n. Every test pattern can be expressed as $T_i=\{t_{i1},t_{i2},\cdots,t_{in}\}$, $1\le i\le m$, $1\le j\le n$, t_{ij} denotes the j^{th} bit of the i^{th} test pattern. Therefore the weighted transitions metric WTM_i, average scan-in power dissipation P_{avg} and peak scan-in power dissipation P_{peak} are estimated as follows:

$$WTM_i = \sum_{i=1}^{n-1}(n-j)*\left(t_{i,j}\oplus t_{i,j+1}\right) \quad (1)$$

$$P_{avg} = \frac{\sum_{i=1}^{m} WTM_i}{m} \quad (2)$$

$$P_{peak} = \max_{1\le i\le m} WTM_i \quad (3)$$

According to the above formula, three parameters can be calculated to evaluate test power dissipation of a test pattern during scan-in operation. An important conclusion can be drawn from the analysis of scan-in test power dissipation model, different X-filling schemes [2] and different ordering strategies [10] besides the logic state transitions all affect test power dissipation.

2.2 Test Power Dissipation Estimated for Filled Test Set

In scan-based BIST, a test pattern that detects many targeted faults may contain a large number of don't care bits (X) [2]. In conventional scan ATPG, each X bit in test pattern is filled with 0 or 1 at random since this will not affect the fault coverage. Actually, the number of X bits in a test set is typically large. The X-filling scheme randomly assign a 0 or 1 to X bits in test set so that the number of logic state transitions in scan cells is minimized, which reduces the overall switching activity in Circuit under Test (CUT) during shift cycles [1]. Table 1 shows WTM comparison in two groups of test sets with four test patterns filled by different filling scheme such as 0-filling, 1-filling and Minimum Transitions filling (MT-filling) [2].

From the above two groups of test sets, 0-filling scheme and 1-filling scheme just show similar results in the evaluation

Table 1 WTM comparison of two test sets

Test pattern	0-filling scheme		1-filling scheme		MT-filling scheme	
	Filled pattern	WTM	Filled pattern	WTM	Filled pattern	WTM
10X1111XX0	1001111000	201	1011111110	180	1001111110	169
0XXXXXXX1	0000000001		0111111111		0000000001	
XX01XXXX11	0001000011		1101111111		1101111111	
11110000XX	1111000000		1111000011		1111000000	
1XX0000XXX	1000000000	122	1110000111	153	1110000000	82
X1XXXX0XXX	0100000000		1111110111		0111110000	
X0000011XX	0000001100		1000001111		0000011111	
XXXXXXXX0X	0000000000		1111111101		1111111100	

of WTM, but MT-filling scheme shows obvious reduction in test power dissipation. So MT-filling scheme is regarded as the power efficient filling method, the scan-in test power dissipation and compression ratio will be further considered in the proposed BIST TPG method.

2.3 Run Length Based Code Scheme

The run length based code scheme has been widely applied to test data compression in BIST. Jas and Touba proposed run-length codes to encode runs of 0s to reduce test data volumes. Then Golomb code was proposed by Chandra and Chakrabarty to encode runs of 0s with variable length code which allows efficient encoding of longer runs [1], however it requires a synchronization mechanism between the tester and the chip. Then they proposed a new scheme named Frequency-Directed Run length (FDR) code [5] with the variable group size compared with Golomb code. It is very efficient for FDR code to compress test data which has few 1s but long runs of 0s. Maleh and Abaji further proposed an Extension of FDR (EFDR) which encodes both types of runs to remedy the defects of the FDR. Therefore, EFDR code outperformed FDR code when the test data has few 0s [7].

For further improving the compression ratio, Hellebrand and Wurtenberger proposed an evolution in alternating run-length code called Alternating Shifted FDR (ASFDR) to reduce the SoC test data volumes [8]. This method has no run-length of zero size, and codeword for run length size 0 is unnecessary. This codeword is assigned to run length size 1 and each codeword is shifted to one position higher. It obtains higher compression ratio compared with Alternating FDR. The test data compression example of two tests is shown in Table 2.

The coding results show that ASFDR scheme has higher compression ratio than EFDR scheme does. In addition, an on-chip decoder with an acceptable area overhead is required to load encoded test data from Automatic Test Equipment (ATE).

3 Proposed BIST TPG Method

Hamming distance based reordering [11] should satisfy the following two facts: ① ATPG derived test patterns contain a large amount of don't care bits [2]. ② Stuck-at faults based test patterns can be reordered without any loss of fault coverage, but the corresponding fault free outputs that are stored in ATE as golden references must be also reordered in the same sequence. In order to reduce scan-in power dissipation of test pattern and obtain high compression ratio in run-length coding, the test set will be preprocessed in accordance with the following procedure.

A given test set T $\{O_1, O_2, O_3, O_4\}$ composed by four test patterns with ten bits is involved in the experiments.

O_1: 0010100011
O_2: 0XX1000110
O_3: 11X01XX01X
O_4: 10XX1XXXXX

(1) don't care bit based first adjusting

The test sets are reordered according to the numbers of don't care bit in each test pattern from more to less, so they are reordered as follows:

O_4: 10XX1XXXXX
O_3: 11X01XX01X
O_2: 0XX1000110
O_1: 0010100011

During don't care bit based first adjusting, the location of test pattern in test set will be interchanged. Test pattern

Table 2 Test data compression example

Type	EFDR with MT-filling scheme		ASFDR with MT-filling scheme	
	1st pattern	2nd pattern	1st pattern	2nd pattern
Original test set	1001111110	1110000000	1001111110	111 0000000
	0000000001	0111110000	0000000001	0 11111 0000
	1101111111	0000011111	1101111111	00000 11111
	1111000000	1111111100	1111000000	11111111 00
Bits number	40	40	40	40
Encoded test set	1000001101	1100001100	1000110111	1100011000
	0011001010	0011001011	1001110000	1101011001
	1111010001	0001111010	0110100101	011011001
	010	1000	1	
Bits number	33	34	31	29
Compression ratio	17.5 %	15 %	22.5 %	27.5 %

with more don't care bits will be changed to the front position as much as possible.

(2) hamming distance based first reordering

The test pattern (O_4) with maximum don't care bits is always placed on the first position in above test sequence. So it is selected as the new first test pattern in the reordered list. The reason for selecting the test pattern with minimum don't care bit is that there is a minimum flexibility for don't care bit mapping.

Hamming Distance is defined as the distance between two test patterns equal to the number of corresponding mismatched bits, and it is calculated by bit position wise [11]. Hamming Distances from the first test pattern (O_4) in adjusted list to all remaining patterns (O_3, O_2, O_1) are calculated respectively. The test pattern with the minimum Hamming Distance from the first test pattern (O_4) will be placed next to it.

Let's find out the Hamming distance between the first test pattern (O_4) and test pattern (O_3), Here we will compare each bit from O_4 with each bit in same position from O_3, If O_4 (i)=O_3 (i) or O_4 (i)= X or O_3 (i)=X, then Hd (i)=0, otherwise Hd (i)=1. So total Hamming Distance between O_4 and O_3 is the sum of Hd(i). For given test set, let's calculate the Hamming distance for all test patterns.

O_4: 10XX1XXXXX
O_3: 11X01XX01X (H_d between O_4 and O_3 is 1)
O_2: 0XX1000110 (H_d between O_4 and O_2 is 2)
O_1: 0010100011 (H_d between O_4 and O_1 is 1)

As test pattern O_3 has minimum Hamming distance from the first test pattern O_4, we will put test pattern O_3 at the second position of new list. Now remaining patterns will be compared with O_2 and O_1, then O_1will be searched and placed based on Hamming distance from the second test pattern O_3. The reordering continues until the last test vector is found. The reordered test set is shown as follows:

O_4: 10XX1XXXXX
O_3: 11X01XX01X
O_1: 0010100011
O_2: 0XX1000110

(3) the first matrix transpose

Considering the given test set as a matrix with the size of 4×10, where 4 is the number of test pattern and 10 is the bits number of each test pattern. Let's clustering don't care bit in each test pattern, so the columns with matched bits should be placed nearby. Then the transpose matrix of the reordered test set is found.

T_1: 1100
T_2: 010X
T_3: XX1X
T_4: X001
T_5: 1110
T_6: XX00
T_7: XX00
T_8: X001
T_9: X111
T_{10}: XX10

(4) don't care bit based second adjusting

All rows are reordered according to the numbers of don't care bit from more to less, the row T_3 with the most don't care bit is always regarded as the new first row.

T_3: XX1X
T_6: XX00
T_7: XX00
T_{10}: XX10
T_2: 010X
T_4: X001
T_8: X001
T_9: X111
T_1: 1100
T_5: 1110

In don't care bit based second adjusting, the location of don't care bits in each test pattern will be interchanged, and don't care bits will be changed to the front position as much as possible.

(5) hamming distance based second reordering

The new first row T_3 remains fixed, the Hamming Distance based reordering of remaining all rows from the new first row T_3 is calculated and compared. As the row T_{10} has minimum Hamming distance from row T_3, it is put at the second position of new list. The hamming distance based second reordering is shown as follows.

T_3: XX1X
T_{10}: XX10
T_5: 1110
T_6: XX00
T_7: XX00
T_2: 010X
T_1: 1100
T_4: X001
T_8: X001
T_9: X111

(6) the second matrix transpose

At the end of the second hamming distance reordering, the reordered list is obtained. Then, it will be transposed

again. So the required test set is obtained from the transpose matrix composed by the reordered test pattern.

N_1: XX1XX01XXX
N_2: XX1XX11001
N_3: 1110000001
N_4: X0000X0111

(7) MT-filling scheme

The proposed TPG method is applied to the test set with four test patterns. Before evaluating the scan-in test power dissipation and the compression ratio, these don't care bits in test set are completely filled and shown in Table 3.

In Table 3, different X-filling schemes applied to test set seriously affect the compression ratio and scan-in test power dissipation. Usually, MT-filling scheme can do better in decreasing the number of switching activities than 0-filling scheme and 1-filling scheme do. Here, don't care bit 2-D adjusting effectively reduces the value of WTM. Hamming distance 2-D reordering further decreases the test power dissipation.

4 The Decoder Architecture and Area Overhead

The run length based code scheme needs an on-chip decoder which loads the encoded test data from ATE, and then decodes them for on-chip scan testing. For showing it holds true in an actual chip design, the test application time, the decoder architecture and decoder area overhead are also considered in the proposed scheme.

4.1 The Decoder Architecture

Figure 1 improves the decoder by inserting a bit swapping logic array before the test patterns injected to single/parallel scan chains for on-chip testing. For all the test sets, don't care bit adjusting and bits swapping in test pattern can be performed by programming the on-chip FPGA. As long as a good control in higher clock speeds of the BIST state machine to generate normal speed test pattern, don't care bit based 2-D adjusting and Hamming Distance based 2-D reordering can perform well during the test set encoding and decoding.

4.2 The Decoder Area Overhead

Table 4 compares the decoder area overhead with different coding methods. The decoder area overhead is computed as: (area of decoder*100)/(area of benchmark circuit), area of decoder includes hardware overhead of the core FSM decoder and bit swapping logic array. The proposed BIST TPG method applied with EFDR/ASFDR only requires the basic decoder, which totally avoids difference test pattern method [11]. So it neither requires any CSR nor involves any delay caused by CSR, but only needs a different routing for scan-in operation.

Compared with CSR decoder structure, the proposed BIST TPG method needs simpler decoder architecture. Obviously, the improved decoder does not consume extra area overhead. So it is easy to implement in an actual chip design.

4.3 A Decoding Example

Recalled a given test set involved in section 3, it is assumed that test set T with four original test patterns {O1, O2, O3, O4} is turned into test set N with four new test patterns {N1, N2, N3, N4}, then encoded by EFDR/ASFDR. The encoded test set needs to be decoded before it is applied to scan testing. However, the orders of scan-in test pattern are not considered. Thus, bits swapping in each test pattern are considered during decoding process, the routing decoder of a given test set is designed. Figure 2 shows the encoded test set is successfully decoded by don't care bit adjusting and bit swapping operations, and then loaded into scan chain for on-chip testing.

Table 3 Compression result comparison with different method

Test pattern	0-filling scheme [2]		1-filling scheme [2]		MT-filling scheme [2]	
	HDDR+ PEBF [11]	HDDR+ PEDCBC	HDDR+ PEBF [11]	HDDR+ PEDCBC	HDDR+ PEBF [11]	HDDR+ PEDCBC
N_1:XX1XX01XXX	0000111100	0010010000	0000111100	1111101111	0000111100	1111101111
N_2:XX1XX11001	1000001000	0010011001	1110111111	1111111001	1110011111	1111111001
N_3:1110000001	1001010100	1111000001	1111111100	1111000001	1111111100	1110000001
N_4:X0000X0011	0000000111	0000000111	0001100100	1000010011	0000000111	0000000111
P_{peak}	36	24	17	20	12	9
P_{avg}	15.8	14.5	10	10	6.3	6
Compression ratio for EFDR	−5 %	0 %	7.5 %	2.5 %	10 %	12.5 %
Compression ratio for ASFDR	−15 %	0 %	15 %	15 %	20 %	15 %

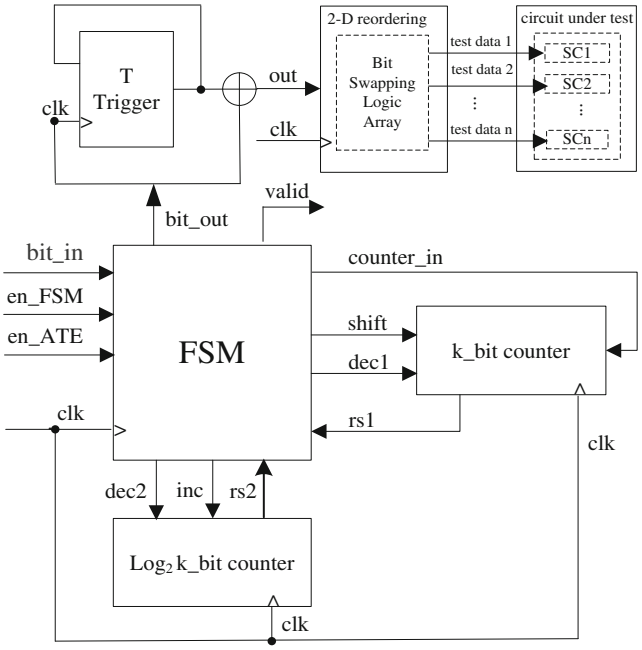

Fig. 1 The decoder architecture

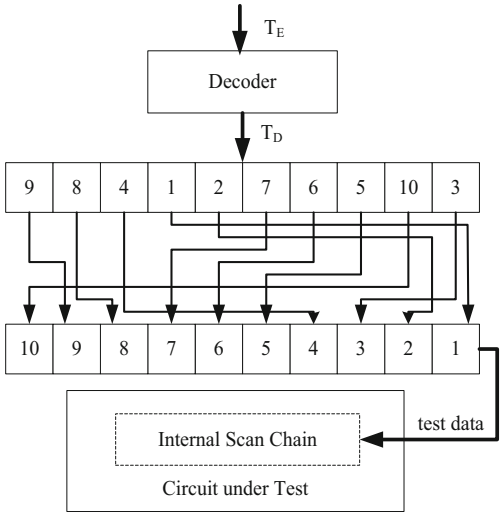

Fig. 2 The decoder architecture of a given test set

The power efficient test set consumes less test power dissipation under the conditions of high compression ratio. As for the architecture complexity of BIST circuit consuming more power especially in deep submicron designs which have high transistor leakage, this paper evaluates scan-in test power dissipation by WTM model, then it is further synthesized and simulated at the gate level for each ISCAS'89 benchmark circuit in section 5.

4.4 Performance Comparison with Previous Works

This paper provides extensive discussions about decoder area overhead, scan-in test power dissipation, test application time and algorithm complexity analysis. Table 5 gives the performance comparisons of some evolution methods.

Compared with existing commercial methods, the proposed BIST TPG method has obvious advantage. The test power dissipation is reduced without affecting test application time and the improved decoder is implemented without adding extra area overhead, which indicates this scheme holds true in an actual chip design.

Table 4 The decoder area overhead

Circuits	FDR [5]	EFDR [7]	Proposed scheme with EFDR	ASFDR [8]	Proposed scheme with ASFDR
S5378	7.8	8.3	8.5	8.2	8.6
S9234	5.9	6.3	6.5	6.1	6.6
S13207	3.5	3.7	3.9	3.8	3.9
S15850	3.6	3.8	4.1	3.9	4.1
S38417	1.4	1.5	1.7	1.7	1.9
S38584	1.5	1.6	1.8	1.6	1.9

5 Simulation Experiment and Results Analysis

5.1 Compression Ratio Comparison

The proposed BIST TPG method is verified by ISCAS'89 benchmark circuits with full-scan chain, the test set obtained from Mintest ATPG program is involved in experiment verification, it was performed on a workstation with a 2.5GHz Intel Core processor and 4G of memory. Before the test patters are injected into scan chain, don't care bits based 2-D adjusting, Hamming Distance based 2-D reordering were in turn applied to the Mintest test set, don't care bits were filled by MT-filling scheme and then encoded by EFDR [7] and ASFDR [8], encoded test set is obtained from these codeword. Assuming T_D and T_E respectively denote the Mintest test set and encoded test set obtained from the proposed BIST TPG method. The compression ratio is calculated by formula (4):

$$\mathrm{CR}\% = \frac{T_D - T_E}{T_D} \times 100\% \quad (4)$$

Table 6 compares the compression ratio obtained by different test set preprocessed methods. For EFDR with MT-filling scheme, the proposed BIST TPG method (HDDR+PEDCBC) shows obvious advantages over than EFDR and the 2-D reordering method (HDDR+PEBF) [11], and the average compression ratio reaches to 72.14 %. For ASFDR with MT-filling scheme, the similar conclusions can be drawn, and the average compression ratio reaches to 72.96 %.

Table 5 Performance comparison of some evolution methods

Some evolution methods	Data compression	Test power	Area overhead	Type of testing	
				Scan-in	functional
EFDR [7] / ASFDR [8]	√	×	√ (decoder)	√	
Vector reorder	√	×	×	√	
Vector reorder and differentiated [1]	√	×	√ (CSR)	√	
Vector reorder, differentiated and EFDR / ASFDR	√	×	√ (decoder + CSR)	√	
Hamming distance based reorder and column-wise bit stuffing with difference vector [10]	√	×	√	√	
Hamming distance based double reordering with power efficient bit mapping [11]	√	√	√	√	√
Don't care bit 2-D adjusting and hamming distance based 2-D reordering	√	√	√ (improved decoder)	√	√

5.2 Scan-in Test Power Dissipation

The proposed BIST TPG method adopts a series of adjusting and reordering strategies to preprocess the test patterns before the test set is loaded for scan testing. Here, don't care bit based 2-D adjusting makes a large reduction of WTM during scan-in operation. Hamming Distance 2-D reordering is further applied to the adjusted test set to eliminate test power dissipation. Table 7 compares scan-in test power dissipation of the encoded test set with different X-filling schemes.

Firstly, don't care bits in original test set are filled by two filling schemes, the experimental results show that MT-filling scheme has obvious advantages in decreasing test power dissipation than 0-filling scheme does. When don't care bits in test pattern are completely filled by MT-filling scheme, scan-in test power dissipation can be evaluated. The peak test power and average test power in the proposed BIST TPG method (HDDR+PEDCBC) are obviously lower than 2-D reordering method (HDDR+PEBF) [11]. And the average reductions of the peak test power and average test power reach to 35.14 % and 43.01 % respectively.

5.3 Algorithmic Complexity Analysis

HDDR+PEDCBC EFDR/ASFDR with MT-filling scheme is based on WTM power model, the test pattern generation include EFDR/ASFDR encoding, don't care bit adjusting and filling, Hamming Distance 2-D reordering. These operations devote to reducing the test power dissipation during scan testing, which seems to make the BIST TPG method more

Table 6 Compression ratio comparison with previous works

ISCAS'89 Circuit	Total bits in original test set	Size of Mintest test set	% Compression with EFDR			% Compression with ASFDR		
			EFDR [7]	HDDR+ PEBF+ EFDR [11]	HDDR+ PEDCBC+ EFDR	ASFDR [8]	HDDR+ PEBF+ ASFDR [11]	HDDR+ PEDCBC+ ASFDR
S5378	23,754	20,758	51.93	53.47	54.81	-NA-	53.99	57.09
S9234	39,273	25,935	45.89	51.76	60.60	44.96	52.03	61.76
S13207	165,200	163,100	81.85	82.38	88.51	80.23	82.41	88.63
S15850	76,986	57,434	67.99	70.15	78.45	65.83	70.24	78.59
S38417	164,736	113,152	60.57	57.74	77.51	60.55	57.78	78.71
S38584	199,104	161,040	62.91	67.91	72.94	61.13	68.02	72.95
Avg.	–	–	61.86	63.90	72.14	62.54	64.08	72.96

Table 7 Test power dissipation comparison

ISCAS circuit	Original test set with 0-filling [2]		Original test set with MT-filling [2]		HDDR+PEBF ASFDR with MT-filling [11]		HDDR+PEDCBC ASFDR with MT-filling		Reduction % than [11]	
	P_{peak}	P_{avg}	P_{peak}	P_{avg}	P_{peak}	P_{avg}	P_{peak}	P_{avg}	P_{peak}	P_{avg}
S5378	10,127	3336	9531	2435	5010	1357	3968	1097	26.25	19.12
S9234	12,994	5692	12,060	3466	6667	1901	4354	1302	34.69	31.51
S13207	101,127	12,416	97,606	7703	37,972	4685	19,386	1362	48.95	70.93
S15850	81,832	20,742	63,478	13,381	34,974	8466	21,910	3303	34.40	60.99
S35932	172,834	73,080	125,490	46,032	8292	3510	5904	3073	28.80	12.45
S38417	505,295	172,665	404,617	112,198	205,989	88,091	82,932	24,092	59.74	72.65
S38584	531,321	136,634	479,530	88,298	182,769	45,467	158,790	30,203	13.12	33.43
Avg.	–	–	–	–	–	–	–	–	35.14	43.01

complicated. So, the algorithmic complexity including test set encoding time, test application time, the decoder architecture and area overhead is roughly evaluated in this paper. Table 8 compares the test set encoding time include don't care bit filling time and Hamming Distance 2-D reordering time. The experimental results show that HDDR+PEDCBC ASFDR by MT-filling scheme consumed less test set encoding time than the other previous works did.

5.4 Test Application Time and Decoder Area Overhead

In proposed scheme, f_{ate} and f_{scan} respectively denotes ATE frequency and on-chip scan frequency, the frequency ratios is defined as $\alpha=f_{scan}/f_{ate}$, the slow speed tester tests the high speed system, so $f_{ate} < f_{scan}$. The decoder includes three stages: The decoder receives the encoded test data from ATE at a frequency of f_{ate}, HDDR+PEDCBC EFDR/ASFDR codes are decoded at a frequency of f_{scan}, the bits swapping in test pattern is performed to further obtain the power efficient test set.

It is assumed that ATE adopts only one channel for sending codeword to CUT and takes only one ATE clock cycle for sending one bit. The clock in bit swapping logic array is synchronized with the chip operating clock during scan testing. Let test application time $t(m,n)$ be the total time required to decode a codeword that is the n^{th} member of the m^{th} group. Let $t_{shift}(m,n)$ be the time required to transfer the encoded test data from ATE to on-chip and $t_{decode}(m,n)$ be the time required to decode the codeword. Let $t_{swap}(m,n)$ be the time required to swap the corresponding bits in test pattern. So the test application time (TAT) reflected by ATE cock cycles [6] is concluded by formula (5).

$$t(m,n) = t_{shift}(m,n) + t_{decode}(m,n) + t_{swap}(m,n) \quad (5)$$

The decoder is synthesized using FPGA optimized for area overhead, and it is assumed that there is a maximum run length of 2000. Then the estimated gates count for the decoder are calculated, Table 9 compares four techniques in terms of

Table 8 Test set encoded time (s)

Circuit	EFDR [7]	HDDR+ PEDCBC EFDR with MT-filling	Reduction %	ASFDR [8]	HDDR+ PEDCBC ASFDR with MT-filling	Reduction %
S5378	2.938	2.829	3.71 %	3.112	2.891	2.28 %
S9234	5.000	4.422	11.56 %	3.368	3.657	−8.58 %
S13207	13.438	13.704	−1.98 %	14.063	13.563	3.56 %
S15850	7.485	7.047	5.85 %	8.206	7.203	12.22 %
S38417	21.454	18.001	16.09 %	23.65	18.392	22.23 %
S38584	25.923	24.299	6.26 %	29.313	25.548	12.84 %
Avg.	–	–	6.92 %	–	–	7.43 %

Table 9 Test application time and decoder area overhead

Circuit	FDR [5]			EFDR [7]			HDDR+PEDCBC EFDR with MT-filling			HDDR+PEDCBC ASFDR with MT-filling		
	TAT		Area cost	TAT		Area cost	TAT		Area cost	TAT		Area cost
	α=4	α=8		α=4	α=8		α=4	α=8		α=4	α=8	
s5378	16,803	14,039	1380	13,172	11,652	1475	13,093	10,946	2158	11,934	10,369	2736
s9234	29,206	24,086		21,424	20,318		20,927	19,853		19,186	17,791	
s13207	70,361	48,358		52,711	36,946		51,382	33,685		50,163	33,287	
s15850	42,270	32,362		32,517	27,172		32,185	26,726		31,358	24,135	
s38417	123,700	110,521		75,614	65,509		78,351	70,837		80,213	69,432	
s38584	118,628	93,260		86,320	74,955		82,916	73,059		78,692	64,186	

the number of clock cycles needed to decode the test set, which corresponds to the test application time under various frequency ratios. Furthermore decoder area overhead is shown.

For all test sets involved in experiments verification, the number of clock cycles needed for HDDR+PEDCBC EFDR/ASFDR with MT-filling is less than that needed for FDR and EFDR. It indicates that the proposed scheme consumed less test application time than the previous works did. In addition, the estimated gates count for HDDR+PEDCBC EFDR/ASFDR with MT-filling are slightly higher than that for FDR and EFDR, and the decoder area overhead is considered small in comparison with the actual circuit size.

6 Conclusion

A power efficient BIST TPG method is proposed to reduce scan-in test power dissipation. Before the scan testing, the test set is preprocessed by don't care bit based 2-D adjusting and Hamming Distance based 2-D reordering in interspersed way. Firstly, the test set is adjusted according to the number of don't cares bits in each test pattern, don't care bit based first adjusting is applied to the test set. Secondly, Hamming Distance based first row-wise reordering is applied to the adjusted list. Thirdly, the first matrix transpose is achieved. Fourthly, don't care bit based second adjusting is applied to the each row in transposed matrix. Fifthly, Hamming Distance based second column-wise reordering is applied to the new list in transposed matrix. Finally, the second matrix transpose is achieved until the power efficient test set is obtained. The six largest ISCAS'89 benchmark circuits verify the power efficient BIST TPG method. The experimental results show that it devotes to decreasing test power dissipation during scan testing, which ensuring high compression ratio, consuming less test application time and occupying small decoder area overhead.

Acknowledgements This research work was supported by the National Natural Science Foundation of China (61001049, 61372149 and 61370189). Scholarship sponsored by China Scholarship Council [2013] 3018.

References

1. Ahmed N, Tehranipour MH, Nourani M (2004) Low power pattern generation for BIST archite cture. Proceedings of the 2004 International Symposium on Circuits and Systems, ISCAS '04, vol. 2, pp 689–692
2. Basker P, Arulmurugan A (2012) Survey of low power testing of VLSI circuits. Int Conf Comput Commun Inform (ICCCI) 1(7):10
3. Chandra A, Chakrabarty K (2000) Test data compression for system-on-a-chip using Golomb codes. VLSI Test Symposium, 2000. Proceedings 18th IEEE, vol. 113, no. 120
4. Chandra A, Chakrabarty K (2002) Low-power scan testing and test data compression for system-on-a-chip. IEEE Trans Comput Aided Des Integr Circ Syst 21(5):597–604
5. Chandra A, Chakrabarty K (2003) Test data compression and test resource partitioning for system-on-a-chip using frequency-directed run-length (FDR) codes. IEEE Trans Comput 52(8):1076,1088
6. ChandraA, Chakrabarty K (2002) Reduction of SOC test data volume, scan power and testing time using alternating run-length codes. Design Automation Conference, 2002. Proceedings 39th, pp 673–678
7. El-Maleh AH (2008) Test data compression for system-on-a-chip using extended frequency-directed run-length code. IET Comput Digit Tech 2(3):155–163
8. Hellebrand S, Würtenberger A (2002) Alternating run-length coding–A technique for improved test data compression. In: Handouts 3rd IEEE International Workshop on Test Resource Partitioning, Baltimore
9. Jas A, Ghosh-Dastidar J, Mom-Eng N, Touba NA (2003) An efficient test vector compression scheme using selective Huffman coding. IEEE Trans Comput Aided Des Integr Circ Syst 22(6):797–806

10. Mehla US, Dasgupta KS, Devashrayee NM (2010) Hamming distance based reordering and column wise bit stuffing with difference vector: a better scheme for test data compression with run length based codes. 23rd International Conference on VLSI Design. VLSID '10, vol. 33, no. 38, p 3
11. Mehta US, Devashrayee NM, Dasgupta KS (2010) Hamming distance based 2-D reordering with power efficient don't care bit filling: optimizing the test data compression method. Int Symp Syst Chip (SoC) 1(7):29–30
12. Nourani M, Tehranipoor M, Ahmed N (2008) Low-transition test pattern generation for BIST-based applications. IEEE Trans Comput 57(3):303–315
13. Sankaralingam K, Oruganti RR, Touba NA (2000) Static compaction techniques to control scan vector power dissipation. In: 18th IEEE VLSI Test Symposium, vol. 35, no. 40
14. Seongmoon W, Gupta SK (2002) DS-LFSR: a BIST TPG for low switching activity. IEEE Trans Comput Aided Des Integr Circ Syst 21(7):842–851
15. Sivanantham S, Mallick PS, Raja Paul Perinbam J (2014) Low-power selective pattern compression for scan-based test applications. Comput Electr Eng 40(4):1053–1063
16. Yuan H, Mei J, Song H, Guo K (2014) Test data compression for system-on-a-chip using count compatible pattern run-length coding. J Electron Test Theory Appl 30(2):237–242

Haiying Yuan received her PhD, M.S. and B.S. in University of Electronic Science and Technology of China respectively. She works in Beijing University of Technology. Her research interests include VLSI and System-on-Chip design, testing, verification, design for testability and fault diagnosis, signal detection and information processing.

Kun Guo is pursuing his M.S. degree in Beijing University of Technology. His research interests include integrated circuit design, testing, design for testability and fault diagnosis.

Xun Sun received his B.S. and. M.S. degrees from University of Electronic Science and Technology of China. He is pursuing his PH.D degree in Tsinghua University. His research interests include satellite communications and navigation, information anti-jamming.

Jiaping Mei received his M.S. degree in Beijing University of Technology. His research interests include integrated circuit design, testing, design for testability and fault diagnosis.

Hongying Song is pursuing her M.S. degree in Beijing University of Technology. Her research interests include signal detection and information processing.