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A New Analytical Model of SET Latching Probability for Circuits Experiencing Single- or Multiple-Cycle Single-Event Transients

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Abstract As technology scales down, more single-event transients (SETs) are expected to occur in combinational circuits and thus contribute to the increase of soft error rate (SER). We propose a systematic analysis method to precisely model the SET latching probability. Due to the decreased critical charge and shortened pipeline stage, the SET duration time is likely to exceed one clock cycle. In previous work, the SET latching probability is modeled as a function of SET pulse width, setup and hold times, and clock period for single-cycle SETs. Our analytical model does not only include new dependent parameters such as SET injection location and starting time, but also precisely categorizes the SET latching probabilities for different parameter ranges. The probability of latching multiple-cycle SETs is specifically analyzed in this work to address the increasing ratio of SET pulse width over clock period. We further propose a method that exploits the boundaries of those dependent parameters to accelerate the SER estimation. Simulation results show that the proposed analysis method achieves up to 97% average accuracy, which is applicable for both single- and multiple-cycle SETs. Our case studies on ISCAS'85 benchmark circuits confirm our analysis on the impact of SET injection location and starting time on the SET latching probability. By exploiting our analytical model, we achieve up to 78% simulation time reduction on the process of SET latching probability and SER estimation, compared with Monte-Carlo simulation.

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1 Introduction

High-energy particle strike on integrated circuits (ICs) results in soft errors [2]. While single-event upsets (SEUs) have been extensively studied primarily for memory elements, single-event transients (SETs) gain increasing attention. This is because more SETs are latched in high-frequency systems and cause more system failures [11, 12, 21]. Measurement results of test chips exposed to heavy ions or alpha particles indicate that the SET pulse varies from 25ps [10] to over 1ns [17]. The SET pulse width depends on the technology node that the test chips use. When a system operates in Giga Hertz regime (e.g. PC7448 for space-qualified equipment [7]), the duration of a SET pulse varies from a portion of one clock cycle to multiple clock cycles. Recently, it has been reported that SET rates increase with system clock frequencies [3, 4, 20]. The increased ratio of SET pulse duration over clock period challenges the analysis of SET-induced soft errors, as multiple soft errors may be introduced by a single SET and thus the superimposition of multiple SETs may cause a complicate error case.

The probability of SET-induced soft error is the combination of (1) the probability that a particle strike on an IC substrate generates a SET pulse that is strong enough to exceed the noise margin, (2) the probability of a SET is propagated through the logic network and not eliminated by logical masking effects, and (3) the probability that a SET reaches the setup and hold time window of a storage element at the end of the combinational logic circuit [15]. The three probabilities above are often referred as the probabilities of electrical masking, logical masking and latch window

masking, respectively. Electrical masking effects have been investigated in [8]. Two exponential functions are used to model a SET current pulse [23]. Recently, the impact of a SET injection is modelled as a voltage source [19]. Logical masking effects have been widely studied in [5]. Electrical, logical and latch window masking effects are considered simultaneously in [9, 16].

As clock period and critical charge decrease, a SET pulse may cover multiple clock cycles. Analysis methods for electrical and logical masking can be reused, as these two masking effects are independent with the duration of a SET pulse. Latch window masking, unfortunately, is sensitive to the SET pulse width. As a result, the models of SET latching probability obtained from previous single-cycle analysis are not suitable now. Moreover, deep pipelining design shrinks the critical path, resulting in the setup and hold time for each pipeline stage being comparable to the clock period. Consequently, the probability of a SET being latched is expected to increase. The simplified models in previous work [5, 14, 16, 22] for the latch window masking probability need to be revised to improve the SER estimation accuracy. In this work, we re-study the SET latching probability to address the emerging challenges. In addition, we also propose a fast simulation method for SET assessment to consider new SET latching scenarios induced by the increased clock frequency and shortened pipeline stage.

The remainder of this work is organized as follows. We summarize the related work and highlight our main contributions in Section 2. Section 3 describes the proposed analytical model for SET latch masking probability for the single- and multiple-cycle SET injection scenarios. We exploit our analytical model for SET latching probability and propose a fast assessment method to examine the impact of SET injection in Section 4. In Section 5, the impact of SET injection location, SET injection timing, system clock period, and SET pulse width on the SET latching probability are evaluated. Conclusions and future work are provided in Section 6.

2 Related Work

2.1 Previous Work

The SET latching probability is recognized as a function of SET pulse width (δ), clock period (T_{CLK}), setup time (T_S) and hold time (T_H). The probability of a SET being latched by the storage cell, $P_{ILW,}$ is expressed in Eq. (1) [13].

$$P_{ILW} = \begin{cases} 0, & \delta < (T_S + T_H) \\ \dfrac{\delta - (T_S + T_H)}{T_{CLK}}, & \delta \geq (T_S + T_H) \end{cases} \quad (1)$$

Although P_{ILW} is categorized for two ranges of SET pulse widths, the model in (1) is loosely constrained. Only the cases of no-SET latched and full-SET latched are considered in (1). The case that a SET partially covers the latch window is ignored in (1). In reality, the SET latching probability contributed by partially latched SETs is not trivial. Moreover, the impact of SET injection location and SET starting timing are not reflected in (1). As expressed in (1), the P_{ILW} has a linear relation with the SET pulse width and there is not upper bound for δ. If δ is larger than the clock period, the P_{ILW} in (1) exceeds 1, which is not realistic for a definition of probability. An upper bound for P_{ILW} is necessary for multiple-cycle SETs.

Alexandrescu et al. [1] improved the probability of latch window masking by assuming that the partially latched SET pulse yields a soft error with a probability of 0.5. Their SET latching probability is modeled in (2), in which the first non-zero probability is the consequence of partially latched SETs.

$$P_{ILW} = \begin{cases} \dfrac{1}{2} \cdot \dfrac{T_H + T_S + \delta}{T_{CLK}}, & (\delta < T_S + T_H) \\ \dfrac{\delta}{T_{CLK}}, & (\delta \geq T_S + T_H) \end{cases} \quad (2)$$

In this model, three latching cases are considered: (i) if a SET pulse covers the entire latch window, that SET will be latched for sure (referred to *sure error*), (ii) if a SET pulse partially covers the latch window, that SET has a 50% chance to be latched (referred to *uncertain error*), and (iii) if a SET pulse does not enter the latch window at all, that SET does not create a soft error (referred to *silent error*). As this model zooms in different situations happened in the latching window, the accuracy of the SET latching probability is improved. However, similar to (1), the effects of SET injection timing and multiple-cycle SETs are not considered in (2).

The recent probabilistic symbolic model [16] suggests to considering the impact of SET re-convergence on the SET latching probability for accurate SER estimation. In that model, the situations that the duration of SET pulse is less than the width of latching window and larger than the clock period are not considered.

In our previous work [18], we additionally consider the starting moment of the SET pulse with respect to the clock edge and the logic delay of the cell contaminated by a SET injection. A set of closed-form expressions for the latching probability are provided in [18] for a wide range of SET pulse widths, different logic gate delays, clock period, setup and hold time. The preliminary results in [18] indicate that the parameter boundaries in our closed-form expression have a potential to be used in fast and efficient SER evaluation. The limitations of our previous work are: the SET pulse width in our analysis is no more than one clock cycle. In this work, we will address our limitations and demonstrate the importance of

the new dependent parameters for the single- and multiple-cycle SET latching probabilities.

2.2 Our Main Contributions

The main contributions of this work are summarized as follows:

- The proposed method studies the new dependency factors of SET latching probability, such as when a SET is injected to circuits and the logic delay of the gate receives a SET. These new parameters can be used to improve the accuracy of exiting SER estimation models, which are a function of clock period, setup and hold time, and SET pulse width. We derived the explicit boundaries for the SET pulse width and the gate delay that are required on the situation of silent errors, uncertain errors and sure errors.
- In the proposed analytical model for the SET latching probability, we differentiate the condition of single-cycle SET injection from that of multiple-cycle SET injection. Previous models cannot be used in the scenario of multiple-cycle SET injection. As the Giga Hertz microprocessor is likely to be integrated in space-qualified equipment [7], it is imperative to study the soft error increase caused by multiple-cycle SETs. We zoomed in the condition of uncertain errors and studied the combination of different error types induced by single SET injection. Our analysis and simulation results confirm that the SET latching probability becomes saturated after a threshold. Our derivation explicitly describes the dependency factors for the threshold point.
- We propose a SET injection method that exploits the boundaries of dependent parameters for the SET latching probability to efficiently estimate SER. As our method is capable of estimating SER through limited SET injection locations and SET pulse width, our entire SER evaluation process is time-efficient. This method facilitates the SER evaluation on the gate level within a moderate amount of simulation time. Compared with existing approaches, our method does not require additional logic gate format change for symbolic analysis and only chooses very limited SET injection locations.

3 Proposed Latching Window Masking Probability

The terminologies and symbols used in the following analysis are depicted in Fig. 1. τ_0 is the starting point of the injected SET pulse with respect to the closest clock rising edge. τ_{gate} is the logic gate delay from the beginning of a critical path to the gate receiving a SET pulse. In Fig. 1, The SET pulse in the middle is the effective SET injection pulse in the digital world. For the realistic SET pulse shape, please refer to [6, 24]. The SET pulse on the bottom of Fig. 1 represents a SET location after that SET propagating through a combinational logic but before reaching the storage element's input.

Assume a SET pulse is injected into a logic chain followed by a D-flip-flop (D-FF), as shown in Fig. 2. An input signal for the circuit in Fig. 2 takes τ_{gate1}, τ_{gate2}, τ_{gate3} and τ_{gate4} to reach the output of Gate 1, Gate2 and Gate3 and Gate4, respectively. If a SET pulse is injected in one of the gates, the logic value of the original signal is pulled down, as shown in the dotted-line in Fig. 2. When no logical or electrical masking happens on the affected signal, the logic dent may enter the D-FF latch window and cause a soft error. As indicated in Fig. 2, the starting point of the SET pulse and the pulse width are critical in determining whether the SET pulse will be latched or not. SETs injected on gates farther from the D-FF are more sensitive to smaller τ_0, as the sum of a small τ_0 and propagation delay is close to the path length to reach the latch window. For the gates near the memory cell, a SET injection with a larger τ_0 is desired in order to ensure that SET to be latched.

3.1 Latching Single-Cycle SETs

In our previous work [18], we provided the closed-form expressions for the SET latching probability, as well as the explicit boundaries for each dependent parameter. For readers' convenience, we copied them in Eq. (3). As indicated in Eq. (3), the SET latching probability is a function of the SET pulse width, setup and hold time, clock period, and gate delay. When $T_H<\tau_{gate}<T_{CLK}-T_S-\delta$ and $0<\delta<T_S+T_H$ or $T_S+T_H<\delta<T_{CLK}-T_S-T_H$, the SET latching probability only depends on SET pulse width and clock period. The sub-Eq. 3b

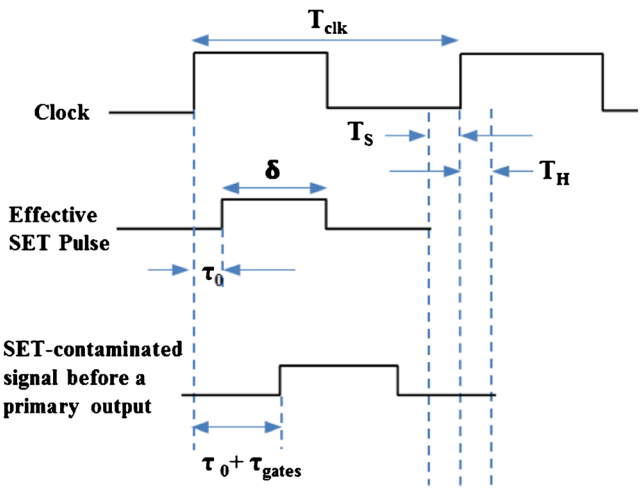


Fig. 1 Parameters used in the analysis of SET injection in this work

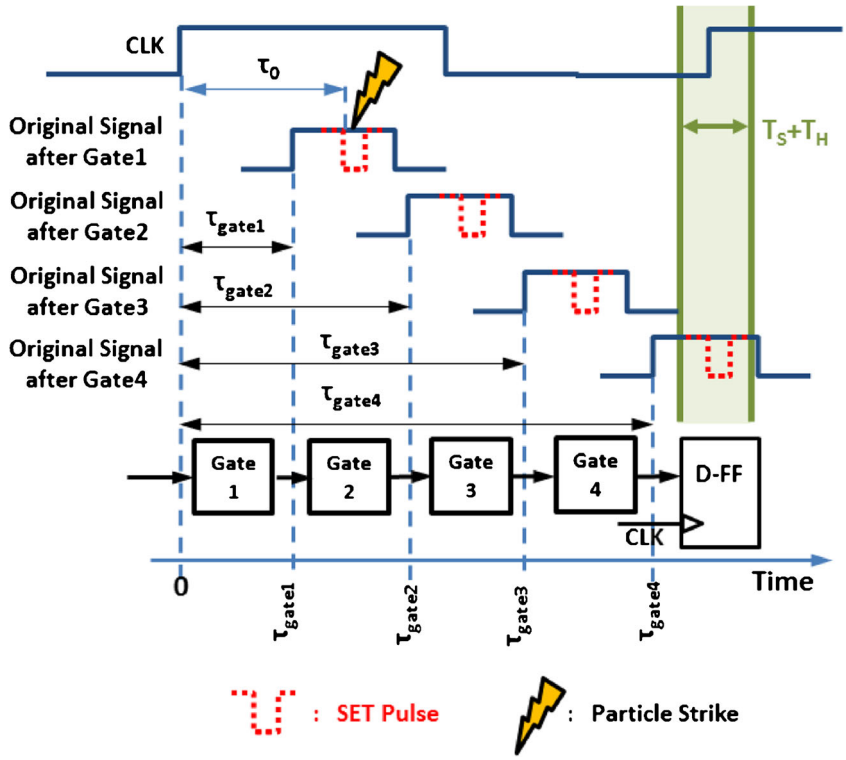


Fig. 2 SET injection on a combinational logic followed by a D flip-flop

and e are consistent with previous models expressed in Eqs. (1) and (2).

For $0<\delta<T_S+T_H$:

$$P_{ILW} = \begin{cases} \dfrac{\frac{1}{2}(\delta + T_H + \tau_{gate})}{T_{CLK}}, & (0 < \tau_{gate} < T_H) \\ \dfrac{\delta}{T_{CLK}}, & (T_H < \tau_{gate} < T_{CLK}-T_S-\delta) \\ \dfrac{T_{CLK}-T_S-\tau_{gate}}{T_{CLK}}, & (T_{CLK}-T_S-\delta < \tau_{gate} < T_{CLK}-T_S) \end{cases} \quad (3a-c)$$

For $T_S+T_H<\delta<T_{CLK}-T_S-T_H$:

$$P_{ILW} = \begin{cases} \dfrac{\delta+\frac{1}{2}(T_H-\tau)}{T_{CLK}}, & (0 < \tau_{gate} < T_H) \\ \dfrac{\delta}{T_{CLK}}, & (T_H < \tau_{gate} < T_{CLK}-T_S-\delta) \\ \dfrac{\frac{1}{2}(\delta + T_{CLK}-T_S-\tau_{gate})}{T_{CLK}}, & (T_{CLK}-T_S-\delta < \tau_{gate} < T_{CLK}-T_S) \end{cases} \quad (3d-f)$$

For $T_{CLK}-T_S-T_H<\delta<T_{CLK}$:

$$P_{ILW} = \begin{cases} \dfrac{\frac{1}{2}(\delta + T_{CLK}-T_S-T_H)}{T_{CLK}}, & (0 < \tau_{gate} < T_H) \\ \dfrac{\frac{1}{2}(\delta + T_{CLK}-T_H-2T_S-\tau_{gate})}{T_{CLK}}, & (T_H < \tau_{gate} < T_{CLK}-T_S) \end{cases} \quad (3g-h)$$

3.2 Latching Multiple-Cycle SETs

In this work, we extend our analysis to the latching probability of multiple-cycle SETs. In the case of single-cycle SETs, we categorize the soft errors induced by SETs into three types: uncertain errors, sure errors, and silent errors [1]. If the SET pulse does not cover the entire setup and hold time period, the probability of latching SET is 50%. We refer it as the *uncertain error* condition (i.e. 50% error). If the SET pulse covers the entire setup and hold time periods, that SET pulse will be latched for sure. We name the 100% SET latching as *sure error* (i.e. 100% error). Silent error means that the injected SET pulse is not latched by the D-FF (i.e. 0% error). We name the silent error as 0% error. For a multiple-cycle SET, we extend the error type to six categories: 50–50%, 50–100%, 100–50%, 100–100%, 0–100%, and 100–0%, in which the first and second numbers represent the probabilities of latching the SET in the following two cycles.

We use a 50–100% SET latching as an example to introduce our analysis method for the estimation of SET latching probability. According to the definition of a 50–100% SET error, the beginning of the SET pulse is partially in the first latch window and the rest of SET pulse remains through the next clock cycle (i.e. covering the entire second latching window). Fig. 3 shows the 50–100% error caused by a multiple-cycle SET. The boundaries for each parameter are expressed in Eqs. (4)

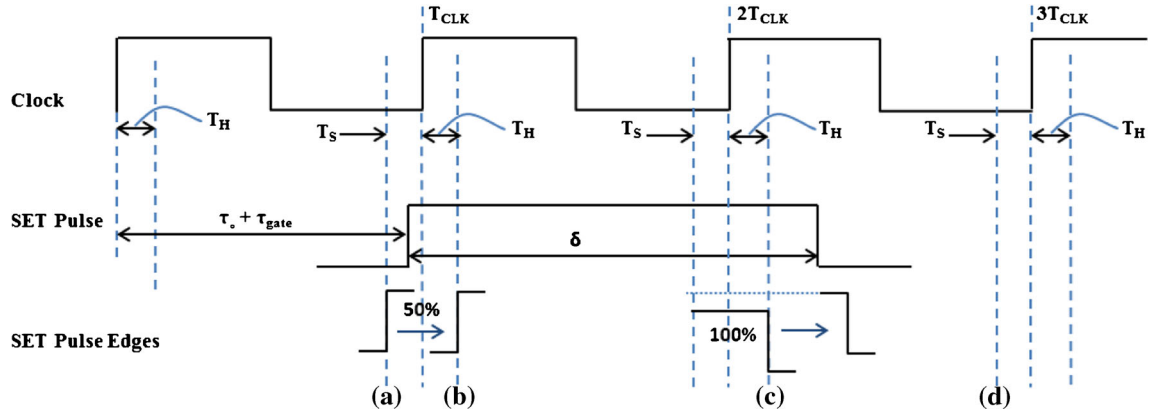


Fig. 3 The multi-cycle SET enters in to two latch windows, partially covering the first latch window (50% chances of error latching) and completely covering the second latch window (100% error latching)

and (5), which describe the boundaries for the SET starting and ending edges shown in Fig. 3.

$$T_{CLK}-T_S < \tau_0 + \tau_{gate} < T_{CLK} + T_H \tag{4}$$

$$2T_{CLK} + T_H < \tau_0 + \tau_{gate} + \delta < 3T_{CLK}-T_S \tag{5}$$

We re-arrange Eqs. (4) and (5) by moving τ_{gate} to the two sides of the inequality and obtain the boundary of SET injection time τ_0, as expressed in Eqs. (6) and (7), respectively. We label the four boundary conditions, (a), (b), (c) and (d). By comparing (a)-(d), we conclude the boundaries for τ_{gate} and δ that ensure the SET pulse result in the 50%-100% SET latching condition.

$$(a) : T_{CLK}-T_S-\tau_{gate} < \tau_0 < (b) : T_{CLK} + T_H-\tau_{gate} \tag{6}$$

$$(c) : 2T_{CLK} + T_H-\tau_{gate}-\delta < \tau_0 < (d) : 3T_{CLK}-T_S-\tau_{gate}-\delta \tag{7}$$

All possible overlap τ_0 ranges in Eqs. (6) and (7) need to be examined. For instance, to satisfy Case 1 in Fig. 4, we perform the comparison expressed in Eq. (8). To compute the number of cases shown in the shadow area, we need further ensure the conditions of (b) and (c) all being greater than zero. Consequently, we obtain the boundary for τ_{gate}, as expressed in Eq. (9).

$$\left.\begin{array}{ll}(c) > (a): & T_{CLK} + T_H + T_S > \delta \\ (b) > (c): & \delta > T_{CLK} \\ (d) > (b): & 2T_{CLK}-T_H-T_S > \delta \\ (d) > (a): & 2 T_{CLK} > \delta \end{array}\right\} \rightarrow T_{CLK} < \delta < T_{CLK} + T_H + T_S \tag{8}$$

$$\left.\begin{array}{l}(b) > 0 : T_{CLK} + T_H > \tau_{gate} \\ (c) > 0 : 2T_{CLK} + T_H-\delta > \tau_{gate}\end{array}\right\} \rightarrow \tau_{gate} < T_{CLK}-T_S \tag{9}$$

Based on the defined conditions for δ and τ_0 in Eqs. (8) and (9), we can obtain the number of cases that result in such latching condition in Eq. (10), in which Δt_s is the step size between two consecutive τ_0 s in simulations. Finally, we obtain the probability of 50–100% SET latching, as expressed in Eq. (11).

$$N_{50\%-100\%} = \frac{(b)-(c)}{\Delta t_s} = \frac{\delta-T_{CLK}}{\Delta t_s} \tag{10}$$

$$P_{50\%-100\%} = \frac{\frac{\delta-T_{CLK}}{\Delta t_s}}{\frac{T_{CLK}}{\Delta t_s}} = \frac{\delta-T_{CLK}}{T_{CLK}} \tag{11}$$

The rest of SET latching window masking probabilities (12)–(17) for other error scenarios are summarized in Table 1.

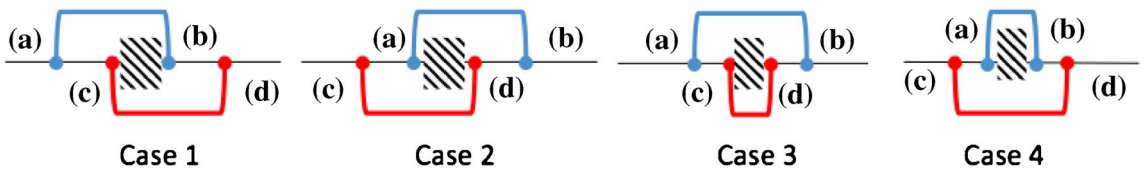


Fig. 4 Four boundary-comparison scenarios for determining the number of SET latched cases. (a)–(d) are four boundary conditions in Eqs. (6) and (7). The shadow area represents the overlapped range defined by (a)–(d)

Table 1 Latching probabilities for the multiple-cycle SETs leading to different soft error categories

Latching condition	Corresponding δ and τ_{gate} boundaries for each latching case	Error latching probability
50%–50%	$T_{CLK} < \delta < T_{CLK} + T_H + T_S \;\; \tau_{gate} < T_{CLK} - T_s$	$\frac{T_{CLK}+T_H+T_S-\delta}{T_{CLK}}$ (12)
50%–100%	$T_{CLK} < \delta < T_{CLK} + T_H + T_S \;\; \tau_{gate} < T_{CLK} - T_s$	$\frac{\delta - T_{CLK}}{T_{CLK}}$ (13a)
	$T_{CLK} + T_H + T_S < \delta < 2T_{CLK} - T_H - T_S \;\; \tau_{gate} < T_{CLK} - T_s$	$\frac{T_H+T_S}{T_{CLK}}$ (13b)
	$2T_{CLK} - T_H - T_S < \delta < 2T_{CLK} \;\; \tau_{gate} < T_{CLK} - T_s$	$\frac{2T_{CLK}-\delta}{T_{CLK}}$ (13c)
100%–50%	$T_{CLK} < \delta \; < T_{CLK} + T_H + T_S \;\; \tau_{gate} < 2T_{CLK} - T_s - \delta$	$\frac{\delta - T_{CLK}}{T_{CLK}}$ (14a)
	$T_{CLK} + T_H + T_S < \delta < 2T_{CLK} - T_H - T_S \;\; \tau_{gate} < 2T_{CLK} - T_s - \delta$	$\frac{T_H+T_S}{T_{CLK}}$ (14b)
	$2T_{CLK} - T_H - T_S < \delta < 2T_{CLK} \;\; \tau_{gate} < T_H$	$\frac{2T_{CLK}-\delta}{T_{CLK}}$ (14c)
100%–100%	$T_{CLK} + T_H + T_S < \delta < 2T_{CLK} \;\; \tau_{gate} < 2T_{CLK} + T_H - \delta$	$\frac{\delta - T_{CLK} - T_H - T_S}{T_{CLK}}$ (15)
0%–100%	$T_{CLK} < \delta < 2T_{CLK} - T_H - T_S \;\; \tau_{gate} < T_{CLK} - T_S$	$\frac{2T_{CLK} - T_H - T_S - \delta}{T_{CLK}}$ (16)
100%–0%	$T_{CLK} < \delta < 2T_{CLK} - T_H - T_S \;\; \tau_{gate} < T_H$	$\frac{2T_{CLK} - T_H - T_S - \delta}{T_{CLK}}$ (17)

SET latching probabilities provided in Table 1 are differentiated from a specific range for δ and τ_{gate}. The main difference between our analytical model and the existing model is that we have considered factors such as τ_{gate} and τ_0 . By including new dependent factors in the model, we obtain more precise SET latching probabilities. Another difference is that the parameter boundaries in Table 1 are more refined than other models [1, 13]. Our new model facilitates fast SET effect assessment as we can exploit the parameter boundaries to avoid a large amount of random simulations that yield the same SET latching probability or SER.

4 Fast SET Injection Approach for SET Assessment

In Monte-Carlo random simulation approaches, all possible situations that result in an error need to be considered. These cases depend on input patterns, SET pulse widths, logical gates used in the circuit, and SET injection time and location. However, it is time consuming to cover all the possible cases in random simulation. To speed up the assessment procedure by decreasing the number of test cases, we propose to use our analytical boundaries for δ and τ_{gate} to assist semi-random simulation. These boundaries define a set of situations that reflect the same SET latching probability. Therefore, the number of test cases depends on the number of boundaries defined for each error latching probability derivation (certainly, one can also slightly increase the test cases). For each set of logic gate delay boundaries, the SET pulse width remains same. Since the SET latching probability depends on the moment when SET reaches the latch window, the logic gate delay and the SET injection time play a significant role to determine whether the SET will be latched. Each circuit can be divided into several blocks, which contain a group of gates with the same logic delay. In this case we can group the gates based on their distance to the memory cell. Categorizing the logic gates facilitates us to choose limited test cases to perform fast SER estimation.

The proposed SER estimation model is presented in Eq. (18).

$$SER = \frac{\sum_{i=1}^{n}\left[(P_{LG} * P_{ILW})_i * \left(\frac{N_{gi}}{\sum_{k=1}^{n} N_{gk}}\right)\right]}{n} \tag{18}$$

In which, P_{LG} is the probability of no logical masking, P_{ILW} is the probability of no latch window masking, N_{gi} is the number of logic gates in the i^{th} logic category, and $\sum_{k=1}^{n} N_{gk}$ represents the total number of logic gates. P_{LG} is achieved from random simulations by keeping the SET pulse width constant. P_{ILW} is obtained from Eq. (3) and (12)–(17). In this work, the electrical masking has not been considered due to the gate level analysis. According to our model we have separated the entire circuit in to different blocks and each block contains gates that are in a specific range of logic delays. We also need to choose limited gates from each selection to be able to decrease the simulation time significantly. Thus, the number of selected gates in each block should be divided over the number of total logic categories to represent an average value.

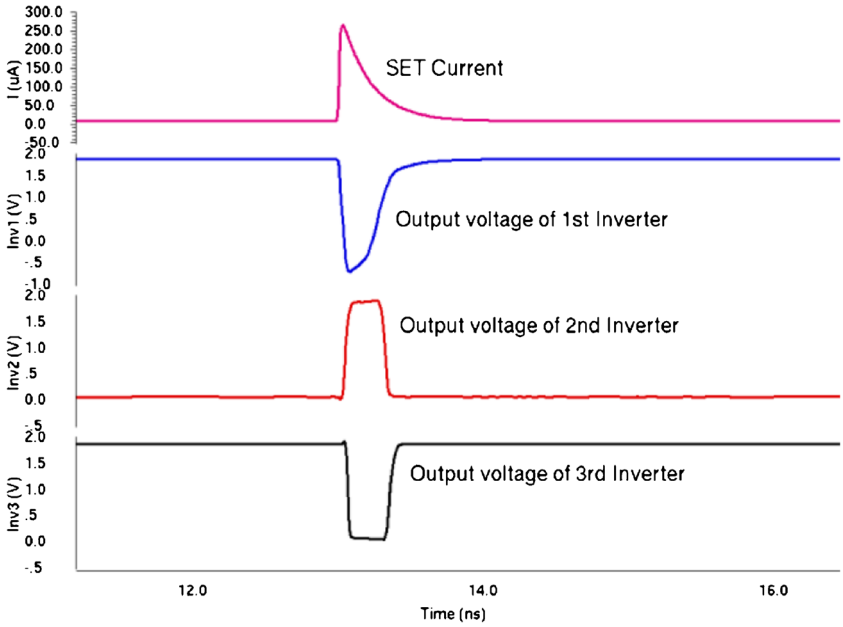


Fig. 5 Gate-level SET model adopted in this work

5 Experimental Results

5.1 Experiment Setup

The SET injection is typically modeled with a current source expressed in Eq. (19) [24]

$$I(t) = \frac{Q_{coll}}{t_f - t_r}\left(exp\left(-\frac{t}{t_f}\right) - exp\left(-\frac{t}{t_r}\right)\right) \quad (19)$$

in which, t_f is the falling time, t_r is the rising time, and Q_{coll} is the total collection charges that are deposited by a particle strike. For instance, a SET pulse is injected to the drain terminal of Gate1 in Fig. 2. We implemented an inverter chain with an IBM CMOS7RF 180nm technology. Q_{coll} is set to 30fC. Because of charging the output capacitor, the SET current pulse is converted to a non-ideal square voltage pulse, as shown in Fig. 5. Certainly, the SET pulse can be modeled with other shapes [6]. As the pulse is propagated through the logic network, the SET-induced voltage pulse gradually becomes a square pulse due to the inherent filtering capability of digital circuits. Considering this characteristic, we assume the SET pulse injected to the circuit under test is a square pulse in our gate level simulation.

In the following experiment, a chain of exclusive-OR (XOR) gates and three modified ISCAS'85 benchmark circuits were synthesized in Synopsys Design Compiler. Three ISCAS'85 benchmark circuits, c432, c1355, and c6288, are modified by adding D-FFs for each primary output, in order to examine the latching probability of SETs injected in the middle of circuits. Post-synthesize simulation were performed in Cadence Verilog-XL tools to collect the D-FF output errors, circuit output errors and masked errors. A TSMC 65nm CMOS technology was used in all of the following simulations.

5.2 Accuracy Evaluation of Proposed Analytical Model

In our previous work [18], we verified the proposed model on an inverter chain that receives single-cycle SETs. Because an inverter does not have logical masking capability, SER of this circuit is equal to the probability of the propagated SET falling in the D-FF latch window. We compared the outputs of the circuit experiencing SETs with that of the golden circuit after every SET injection. Eq. (3) indicates that the probability that SET enters the flip-flop latch window is typically proportional to the SET pulse width δ, despite of different coefficients and constant offsets. Simulation results shown in Fig. 6 confirm our predictions: (i) SER increases with SET pulse width; (ii) SER increasing slope varies with different logic gate delays and SET pulse widths. Figure 6 shows that the proposed model perfectly matches to the simulation results. The accuracy of our proposed model is over 92% and the average accuracy is 95.7%. The high accuracy achieved here is mainly

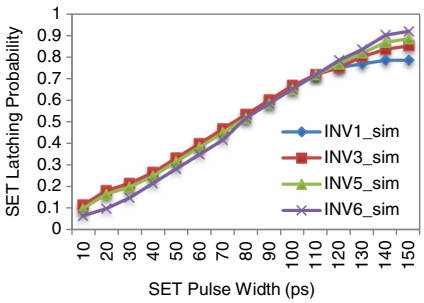


Fig. 6 Simulated soft error rate for the inverter chain

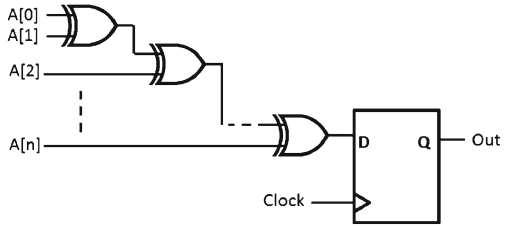


Fig. 7 XOR chain

contributed by the accurate probability related to the latching window masking effect. The proposed analytical model precisely considers various timing-dependent situations of when SETs are latched by memory elements, rather than a single SET latching moment [16]. Although Miskov-Zivanov et al. [16] noticed the impact of latching window effects on SER estimation, their work only considered the situation of $T_S+T_H<\delta$. Since our approach further zooms in different SET-latching timing conditions, our model achieves a better estimation accuracy for the SET latching probabilities and reliable SER prediction.

In this work, we also verified the latching probability model for multiple-cycle SETs. As an XOR gate does not have logical masking capability, we first used an XOR chain (shown in Fig. 7) to assess the latching window masking effect. SET pulses were injected to one XOR gate in Fig. 7 to flip the gate output logic. Because XOR lacks logical masking capability, the consequence of SET injection is propagated to the entry of D-FF. If the propagated SET pulse is in the range of D-FF latching window, that SET pulse is latched, resulting in an error. Note, no matter how many times does the multi-cycle SET be latched, we only count it once if the SET is latched at some point. Therefore, we slowed down the switching frequency of input vectors to examine the latching probability of each multi-cycle SET injection.

We verified the SET latching probabilities in Table 1 by varying SET pulse width and SET injection places. As Eqs. 12, 13, 14, 15, 16 and 17 are the SET latching probability after averaging τ_0, we randomized the SET starting time within a clock cycle in this set of experiments. The number of latched SETs were recorded and sorted for different SET latching cases as categorized in Table 1. We used nine pie charts shown in Figs. 8, 9 and 10 to conclude the trend of SET latching probabilities and identify the dominant SET latching cases. The SET latching probability for 100–100% cases increases with the increase of δ. For instance, as shown in Figs. 8a–c, the SET latching probability increases from zero to 60.53% as the SET pulse width δ increases from one clock-cycle to 1.975 clock-cycles. Similar trends can be found in Figs. 9 and 10. This trend matches to the linear proportional relationship between δ and the latching probability as indicated in Eq. (15). Those results also match to our physical understanding that a SET pulse with a higher δ can inherently cover a larger range of the latch window. As a result, the probability for 100–0% cases decreases due to the increase of δ. This negative trend matches to the negative proportional relationship between and latching probabilities indicated in Eqs. (16) and (17). Comparing three figures in Figs. 8–10, we can see that the 0-100% and 100–100% SET latching cases are alternatively dominant in the overall latching probability. We placed the 50–100% and 100–50% categories together in our simulation results as the SET latching probabilities for these two categories are similar. In the 65nm TSMC library (the technology used in our gate-level simulations), T_S and T_H are all equal to19ps. As the clock period T_{CLK} is equal to 1.6ns, the probabilities indicated in Eqs. (13) and (14) are relative smaller than other SET latching probabilities. This is consistent with our simulation results shown in Figs. 8a, 9a and 10a. The 50–50% latching case can be found only when δ is in the smallest values. Both Eq. (12) and Figs. 8–10 confirm that 50–50% SET latching probability are the smallest portion for the overall SET latching probability.

5.3 Impact of Dependency Factors on Latching Window Masking

5.3.1 Impact of SET Injection Timing

The SET injection timing affects the probability of SET pulse entering the latch window. We examined this dependence on the NAND gate network shown in Fig. 11a. The SET pulse width for this set experiment is 120ps. We vary τ_0 from 20ps to 150ps, each step 10ps. As shown in Fig. 11b, the starting point of SET pulse on n1 (the gate farther to D-FF) is earlier

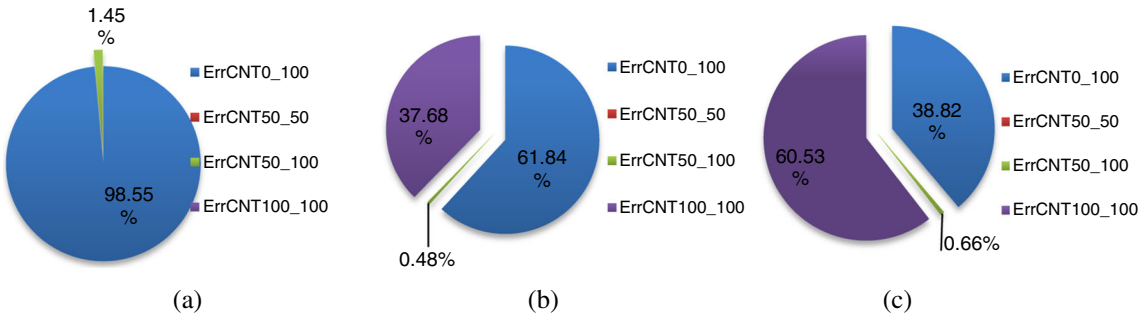


Fig. 8 The first XOR gate receiving SET pulse (**a**) 1 cycle, (**b**) 1.375 cycles, and (**c**) 1.975 cycles

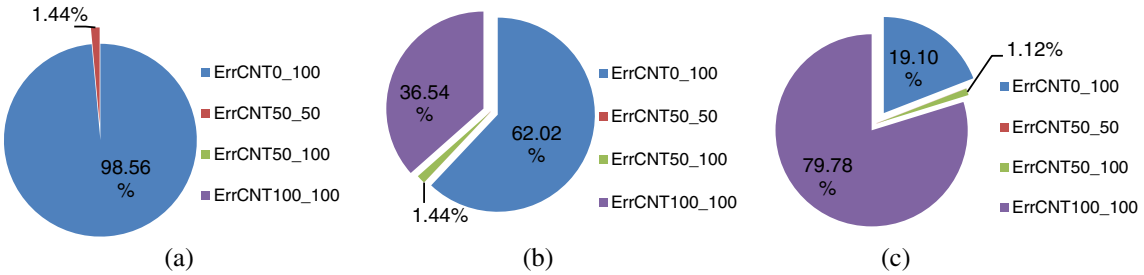


Fig. 9 The fourteenth XOR gate receiving SET pulse (**a**) 1 cycle, (**b**) 1.375 cycles, and (**c**) 1.975 cycles

than that of SET pulse on n8 (the gate nearer to D-FF) to reach a saturated error rate. This means, a later starting point of SET pulse on the farther gate may lead to an underestimated soft error rate. Figure 11b also shows that the saturated error rate obtained at SET injection on farther gates does not reflect the maximum SER. This is because the logical masking effect reduces the soft error rate. To find the maximum SER, one needs to inject SET pulses to the gate closer to registers. When the SET pulse starting point is larger than 100ps (at the IBM 65nm technology node), SER begins to drop because the propagated SET pulse starts to leave the D-FF latching window.

Experimental results on the XOR gate network (i.e., replacing NAND2 with XOR2 in Fig. 11a) are more interesting than those for NAND gate network. As shown in Fig. 12, the SET pulse injected on any gate in the XOR network reaches the same saturated SER, although the starting points for SET pulse are different. In Fig. 12, the SER demonstrates a periodic feature. Take n5 as an example, the SER first increases with the increase of τ_0; after saturation, the soft error rate of n5 grows again at 140ps. The first peak of error rate is caused by the fact that SET is latched in the next cycle. The error rate growth at 140ps is because the SET pulse is latched in the cycle after next clock. As the SET pulse width for Fig. 12 is 60ps, the saturation width of soft error rate is short.

We also used one benchmark circuit, c432, to demonstrate the impact of SET injection timing on the SET latching probability. More precisely, the SET injection timing τ_0 means the starting point of SET pulse with respect to the clock edge that the DFF starts to sample new inputs. A larger τ_0 means the starting time of the injected SET pulse is later in the clock cycle. Figure 13 shows the number of latched SETs for eight million test cases while SET injection timings are varied. In this experiment, the clock period is 1600ps (slightly larger than the critical path delay of c432 in 65nm). Eleven data points for different τ_0s are plotted in Fig. 13. Six gates on one of the critical paths of c432 are selected to inject SET pulses. The subscript of ST_j (j=1…6) on the right side of the gate instance name (e.g. N118) indicates the occurrence order in time. As shown in Fig. 13a, as the gate gets closer to the end of the critical path, the peak value of the latched SETs occurs at a larger τ_0. For example, N429 (ST6) reaches the peak value at 890ps; in contrast, N203 (ST3) reaches the peak value at 670ps. Since δ of 100ps in Fig. 13a is close to the step size of τ_0, only one peak point is observed. When δ reaches 500ps, the peak value of latched SETs remains same for four data points, as shown in Fig. 13b. Moreover, the peak value in Fig. 13b occurs at a smaller τ_0 than that in Fig. 13a. The difference on the number of latched SETs for each gate is originated from logical masking effects. It is clearly shown in Fig. 13 that random starting timing of the SET pulse leads can lead to a large variation on the number of latched SET pulses, thus large variation on soft error rate estimation.

5.3.2 Impact of the Ratio of SET Pulse Width over Clock Period

Our derivation indicates that the SET latching probability has a strong dependency on clock period, SET pulse width, and the SET injection timing with respect to the clock period. We

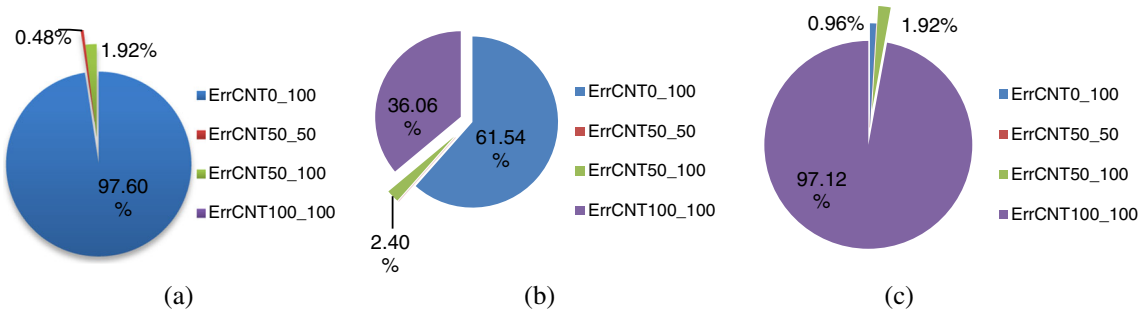
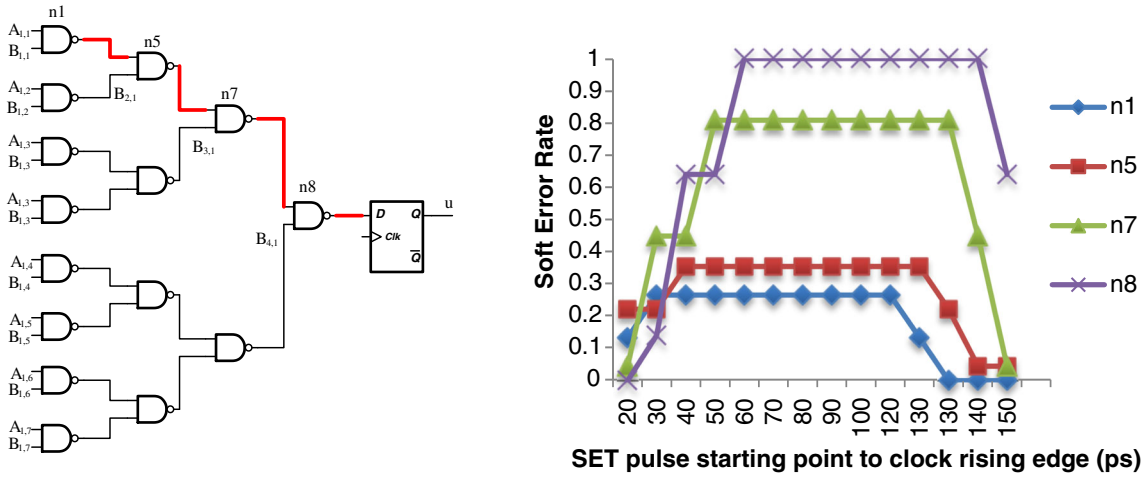


Fig. 10 Pie chart for different SET latching scenarios in an XOR chain with 23 XOR gates that receives one SET pulse with the length of (**a**) 1 cycle, (**b**) 1.375 cycles, and (**c**) 1.975 cycles



(a) (b)

Fig. 11 Impact of SET starting timing on soft error rate. (**a**) A NAND gate network. (**b**) Soft error rate for NAND network

chose two benchmark circuits, c432 and c1355, to validate our derivation. In this experiment, we assumed that the SET pulse width for each gate is same and does not change through propagation. The circuit c432 has a large variety on the applied logic gates; 68 out of 160 gates do not have inherent logical masking capability. In contrast, the circuit c1355 have only 67 out of 546 gates that cannot mask SET-induced errors via the gates themselves. Based on the worst-case delay reported by the Synthesize tool Design Compiler, we selected a slightly higher value than the worst-case delay as the clock period for each benchmark circuit and performed post-synthesize simulation in Cadence NC-Verilog. The clock period used in this experiment is 2.4 ns. Three different SET pulse widths were used to examine the impact of the ratio of SET pulse width over clock period on the number of SETs being latched. Single SET pluses were injected to all possible gates in the benchmark circuit. Each data point in Figs. 14 and 15 was collected after over eight million testing cycles. We randomly chose the SET starting point for each SET pulse injection.

Comparing Fig. 14a–c, we can see that the number of latched SETs varies more significantly for a larger δ/CLK ratio than a smaller one. This means, for a given clock period, increasing SET pulse width results in increasing the probability of a SET being latched. The scattered data points can be

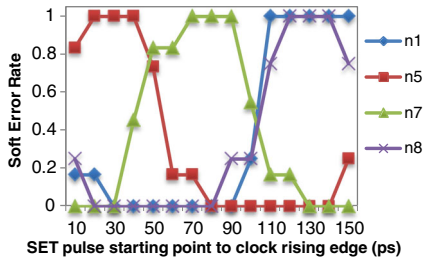


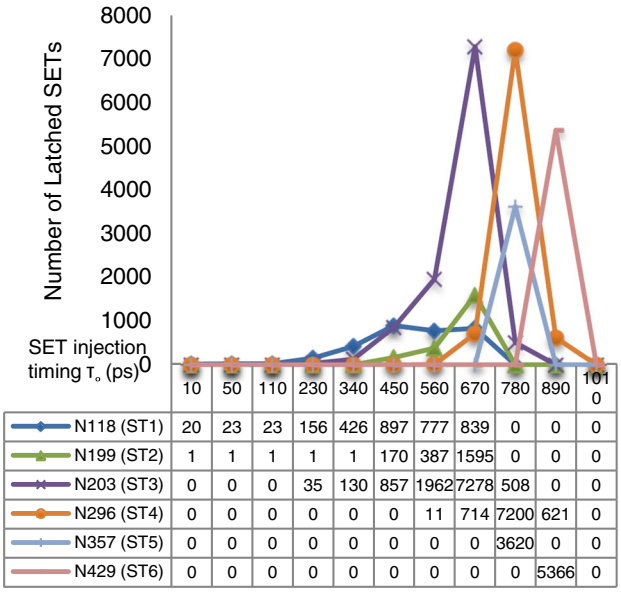
Fig. 12 Impact of SET starting timing on soft error rate for a XOR network

interpreted that random SET injection location leads to a noticeable variation on the SET latching probability, as different gates have different logic delays to reach the flip-flop latching window and different logical masking capabilities. The variation of SET latching probability does not only come from different logical masking capabilities of gates receiving SETs, but the relative delay of the gates in the critical delay path also plays an important role. Figure 15 confirms this conclusion.

We further validate our conclusions by varying the clock period and SET pulse width in the simulation of c432 and c1355. As shown in Fig. 16, no matter how δ or clock period T_{CLK} is changed, a higher ratio of δ/ T_{CLK} always results in a higher standard deviation of the number of latched SETs in a given simulation time. Figure 16 also shows that c432 has a higher standard deviation on the number of latched SETs than c1355. One of the reasons for that is c432 has a larger variety on the gate type and a higher ratio of gates w/ over w/o logical masking capability than c1355.

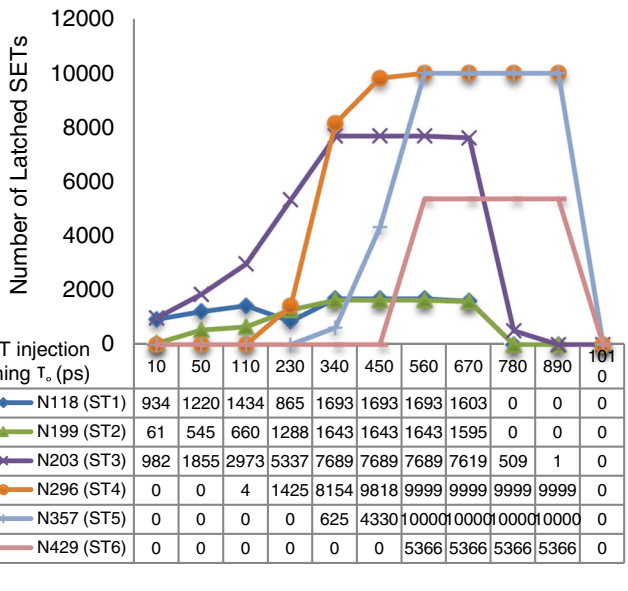
5.3.3 Impact of Gate Delay and SET Pulse Width

We examined the impact of gate delay and SET pulse width on the SET latching probability of an XOR chain shown in Fig. 7. As shown in Fig. 17, the SET latching probability is close to 1 (i.e. 100% latching probability), because XOR gate does not have inherent logical masking capability. The gate delay shown in Fig. 17 represents the position of the XOR gate in the chain. The larger gate delay means being closer to the flip-flop at the end of the XOR chain. As shown in Fig. 17, the SET latching probability of the earlier gates in the XOR chain is slightly less than that of the latter gates, when the SET pulse width is just over one clock cycle long. This is reasonable, as the earlier gate has a longer path to propagate the SET effect to the latching window and there is still a chance of error



SET injection timing T_o (ps)	10	50	110	230	340	450	560	670	780	890	1010
N118 (ST1)	20	23	23	156	426	897	777	839	0	0	0
N199 (ST2)	1	1	1	1	1	170	387	1595	0	0	0
N203 (ST3)	0	0	0	35	130	857	1962	7278	508	0	0
N296 (ST4)	0	0	0	0	0	0	11	714	7200	621	0
N357 (ST5)	0	0	0	0	0	0	0	0	3620	0	0
N429 (ST6)	0	0	0	0	0	0	0	0	0	5366	0

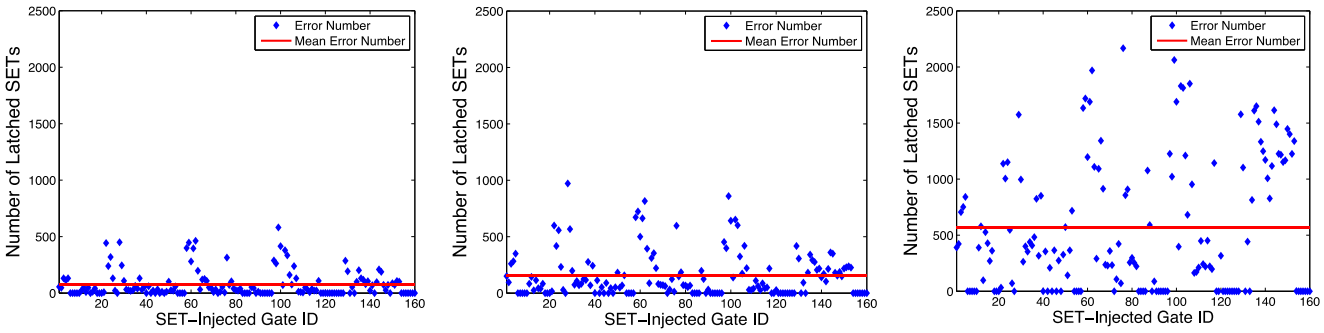
(a)



SET injection timing T_o (ps)	10	50	110	230	340	450	560	670	780	890	1010
N118 (ST1)	934	1220	1434	865	1693	1693	1693	1603	0	0	0
N199 (ST2)	61	545	660	1288	1643	1643	1643	1595	0	0	0
N203 (ST3)	982	1855	2973	5337	7689	7689	7689	7619	509	1	0
N296 (ST4)	0	0	4	1425	8154	9818	9999	9999	9999	9999	0
N357 (ST5)	0	0	0	0	625	4330	10000	10000	10000	10000	0
N429 (ST6)	0	0	0	0	0	0	5366	5366	5366	5366	0

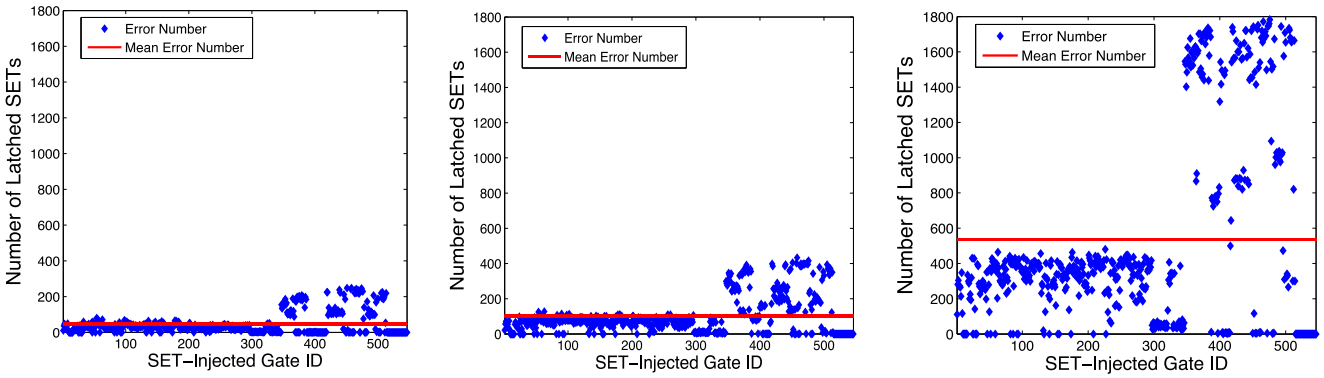
(b)

Fig. 13 The number of latched SETs for SET pluses being injected to different gates on a critical path of c432. (**a**) δ=100ps, (**b**) δ=500ps



(a) (b) (c)

Fig. 14 Impact of the ratio of SET pulse width over clock period on SET latching for c432. (**a**) δ/T_{CLK}=50/2400, (**b**) δ/T_{CLK}=100/2400, (**c**) δ/T_{CLK} =500/2400



(a) (b) (c)

Fig. 15 Impact of the ratio of SET pulse width over clock period on SET latching for c1355. (**a**) δ/T_{CLK}=50/2400, (**b**) δ/T_{CLK} =100/2400, (**c**) δ/T_{CLK} =500/2400

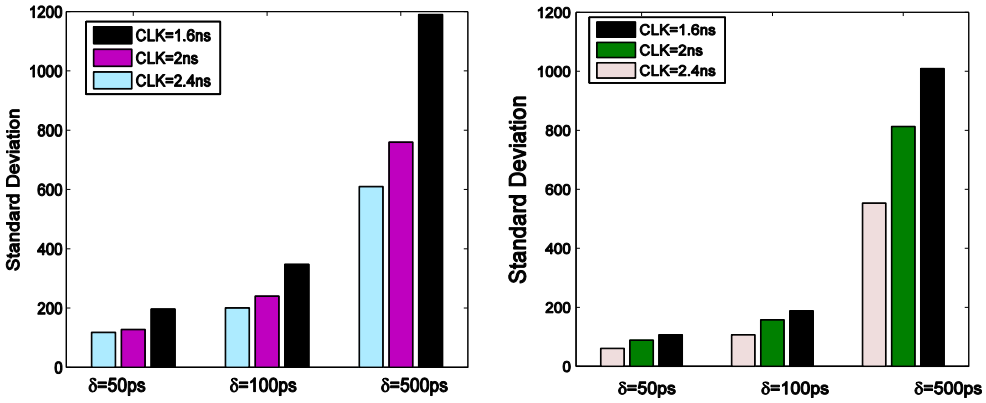


Fig. 16 Standard deviation of the latched SETs by varying clock period and SET pulse width. (**a**) c432, (**b**) c1355

masking. If we sum up all possible error conditions listed in Table 1, we have the overall SET latching probability, expressed in Eq. (20), for the gate delay within the range between T_H and $2T_{CLK}+T_H-\delta$. In this experiment, T_{CLK}, T_S and T_H are 1.6ns, 19ps, and 19ps, respectively. The inaccuracy of our derived P_{ILW} (=0.97625) is less than 2%, compared to the simulated P_{ILW} of 0.995.

$$P_{ILW} = (T_{CLK} - T_S - T_H)/T_{CLK} \tag{20}$$

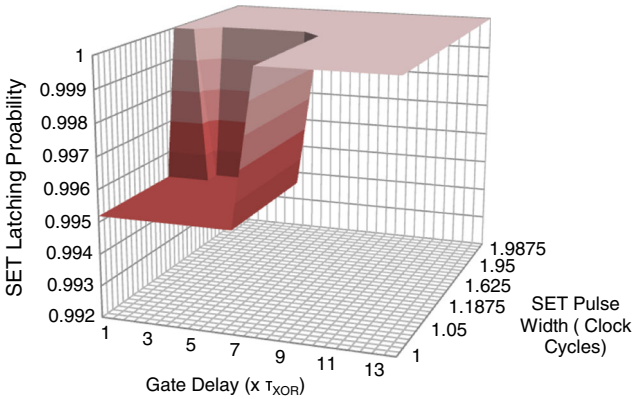


Fig. 17 Simulated SET latching probability for the XOR Chain shown in Fig. 7

Multiple-cycle SET injection in a circuit without inherent logical masking yields a SET latching probability close to 1. Next, we performed the similar experiment on a large-scale benchmark circuit c6288 from ISCAS'85, which has effects of SET pulse broadcast and re-convergence. We combined the SET latching probability and logical masking probability into the overall SER. We define the SER as the ratio of the number errors detected by comparing the faulty version with a golden model over the total test cases. As shown in Fig. 18a, generally the SER increases with the increase of δ, if δ is less than one clock cycle. For some gates that have strong logical masking capability for the given input pattern, the SER in Fig. 18a experiences some dents. When δ is greater than one clock cycle, the non-logical masking gate produces a latching probability of 1; two valleys shown in Fig. 18b are caused by logical masking. To zoom in the impact of multiple-cycle δ on the latching probability, we chose four random gates and randomized SET injection location. As shown in Fig. 19, the SET latching probability remains nearly constant when δ is slightly larger than one clock cycle. As δ increases, the SET latching probability approaches 1. The curve for random gate in Fig. 19 shows that the variation on the SET latching probability is up to 3.1%.

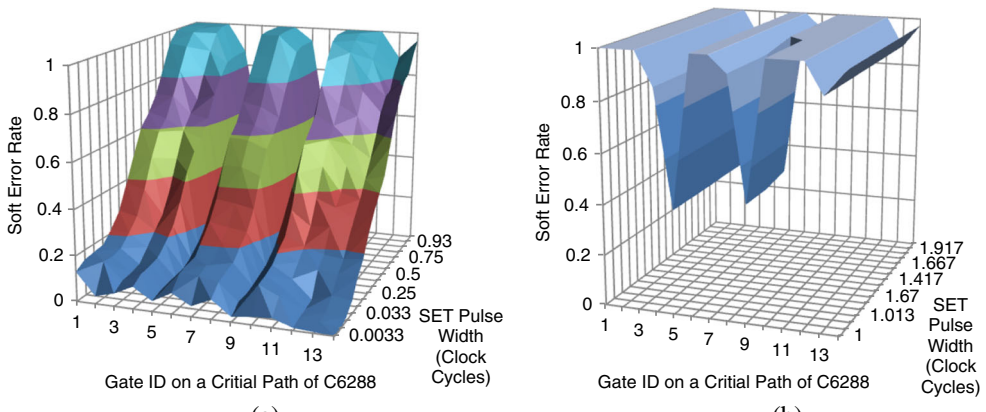


Fig. 18 Simulated SET latching probability for c6288 experiencing SET pulse (**a**) less one cycle, and (**b**) greater than one cycle

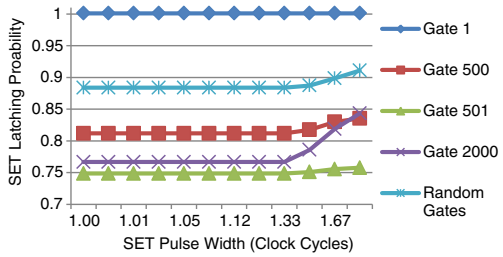


Fig. 19 Latching probability for c6288 experiencing multiple-cycle SETs

5.3.4 Simulation Time Reduction

We compared the simulation time for the random simulation to reach a stable SER with that for our semi-random method. The modified c1355 benchmark circuit was used in the experiment performed for this section. In the random simulation, the gate receiving a SET pulse and the SET starting timing were random. As shown in Fig. 20a, the SER obtained from Monte-Carlo (MC) random simulation has a variation of 50% (=the second data point 0.014286/ the last stable data point 0.028554. We ignored the first data point). In the proposed method, we used the same random input patterns as we used in the random simulation, and multiplied the measured SER with δ/T_{CLK} (=500/3200 in Fig. 20a) to predict the average SER. We specified the reasonable stable SER as the variation swing amplitude is within 5% of the final stable SER. The proposed method reaches the stable SER at the time of the 1165th cycle. The random simulation reaches a stable data point at the 2920th cycle. This means that the proposed method can reduce the simulation time by 60%, as the proposed method only need a small amount of simulation time to reach a stable SER. We increased the SET pulse width to 600ps and repeated the same experiment. As shown in Fig. 20b, the proposed method reaches the stable SER at the time of the 580th cycle. The random simulation reaches a stable data point at the 2665th cycle. This means that the proposed method can reduce the simulation time by 78.2%. We repeated the experiments on the modified benchmark circuits c432 and c6288. As shown in Fig. 21, the proposed method reduces the deviation on SER significantly faster than random simulation.

6 Conclusion

SET pulse width is typically less than one clock cycle at current technology node; however more single-event transients are expected to be latched in a system implemented in a smaller technology node. As a result, studies on the SET latching probability are imperative to precisely estimate soft error rate for integrated circuits in the nanometer regime. In previous work, the model for SET latching probability is simple and derived for singe-cycle SETs. In this work, we propose a systematic analysis method to precisely model the SET latching probability, which additionally considers SET injection location, SET starting time, and the scenarios of

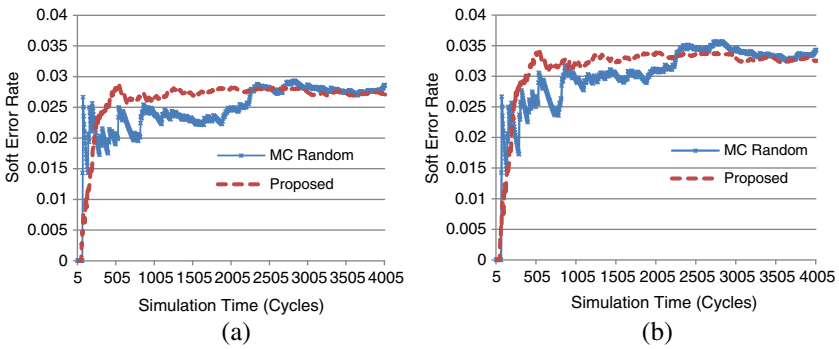


Fig. 20 Reduction of simulation time. (**a**) δ=500ps. (**b**) δ=600ps

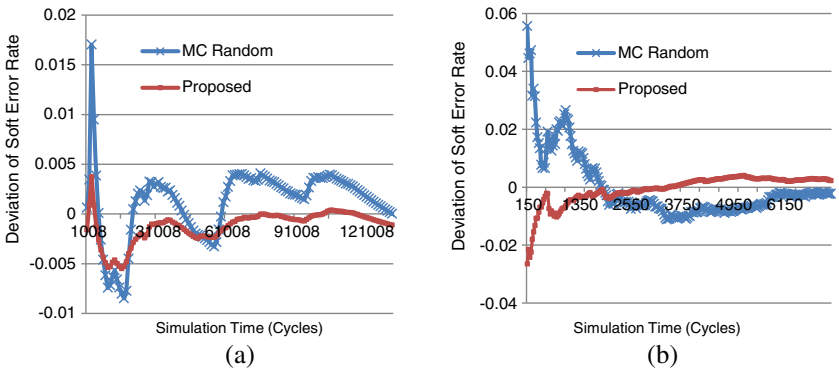


Fig. 21 Deviation reduction achieved by proposed method. (**a**) c432, (**b**) c6288

multiple-cycle SET injection. Our model is more comprehensive than the existing models for SET latching probability; thus, our model has a potential to improve the accuracy of soft error rate estimation.

Simulation on the circuit without inherent logical masking capability shows that the proposed systematic analysis method achieves up to 97% average accuracy for single-cycle SETs, and up to 98% accuracy for multiple-cycle SETs. Our case studies on ISCAS'85 benchmark circuit show that the SET latching probability has strong dependency on the SET injection location (i.e. the gate delay from the beginning of a critical path) and the SET starting time with respect to a clock latching edge. Our analytical model for new dependent parameters is consistent with the trend obtained from Monte-Carlo simulation. As our semi-random simulation method fully exploits the boundaries and explicit latching probabilities indicated in the proposed model, our method reduces the SET assessment time by up to 78% in the c6288 circuit, compared with Monte-Carlo simulation. Significantly simulation time reductions are also observed during the evaluation of soft error rate for c432 and c1355 benchmark circuits.

In this work, we assumed the SET pulse width remains same through propagation. In future work, we will extend our analytical model to include the factor of SET pulse width modification during propagation. In addition, we will extend our model by considering multiple-event transients and the impact of SET propagation through multiple pipeline stages in sequential circuits.

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