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Crosstalk Induced Fault Analysis and Test in DRAMs

ZEMO YANG AND SAMIHA MOURAD
Department of Electrical Engineering, Santa Clara University, Santa Clara, CA 95053

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Abstract. This study analyzes the effects of crosstalk-induced faults due to parameter variation during the manufacture of DRAMs. The focus is on read operations, which are sensitive to crosstalk and to neighborhood data patterns. Analytical studies and numerical simulations have been used to investigate a class of crosstalk reading faults (CRF) that read operations are susceptible to. The results reveal that there exist worst case data patterns in each physical RAM block and cell arrangement. The worst case data pattern occurs when neighboring and victim bit-lines switch to opposite values at the same time. If the bit-line arrangement is known, the test for the CRFs is quite trivial. If there is no knowledge of the internal chip structure, a deterministic pattern cannot be assigned and therefore a generic test method is needed. In this paper, a test algorithm is proposed that exhausts every state of any 3 or 5 bit-lines of a RAM block.

Keywords: crosstalk, DRAMs, pattern sensitive faults

1. Introduction

Progress in Integrated Circuits (IC) process technology has pushed the circuit and the interconnect feature size down to tens of nanometers. As a result, the complexity of the circuits as well as the circuit speeds has rapidly increased up to the "alleged" physical limits of silicon devices. Small physical size, higher speed, and lower noise margin due to the reduced power supply voltage have made coupling noise and signal integrity increasing concerns in IC design. Coupling noise is known to be due to the mutual capacitance and inductance that exist between the interconnect lines on the IC. This has prompted analytical studies to be performed on the internal interconnects of an IC. When the magnitude of the crosstalk exceeds a certain limit, there is the potential risk of the internal circuit toggling incorrectly. In addition to the problem of the crosstalk voltage generated at the victim lines, a timing difference can also be induced as a result of the differences in the signal propagation modes of the interconnects. These modes are closely dependent on data pattern through the interconnect lines. The switching of neighborhood lines can result in an increase or a decrease of the propagation delay [5–7]. All of studies discussed to this point are based on the generic model of a CMOS driver driving another CMOS gate through interconnects. A more recent study covered crosstalk resulting from weak bridging defects [26].

Compared to logic circuits, RAMs have many more long parallel lines, which provide a greater probability for excessive crosstalk coupling especially among the bit-lines [8–10]. Eventually, a folded-bit-line architecture was employed to avoid common mode noise. This architecture has a reference bit-line for each data bit-line. Twisted bit-lines are often used to further reduce the coupling effect between adjacent bit-lines, [10]. This structure can reduce the coupling between the directly adjacent bit-lines but it increases the complexity of the layout as well as the likelihood of creating shorts between non-adjacent lines. In addition, a complicated twisted bit-line design might reduce the product's yield. Therefore, some DRAM manufacturers have chosen to abandon this structure in favor of smaller block sizes. Crosstalk among bit-line arrays is much greater than in ordinary logic circuits partly because they require highly sensitive voltage-sensing circuits to detect the values. The increased complication of the coupling process due to the data stored in DRAM cells, is referred to as neighborhood-pattern sensitivity (*NPS*). The DRAM read operation is significantly affected by a number of factors, including the magnitude of the cell capacitance, the arrangement and layout of the cell array, the bit-line architecture, the material properties, the neighborhood data patterns, and the sense amplifier (SA) [11]. Although extensive simulations are performed in the design phase to ensure a sufficient noise margin, the process parameter fluctuation and defects

introduced during fabrication can also cause a chip to fail [12–15].

A number of studies have been undertaken to detect neighborhood pattern-sensitive faults in DRAMs [16–19]. These tests, which are based on mathematical models of state machines, use exhaustive test sets. They were performed primarily on a highly abstract model of a RAM array without consideration for the physical failure modes. More recently, the dynamic behavior of DRAMs has been used to define speed-related fault models and test methods [21–23].

Manufacturing defects can be modeled by stuck-at and bridging faults at the cell, word-line, bit-line, decoder, and sensing-circuit levels. These kinds of faults are easily observable and most usually readily detected during the final test. Some defects, however, only cause local variations in electrical parameter such as the resistance or capacitance. In addition, lower voltage, higher temperature, or higher speed might create a condition that produces reading faults only for certain patterns in the neighborhood data.

This paper presents a study of crosstalk-induced faults that result from process defects. The effect of crosstalk on the read operation in a DRAM is described in Section 2. An analytical investigation of the read operation and how crosstalk affects it is given in Section 3. That is followed by a discussion of the simulation of an ASIC DRAM in Section 4. As a consequence of understanding the cause of these faults, we developed two test algorithms that detect the crosstalk-induced faults, as described in Section 5 of this paper.

2. Crosstalk in DRAMs

Crosstalk exists among word-lines, bit-lines, and between word-lines and bit-lines of a DRAM [10]. Among neighboring word-lines, crosstalk can cause data retention problems because sub-threshold leakage increases in the word-line as its neighbor is turned on [11]. Previous analytical studies have shown that lowering the effective resistance of word-lines can efficiently reduce the coupling voltage magnitude [1, 2]. Following the same principle, lowering the effective resistance of the word-lines can reduce the sub-threshold leakage induced by crosstalk among word-lines. Crosstalk between bit-lines and word-lines causes similar data retention problems but the magnitude is much smaller because the bit-lines and word-lines have a perpendicular orientation and the voltage swing of a bit-line and its complement are in opposite directions. Thus, the coupling voltage due to the switching of these two bit-lines signals cancels out. Coupling between word-lines and bit-lines causes problems in an open bit-line DRAM block structure, but becomes much less of a problem when a folded bit-line structure is used.

Crosstalk among bit-lines has always been most significant because (1) bit-lines are long parallel lines, (2) all bit-lines in a memory block can be switched at the same time during read/write operations, and (3) highly sensitive differential sense amplifiers (SAs) are involved with their initial state close to the switching point. Therefore, we will focus on the analysis of crosstalk among bit-lines during the read operation with an emphasis on the cases involving defects and parameter variations.

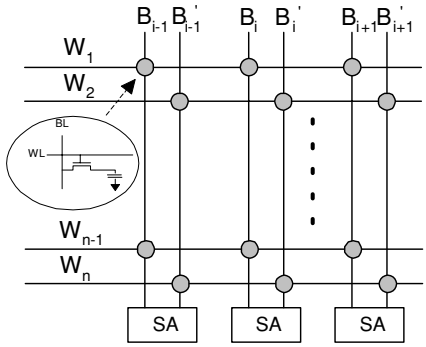


Fig. 1. Representation of a DRAM memory block.

2.1. Reading Operation

A basic DRAM array is shown in Fig. 1. It consists of memory cells at the intersections of bit-line pairs, (B_{i-1}, B'_{i-1}), (B_i, B'_i) and (B_{i+1}, B'_{i+1}), and word-lines, W_1, W_2 ... W_j ...W_n. Each bit-line pair is connected to a SA. The memory cell is composed of a transistor and a capacitor in which the data is stored. Each SA consists of a latch with some auxiliary transistors to control its operation [10]. An example of an SA is shown in Fig. 2. It shows a latch that is isolated from its power rails by the switches SE and SE'. The read operation of a memory cell using the bit-line pair *i* consists of the three stages illustrated in Fig. 3, where the voltages of the bit-lines connected to the same SA are plotted versus time over the entire read cycle. The waveforms in the figure represent the case where the value stored in memory cell is a "0". The shape of each waveform depends on the value of

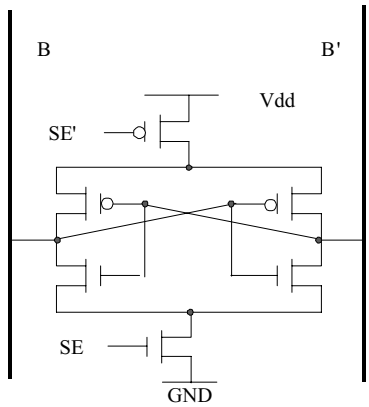


Fig. 2. Circuit of the sensing Amplifier [10].

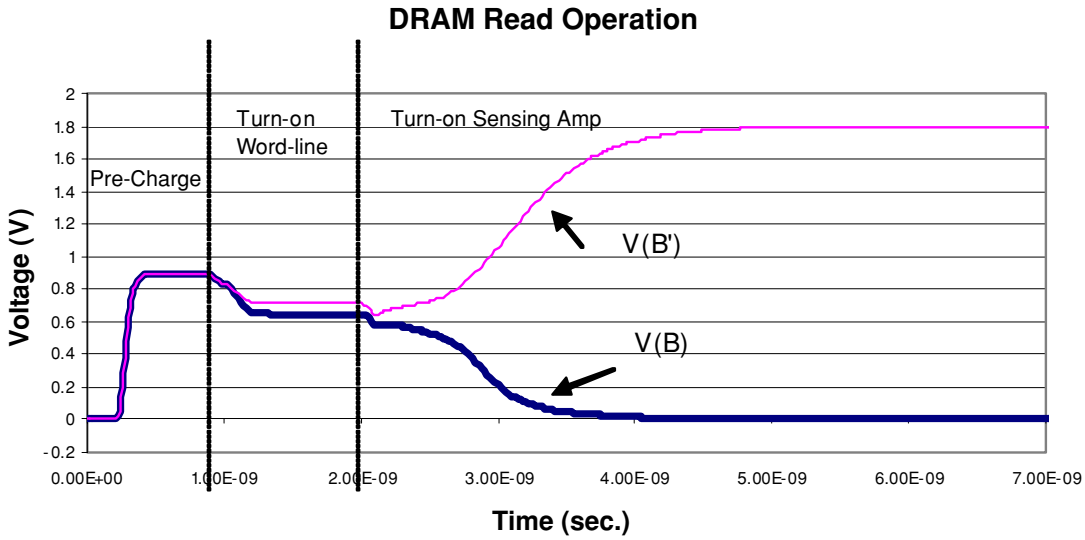


Fig. 3. Stages of the read operation.

the memory cell because the stored voltage level determines how much influence the coupling capacitance between the bit-lines will have on the final value [8, 10].

Due to the high-gain that is inherent in positive feedback, this SA can detect very small voltage differences that exist between the pair of bit-lines, B_i and B_i'. In the first phase of the read cycle, all the bit-lines in the array are precharged to a voltage level of $V_{dd}/2$ so that they only have to swing through half of the voltage range to reach the correct value, which allows for faster reading. The word-line is activated in the second phase and the storage capacitor is either charged or discharged depending on the data previously written into the cells. Under certain approximations, this voltage difference can be calculated using a charge-sharing model [8]. The third phase consists of turning on the SA ($SE = 1$, $SE' = 0$) while the voltage on the word-line is still high. The voltages on the pair of bit-lines will then diverge from each other towards their expected values, one high and the other low.

At the beginning of the third phase of the read cycle, the SA can be represented by the small signal model shown in Fig. 4. In this model, Cc is the coupling capacitance between the two bit-lines while G_N and G_P are the small signal gains of the NMOS and the PMOS transistors, respectively. C_1 and C_2 are the total capacitance associated with bit-line B_i and its complement B_i', respectively. C_1 consists of the line capacitance of bit-line B_i, the cell capacitance, and the diffusion capacitances C_{dif} of all the transistors connected to bit-line B_i. Thus, $C_1 = C_L + C_{\text{cell}} + C_{\text{dif}}$ while $C_2 = C_{\text{L}} + C_{\text{dif}}$ if a cell associated with bit-line B_i is turned on. After the SA is turned on, the high gain of its positive feedback will pull down the lower voltage port and pull up the higher voltage port, thus completing the voltage sensing and the write back steps. In the special case where reference cells are used in the RAM, the capacitances of the reference cells should be added to C_1 and C_2.

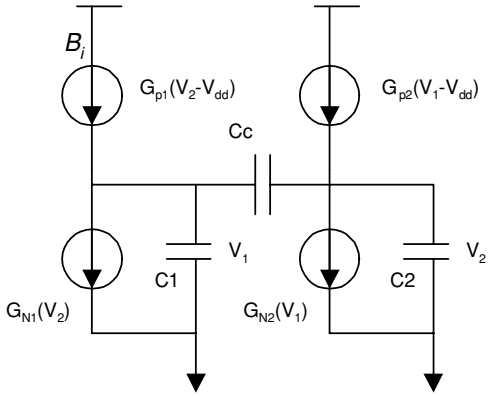


Fig. 4. Equivalent circuit of the sense amplifier during the read operation. $C_1 = C_{\text{line}} + C_{\text{cell}} + C_{\text{dif}}$ if the cell under read is associated to bit-line B_i.

Each bit-line i is also coupled to the adjacent bit-line in the neighboring bit-line pair. C_d denotes the coupling capacitance between B_i (or B_i') and its neighbor B_{i-1}' (or B_{i+1}). The equivalent circuit for the three pairs at the beginning of phase three of the read operation is shown in Fig. 5.

Due to the various coupling capacitances in this model, the crosstalk signal is likely to cause a false output from the read operation depending on the stored data patterns.

2.1.1. Crosstalk Reading Faults. Under normal operation with the correct values of the coupling capacitances between the bit-lines and word-lines, the value read from the cell is expected to be correct. However, a fault may occur due to variation in the coupling capacitance or the resistive values of the bit-lines. These factors are even more disruptive in the presence of specific patterns of stored data since they are likely to trigger crosstalk faults. Because of this relationship, these faults may be considered a subset of pattern sensitive faults [18] and we call this fault *crosstalk reading faults*

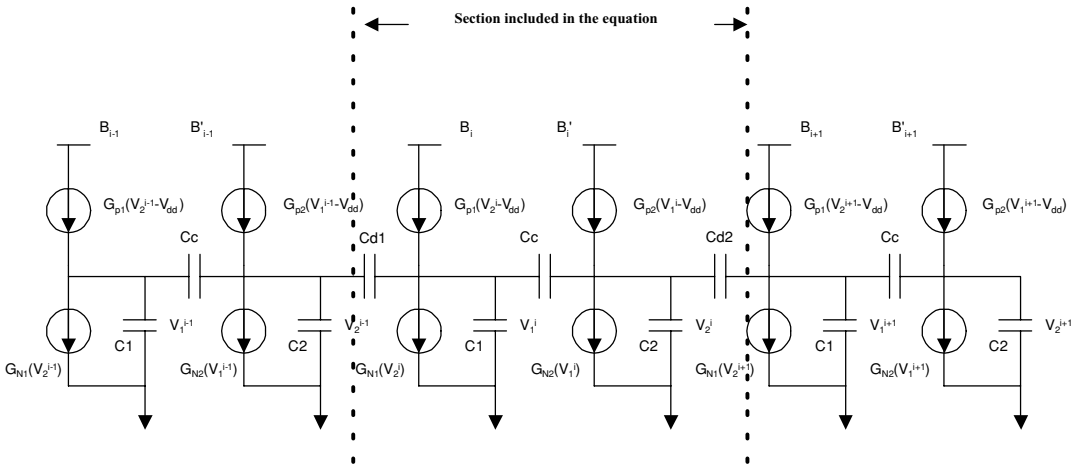


Fig. 5. Equivalent circuit of sense amplifiers and bit-lines during the read operation.

(CRFs). While crosstalk faults may be only temporary faults in themselves, in the case of the DRAM the effects of these faults are permanent because the faulty value is immediately rewritten into the same location. An analytical study was done to analyze these faults and was then followed up by a simulation experiment in Section 4 to confirm our findings.

CRFs occur when reading is performed for particular stored patterns that we will refer to as *worst case patterns* [8]. Worst case patterns occur when every bit-line swings in the opposite direction of its two neighboring bit-lines. These patterns are dependent on the physical arrangement of the DRAM core cell. Through Section 4 of the paper we will concentrate on the architecture shown in Fig. 1. This will change in Section 5 when we describe test pattern generation for these faults and show how it is affected by the architecture. CRFs can occur on any bit-line whose immediately adjacent bit-lines are switching in the opposite direction during a read operation. For example, using the arrangement in Fig. 1, any word-line associated with zeros stored in the three bits of the word will cause the six bit-lines involved in the reading to switch in opposite direction. Hence the worst case patterns are 000 and 111.

For a given cell arrangement, bits in the same word are not necessarily physically adjacent. Since the physical layout is usually not disclosed by the DRAM IP provider, exercising the RAM for the all 0s pattern is thus not a sufficient test. This issue will be elaborated on in Section 5 when test pattern generation is described.

3. Analytical Derivation of the Effect of Crosstalk

In this section, we will derive an expression for the voltage difference across the latch of the SA and use it to understand the effect parameter variations have on the RAM's read operation. The voltage difference is quite small because the initial state of this latch is near its metastable point. With all four transistors of the latch in saturation mode, a small signal model of the MOS transistor can be used to accurately analyze the latch operation [24, 25]. An equivalent circuit for modeling the SA operation can be created by combining the small signal model of the latch, a bit-line pair, and the neighborhood bit-line pairs. As shown in Fig. 5, three pairs of adjacent bit-lines and the associated SAs are represented by an equivalent circuit with capacitors and voltage-controlled current sources. The three pairs are coupled with capacitors C_{d1} and C_{d2}. Amongst the circuitry associated with the center pair SA, which is the circuit of interest, the following equations can be written using KCL (Kirschoff Current Law):

$$\begin{aligned} G_{P1}\left(V_2^i - V_{DD}\right) &= G_{N1}V_2^i + C_1\frac{dV_1^i}{dt} + C_C\frac{d}{dt}\left(V_1^i - V_2^i\right) \\ &\quad - C_{d1}\frac{d}{dt}\left(V_2^{(i-1)} - V_1^i\right) \qquad (1) \\ G_{P2}\left(V_1^i - V_{DD}\right) &= G_{N2}V_1^i + C_2\frac{dV_2^i}{dt} - C_C\frac{d}{dt}\left(V_1^i - V_2^i\right) \\ &\quad + C_{d2}\frac{d}{dt}\left(V_2^i - V_1^{(i+1)}\right) \qquad (2) \end{aligned}$$

where, the notation $(i-1)$ and $(i+1)$ refer to the pairs on each side of pair i of bit-lines.

After defining $\Delta V = V_1^i - V_2^i$ and performing the detailed deduction shown in the appendix, the solution for the voltage difference between the two bit-lines associated with the same SA becomes

$$\begin{aligned} \Delta V = {} & \Delta V^+ e^{\lambda_1 t} + \Delta V^- e^{\lambda_2 t} \\ & - \frac{(G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}}{(G_{P1} - G_{N1})(G_{P2} - G_{N2})} \\ & + \frac{C_{d1}(G_{N2} - G_{P2})}{\sqrt{B^2 - 4AC}}\lambda_1 V_2^{+(i-1)} t e^{\lambda_1 t} \\ & + \frac{(C_2C_{d1} + C_{d1}C_{d2})}{\sqrt{B^2 - 4AC}}(\lambda_1)^2 V_2^{+(i-1)} t e^{\lambda_1 t} \\ & - \frac{C_{d2}(G_{N1} - G_{P1})}{\sqrt{B^2 - 4AC}}\lambda_1 V_1^{+(i+1)} t e^{\lambda_1 t} \\ & - \frac{(C_1C_{d2} + C_{d1}C_{d2})}{\sqrt{B^2 - 4AC}}(\lambda_1)^2 V_1^{+(i+1)} t e^{\lambda_1 t} \qquad (3) \end{aligned}$$

Where $\lambda_1 = \frac{-B+\sqrt{B^2-4AC}}{2A}$, $\lambda_2 = \frac{-B-\sqrt{B^2-4AC}}{2A}$ are the solutions of the characteristic equation, and

$$\begin{aligned} A &= (C_1C_2 + C_1C_C + C_1C_{d1} + C_CC_2 + C_CC_{d2} + C_2C_{d1} \\ &\quad + C_CC_{d1} + C_{d1}C_{d2}), \\ B &= -C_C(G_{P1} - G_{N1} + G_{P2} - G_{N2}) \text{ and} \\ C &= -(G_{P1} - G_{N1})(G_{P2} - G_{N2}). \end{aligned}$$

The first two terms of (3) are solutions of the homogenous equation. Under normal operation $\lambda_1 > 0$ and $\lambda_2 < 0$. The remaining terms are the particular solutions. The third term, which contributes to the DC level of the solution, depends on the SA parameters but is usually a fraction of V_{dd}. The last four terms are functions of the voltages at the neighboring bit-lines B_{i-1} and B_{i+1}. When data stored in the cell i is "0", the initial condition for the read operation is $\Delta V|_{t=0} < 0$ which yields $\Delta V^+ < 0$ with the magnitude of the first term of (3) increasing exponentially with time from that point on. This is a good mathematical description of how a differential SA typically behaves. Crosstalk from the neighboring bit-lines plays a role in accelerating or drawing back the voltage differential between the bit-lines and. When the value stored at both cell $i-1$ and cell $i+1$ is "0", and. Under these conditions the crosstalk terms are all positive so they tend to increase the voltage differential while the first term tends to reduce the same voltage. Similarly, if a "1" is stored in cell $i-1$ and $i+1$, then. $V_2^{+(i-1)} < 0$. and $V_2^{+(i+1)} > 0$. In this case the crosstalk terms are negative, which helps the SA of group i to differentiate between the signals on its lines. In the extreme case when the coupling capacitances are not balanced, CRFs may occur. Using the three bit-line pairs in Fig. 1 as an example, crosstalk during the read operation will result in the three bits connected to the same word-line being all 0s or all 1s.

If a parameter such as C_L or C_C differs from its nominal value due to process variations, the solution will have a different form because the characteristics of the central bit-pair will no longer be the same as the neighborhood bit-lines. For this case, $\lambda_1^{(i-1)}$, $\lambda_1^{(i+1)}$are no longer solutions for the characteristic equation of the bit-line group, and so $A\lambda_1^{(i-1)^2} + B\lambda_1^{(i-1)} + C \neq 0$, and $A\lambda_1^{(i+1)^2} + B\lambda_1^{(i+1)} + C \neq 0$. The solution of the voltage difference is:

$$\begin{aligned} \Delta V = {} & \Delta V^+ e^{\lambda_1 t} + \Delta V^- e^{\lambda_2 t} \\ & - \frac{(G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}}{(G_{P1} - G_{N1})(G_{P2} - G_{N2})} \\ & + \frac{C_{d1}(G_{N2} - G_{P2})}{A\lambda_1^{(i-1)^2} + B\lambda_1^{(i-1)} + C} \lambda_1^{(i-1)} V_2^{+(i-1)} e^{\lambda_1^{(i-1)} t} \\ & + \frac{(C_2C_{d1} + C_{d1}C_{d2})}{A\lambda_1^{(i-1)^2} + B\lambda_1^{(i-1)} + C} \left(\lambda_1^{(i-1)}\right)^2 V_2^{+(i-1)} e^{\lambda_1^{(i-1)} t} \\ & - \frac{C_{d2}(G_{N1} - G_{P1})}{A\lambda_1^{(i+1)^2} + B\lambda_1^{(i+1)} + C} \lambda_1^{(i+1)} V_1^{+(i+1)} e^{\lambda_1^{(i+1)} t} \\ & - \frac{(C_1C_{d2} + C_{d1}C_{d2})}{A\lambda_1^{(i+1)^2} + B\lambda_1^{(i+1)} + C} \left(\lambda_1^{(i+1)}\right)^2 V_1^{+(i+1)} e^{\lambda_1^{(i+1)} t} \end{aligned} \tag{4}$$

Process defects may introduce bridging faults between lines on the RAM plane. When bridging occurs between the bit-lines of the same SA, the equivalent circuit can be modeled by adding a resistor across the coupling capacitor C_c shown in Fig. 5. With the conductance of the shorting resistor being denoted as G, the KCL equations describing the bit-line group are:

$$\begin{aligned} G_{P1}(V_2 - V_{DD}) &= G_{N1}V_2 + C_1\tfrac{dV_1}{dt} + C_C\tfrac{d}{dt}(V_1 - V_2) \\ &\quad + G(V_1 - V_2) - C_{d1}\tfrac{d}{dt}\left(V_2^{(i-1)} - V_1\right) \end{aligned} \tag{5}$$

$$\begin{aligned} G_{P2}(V_1 - V_{DD}) &= G_{N2}V_1 + C2\tfrac{dV_2}{dt} - C_C\tfrac{d}{dt}(V_1 - V_2) \\ &\quad - G(V_1 - V_2) + C_{d2}\tfrac{d}{dt}\left(V_2 - V_1^{(i+1)}\right) \end{aligned} \tag{6}$$

Solving the (5) and (6) and assigning $B' = [B + G(C_1 + C_2 + C_{d1} + C_{d2})]$, $C' = [C + (G_{N1} - G_{P1} + G_{N2} - G_{P2})G]$, the solution for the voltage difference with a bridging fault can be obtained:

$$\begin{aligned} \Delta V = {} & \Delta V^+ e^{\lambda_1 t} + \Delta V^- e^{\lambda_2 t} \\ & - \frac{(G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}}{(G_{P1} - G_{N1})(G_{P2} - G_{N2})} \\ & + \frac{C_{d1}(G_{N2} - G_{P2})}{A\lambda_1^{(i-1)^2} + B'\lambda_1^{(i-1)} + C'} \lambda_1^{(i-1)} V_2^{+(i-1)} e^{\lambda_1^{(i-1)} t} \\ & + \frac{(C_2C_{d1} + C_{d1}C_{d2})}{A\lambda_1^{(i-1)^2} + B'\lambda_1^{(i-1)} + C'} \left(\lambda_1^{(i-1)}\right)^2 V_2^{+(i-1)} e^{\lambda_1^{(i-1)} t} \\ & - \frac{C_{d2}(G_{N1} - G_{P1})}{A\lambda_1^{(i+1)^2} + B'\lambda_1^{(i+1)} + C'} \lambda_1^{(i+1)} V_1^{(i+1)} e^{\lambda_1^{(i+1)} t} \\ & - \frac{(C_1C_{d2} + C_{d1}C_{d2})}{A\lambda_1^{(i+1)^2} + B'\lambda_1^{(i+1)} + C'} \left(\lambda_1^{(i+1)}\right)^2 V_1^{(i+1)} e^{\lambda_1^{(i+1)} t} \end{aligned} \tag{7}$$

where $\lambda_1 = \frac{-B'+\sqrt{B'^2-4AC'}}{2A}$, and $\lambda_2 = \frac{-B'-\sqrt{B'^2-4AC'}}{2A}$, and $\lambda_1^{(i-1)}, \lambda_1^{(i+1)} = \frac{-B+\sqrt{B^2-4AC}}{2A}$.

If the bridging resistance is very high, namely as $G \to 0$, then $B' \to B$ and $C' \to C$, which reduces (7) to (4). On the other hand, if the resistance is a very small value such as 1Ω, the initial voltage difference between the bit-lines is almost zero. More importantly, λ_1 and λ_2 are negative and so the characteristic terms of the equation decay rapidly. The value of ΔV remains zero for all cases, even where coupling voltages from the neighboring bit-lines exist.

4. Simulation Study

The analytical study in the preceding section gives a description of how crosstalk from neighboring bit-lines induces a

faulty reading, especially when aggravated by defects or fluctuations in process parameters. However, to make the results more accurate the small signal gains G_n and G_p for the latch transistors need to be extracted from the SA circuit using a detailed SPICE model at a specific voltage level. These small signal gains are sensitive to the voltage level the transistor is operating at and can change significantly during the sense operation [25]. Therefore, a time-stepped transient analysis and a recalibration of G_n and G_p at each step are needed for accuracy. The purpose of the analytical study is to clearly describe the physics during the read operation. In order to produce a simulation that is accurate enough to base design decisions on, a more accurate model and numerical calculations are required. In the following sections we will use SPICE to analyze the effect of crosstalk, in the presence of parameter fluctuations, on the DRAM read operation.

4.1. Experiment Setup

In this experimental study the configuration in Fig. 1 is represented by a SPICE model where each of the 400 μm long aluminum bit-lines is represented by an equivalent distributed RC circuit. The model also includes the cell transistors, and the coupling capacitance. The memory cell is represented by a 25 fF capacitor and an NMOS transistor with $W/L = 0.24\ \mu m/0.18\ \mu m$ using a 0.18 μm technology. Table 1 lists the parameters for the lines and transistors. For the SA circuit shown in Fig. 2, the aspect ratio of the transistors is 3 μm/0.18 μm. A level-42 transistor HSPICE model was used in the simulation.

We studied the impact that process defects and parameter variations had on each of the capacitances between: (a) bit-lines of the same SA, (b) bit-lines of two adjacent SAs, and (c) a bit-line and ground or V_{dd}. The capacitor associated with each case, C_C, C_d, and C_L respectively, are shown in Fig. 5. Extra resistors are added between the bit-lines to simulate bridging faults and between a bit-line and power or ground to simulate stuck-at faults. Circuit simulations of the read operation were performed for each of the possible eight data patterns that could be stored in the three bits associated with a single word-line in the configuration under test. The simulations were performed for a range of capacitance (or resistance) values centered around the nominal value but reaching out to values that are much less likely to occur. Even though the probability of some of the values occurring is very low, the wide range allows for the examination of the read operation's sensitivity to variations in these parameters. The results are presented and interpreted in the next subsections.

Table 1. Spice circuit parameters

Technology	0.18 μm
Vdd (V)	1.8
Vtn (V)	0.35
Vtp (V)	0.42
R (Ω/mm)	108.8
C (fF/mm)	32.1
Cm (fF/mm)	56.8

4.2. Effect of Coupling Capacitance Cc between Bit-Line Pairs

In this subsection, we vary the value of the coupling capacitor, C_C, between the complementary bit-line pair B_i and that share the same SA. Fig. 6 shows the waveforms on bit-line B_i during the read operation when the values stored in the three adjacent cells associated with word-line W_1 are 000. The waveforms for several values of the coupling capacitor C_C are shown. The heavy line represents the waveform of the *good* circuit with the nominal C_C value. The lighter lines are the waveforms corresponding to the values of C_C ranging from 1.5 to 3 times its nominal value.

For most of the waveforms, the voltages of the bit-line, and at the connected cell are eventually pulled down to zero, the original state of the stored data. As the capacitance of C_C increases to 1.9 times its nominal value, the final result is still correct but the fall time increases. When C_C is greater than twice its nominal value, the data is always incorrect. The metastable state occurs when C_C is about 1.9 times, that is 90% higher than, its nominal value.

As C_C increases beyond twice its nominal value, the read result is incorrect only for the data pattern 000. Based on the analytical study, 000 is indeed one of the two "worst case" data patterns for the cell architecture shown in Fig. 1. Pattern 000 is worse than 111 for the specific latch design of the SA where the NMOS is stronger than PMOS. When the aspect ratio of the PMOS transistors is increased to three times that of the NMOS transistors, in order to balance the ON resistance of the transistors due to the mobility difference, the same faulty reading appears with the 111 pattern as well. An important point to note is that the faulty reading is caused by crosstalk among neighboring bit-lines since no faulty readings happen when the simulation consists of only one set of bit-lines and the sensing circuitry.

4.3. Effect of the Coupling Capacitance Cd

A similar set of simulations were performed with the coupling capacitance between the neighboring bit-lines of two adjacent SAs: In this setup a faulty reading occurs when C_{d1} and C_{d2} are both 2.6, or more times their nominal value with the data pattern 000. However, unlike the previous case with Cc, the bit-line arrangement is non-symmetrical because SA_{i-1}, and SA_{i+1} have no adjacent neighbors on the left-hand side and right-hand side, respectively. To achieve a meaningful result for all three bits, five pairs of bit-lines need to be included in the SPICE model and more data pattern combinations (2^5) need to be simulated. Verification

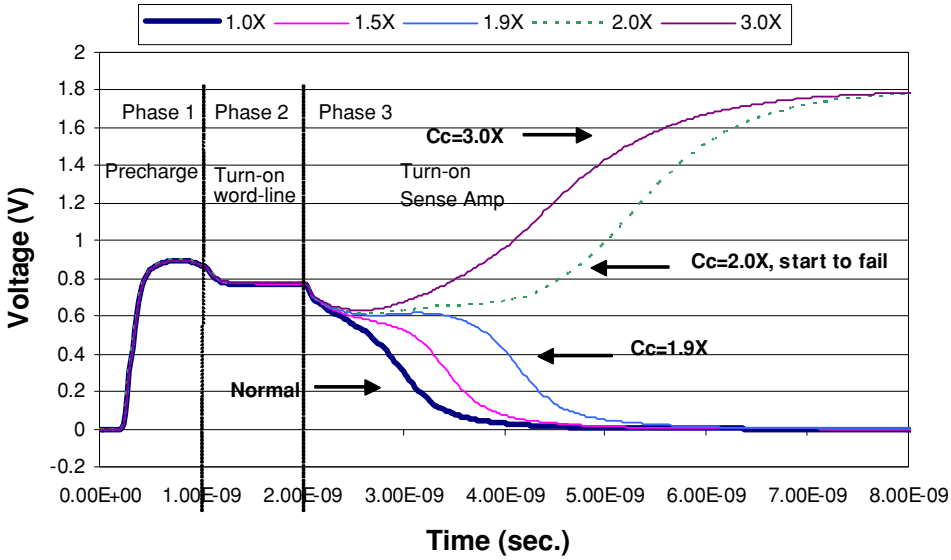


Fig. 6. Simulation result of a read operation with various Cc values.

studies with a five-group bit-line model were performed to check the validity of the center bit B_i in all 2^5 data patterns. The results for the center bit-line B_i are identical to the three-group bit-line result described above. This means that in order to study further such behaviors only one neighboring bit-line is required on each side.

4.4. *Effect of the Capacitance to Ground, C_L*

A simulation study was conducted to examine the effect of the variations in C_L in the configuration of Fig. 1 with the equivalent circuit shown in Fig. 5. The experiment consisted of storing all eight possible data patterns in bits $i-1$, i and $i+1$ of the same word while increasing C_L up to 10 times its nominal value. The only CRFs that occurred were for the patterns indicated in Table 2. The first column of the table lists the capacitance to ground in terms of the nominal value, which is indicated as 1X. The other four columns show the data that was read back with the corresponding value of C_L. The initial values stored in the bits are the values shown in the 1X row for each column. In all of the cases included in the table, the stored data on the center bit, bit i, is "0". The simulation clearly displays the pattern sensitivity caused by crosstalk among the neighboring bit-lines, $i-1$ and $i+1$. For the pattern 000, which was encountered as the worst case

Table 2. Effect of the capacitance C_L

C_L	Read data			
1X	000	100	001	101
1.9X	010	100	001	101
5X	010	110	001	101
10X	010	110	011	101

in previous simulations, the adjacent neighbor of each bit-line, in the pair under consideration, switch in the direction opposite to that bit-line. One would have expected the same CRFs to be displayed for all patterns. However, for the other two patterns, 100 and 001, the capacitive loads on the bit-lines are not symmetrical as was noted in Section 2, where $C_1 > C_2$. Thus the faults do not first appear at the same value of capacitance. For the last pattern 101, the crosstalk does not cause any faults since, under this pattern, it rather helped the SA to read the correct value.

4.5. *Effect of Resistive Short between Bit-line Pair*

During the IC manufacturing process, defects, such as incomplete removal of metal, can often cause a bridging short between lines. This fault is usually modeled as a resistor connected to two lines with a value in the order of 1 Ω to 10^6 Ω. In this section, we study the impact of the bridging short between the same SA pair of bit-lines. According to the analytical study from Section 3 (Eqs. (5), (6) and (7)) of the paper, the bridging resistor can change the characteristic solutions of the sensing circuitry as shown in the equation, $\lambda_1 = \frac{-B'+\sqrt{B'^2-4AC'}}{2A}$, $\lambda_2 = \frac{-B'-\sqrt{B'^2-4AC'}}{2A}$. In this equation, $B' = [B + G(C_1 + C_2 + C_{d1} + C_{d2})]$, $C' = [C + (G_{N1} - G_{P1} + G_{N2} - G_{P2})G]$, G is the conductance of the bridging resistor. Using numerical parameters, we calculated the value of λ_1 and λ_2 with the various bridging resistance values when the data pattern stored in the cells is 000. The results are listed in Table 3. For each value of the bridging resistor listed in column 1, the values of λ_1 and λ_2 are given in the next two columns. The last row gives the correct parameter for the good circuit (no short). According to the results, the sense amplifier can't differentiate the voltage when the bridging resistor has a value lower

Table 3. Characteristics of the sensing circuitry with a range of bridging resistors.

Case	λ_1	λ_2
$R_b = 1\ \Omega$	−5.62E+09	−6.55E+12
$R_b = 1\ k\Omega$	−2.99+09	−5.66E+09
$R_b = 10\ k\Omega$	2.87E+09	−5.55E+09
$R_b = 100\ k\Omega$	2.92E+09	−4.36E+09
Normal	3.46E+09	−5.56E+09

than 1 kΩ because both exponential terms of the characteristic equation are decaying. When the bridging resistance is in the range of 10 kΩ, the sense amplifier begins to respond but at a lower speed. In this range, the read operation is susceptible to CRFs from the neighborhood data patterns.

Using the analytical formula deduced in Section 3, we further estimated the voltage difference between B_i and B_i' when the stored data is 000. The calculation was performed in two time segments: before and after the voltages settled in the neighborhood. The results are plotted in Fig. 7(a) for the values of the bridging resistance in Table 3. Segment one represents the phase before the neighborhood bit-lines reach their final state so the crosstalk terms are included. Segment two represents the phase after the neighborhood bit-lines have reached their final state, which is after the crosstalk terms have subsided. The crosstalk terms diminish since dV/dt at these lines is zero. When the value of the bridging resistor is 1 Ω, there is no significant voltage difference between B_i and B_i', so ΔV is a constant. When the resistance is 1 kΩ, it is big enough to stand an initial voltage difference between B_i and B_i'. However, both of the characteristic terms decay with time since λ_1 and λ_2 are both negative. During the switching period of the neighborhood bit-lines, the crosstalk coupling voltage contributes significantly to establishing a voltage difference betweenB_i and B_i'. After the neighborhood bit-lines reach their final voltage level, the crosstalk terms diminish in importance and the decay characteristics of the SA dominate. The final voltage difference betweenB_i and B_i' diminishes after a period of time as well. When the bridging resistor reaches 10 kΩ, the SA starts to work according to the calculated result in Table 3, but the strong crosstalk from the neighborhood bit-lines toggles the bias of the voltage across B_i and B_i' before the neighborhood bit-lines settle to their final states. As a result, the initial condition of the second time segment changes to positive (the 000 data pattern causes the initial voltage difference across B_i and B_i' to be negative). Finally a faulty reading "1" is reached as the voltage atB_i reaches V_{dd} and B_i' reaches 0. When the bridging resistance increases to the level of 100 kΩ, the exponentially increasing term is stronger than the crosstalk terms and the final ΔV reaches its correct final state. We show the results of the simulations for the same range of bridging resistances in Fig. 7(b). Both set of results, calculated and simulated are in agreement.

4.6. Resistive Short to Power and Ground

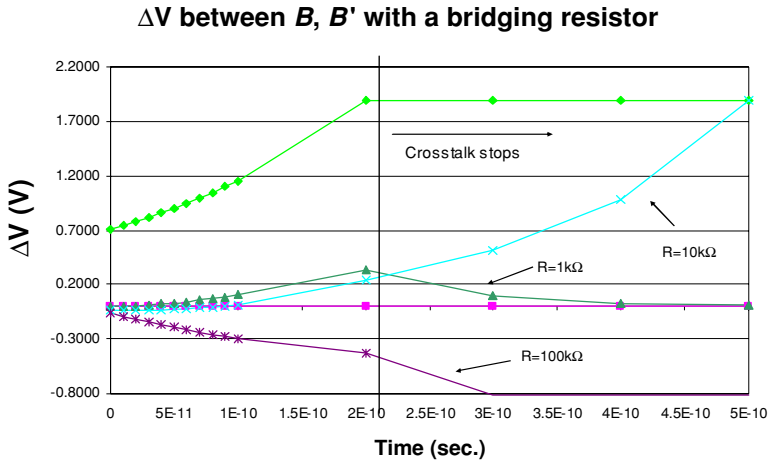
In the case where the short is between a bit-line and any of the power rails, the read operation will depend on the value of the shorting resistance. For resistance values less than 10 kΩ, the short is equivalent to a stuck-at fault. For values between 10 kΩ and 100 kΩ, the faults are neighborhood pattern sensitive. For example, we observe CRFs when the data pattern is 111 and the resistive short is 100 kΩ regardless whether the short is to V_{dd} or Gnd. For the same resistance, CRFs are only observed for the pattern 000 when the short is to V_{dd}. If the resistance is greater than 100 kΩ, there is not enough effect on the circuit's performance to create a fault.

5. Proposed Test Scheme

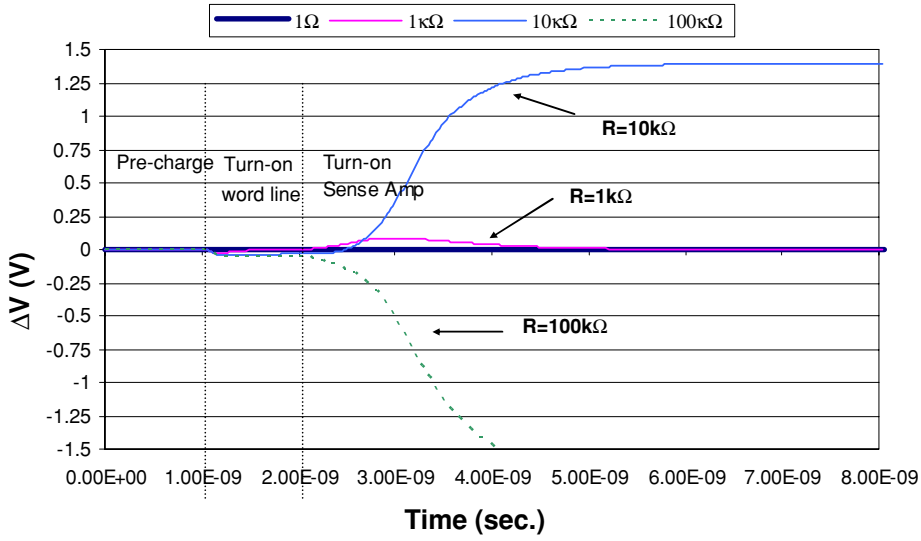
The analytical and simulation results discussed above have given us insight on how to detect CRFs that were described in Section 2.2. This class of faults is detected by what we defined as worst case patterns among the neighborhood bit-lines. As mentioned before, worst case patterns are those in which every bit-line has its two neighbor bit-lines to swing to opposite directions. These patterns are dependent on the DRAM core cell arrangement. For the design shown in Fig. 1, the worst case patterns are "all 0" and "all 1", For more elaborate arrangement such as the one shown in Fig. 8, the worse patterns are not as easily developed, for this reason, we will consider later in this section, patterns for any arrangement.

Often the exact physical layout of the DRAM block is not the same as the logical arrangement. Bit-lines that appear to be immediate neighbors on a logical schematic may not be neighbors in the physical layout. Hence, the logical design is not sufficient to derive the worst case patterns. In addition, most vendors do not divulge the exact physical layout. If we have no knowledge of the internal cell and array arrangement, it is difficult to determine a fixed pattern that will detect the class of CRFs. Without knowing the exact physical layout of the RAM cells, an exhaustive test set may seem like the only way to cover all possibilities of the physical layout. However, the most likely scenario is that crosstalk will be induced by close neighbors. Hence, we can anticipate "local worst pattern cases" by confining the observed neighborhood to 3 or at most 5 pairs. In such cases, the complexity of test pattern generation can be reduced. This scenario is similar to the known K-coupling-fault problem [20]. In this study, we used two values of K: 3 and 5. Without knowledge of the layout, we need to try 2^k data patterns for any group of k bit-line pairs in a memory block.

Typically, the total number of bit-lines in a block ranges from 1024 to 4096, depending on the physical design of the memory block. Theoretically, the 2^k data patterns only need to be applied to any k ($k = 3$, or 5) bit-lines chosen from all of the bit-lines in the block. However the test algorithm



(a)



(b)

Fig. 7. Voltage difference between B_i and B_i' with the existence of various bridging resistors (a) Analytic Results, (b) Simulation Results.

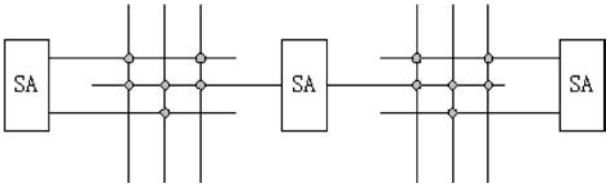


Fig. 8. Examples of Cell Arrangement $6F^2$ mixed bit-line structure [9].

needs to be generic so it can not add any constraints to the physical design. Therefore, we will extend the test to all bit-lines within a memory bank and to each bank in a multi-bank structure. The number of the bit-line pairs in a memory bank is denoted as M and equals 2^X where X is the number of row address bits in the chip. The total number of cells in a memory chip is usually denoted as N and equals 2^{X+Y} where Y is the number of column address bits. In a shared I/O architecture memory chip, X is approximately equal to Y so $M^2 \approx N$. It is very important to note this approximate relationship in calculating the complexity of the test.

The test proposed in this paper contains two parts. The first part uses the "global worst case" pattern where every bit-line in a block switches in the opposite direction from its immediate neighbors, assuming the logical groupings match the physical ones. This "global worst case" pattern is more ad hoc in nature and is not mathematically complete. However, it should work for the memories with the $8F^2$ cell arrangements shown in Fig. 1. The second part of the test is to exhaust the 2^k possible data patterns amongst any k bit-line pairs in each memory bank. Both parts are included in the following algorithms.

1. Test for CRF faults for $K = 3$:

```
// Best try for global worst case patterns
Write/Read All 0s
Write/Read All 1s
Write/Read All 01s
Write/Read All 10s

//exhaust all eight patterns among any three chosen bit lines in a memory bank
// March 1 (1→00000000...) Guarantee 000, 100, 010, 001 state among any 3 bit-lines
Write all 0 background          //(write 000000000.....)
For I=1,M
Read I=0
Write I=1
Read I=1
Write I=0
End

// March 0 (0→11111111...) Guarantee 111, 101, 011, 110 state among any 3 bit-lines
Write all 1 background          // (write 11111111.....)
For I=1,M
Read I=1
Write I=0
Read I=0
Write I=1
End
```

With this test, we guarantee that every three bit-lines will exercise all 8 patterns. The complexity of the test set is 18 M where M is the total number of bit lines in a memory bank.

2. Test for CRF faults for $K = 5$:

A more stringent test set would include the neighborhood of 5 ($K = 5$). Following the same methodology, we need to exhaust 2^5 (32) states among any five chosen bit lines in a memory block. Since we don't add any constraint to the physical arrangement of the memory block, the complexity of increases drastically. In addition to the All "0", "1" and March test, a test is developed to exhaust the $K = 5$ CRF faults, whose complexity of $O(M^2)$, where M is the number of bit-line pairs. The algorithm for this test is shown below.

6. Summary and Conclusion

This paper presents a novel approach to study the effect that crosstalk has on the DRAM read operation. It describes how crosstalk among long bit-lines of a DRAM may cause reading faults in the presence of parameter variations and manufacturing defects. This class of faults is referred to as crosstalk reading faults (*CRFs*). Analytical expressions are derived for the behavior of the SA operation that helped predict the occurrence of these faults. The analytical study is then confirmed with extensive simulation studies.

The study is conducted using the arrangement of the DRAM plane shown in Fig. 1. The SAs and their corresponding bit-lines are represented by their equivalent circuit in Fig. 5. The model includes all the RAM cells in the plane

```
// Best try for global worst case patterns
Write/Read All 0s
Write/Read All 1s
Write/Read All 01s
Write/Read All 10s

//exhaust all thirty two patterns among any five chosen bit-lines in a memory bank
    //Write all 0 background              (write 000000000.....)
    //March 1 (1→00000000...);
                                          //Guarantee 00001, 00010, 00100, 01000, 10000 states among any 5
                                          //bit-lines of the M bit-lines in the block
    Write all 0 background                // (write 000000000.....)
    For I=1, M
            Read I=0                      // Guarantee 00011, 00101, 01001, 10001, 00110, 01010
            Write I=1                     // 10010, 01100, 10100, 11000 states among any 5 bit-lines
            Read I=1                      // of the M bit-lines in the block
                    For J=I+1, M
                            Read J=0
                            Write J=1
                            Read J=1
                            Write J=0
```

```
                End
            Write I=0
            Read I=0
End
//Write all 1 background (write 11111111.....)          // Guarantee 11110, 11101,11011, 10111, 01111
//March 0 (0→11111111...);                              // Guarantee 11110, 11101,11011, 10111, 01111
Write all 1 background (write 111111111.....) // states among any 5 bit-lines of the M bit-lines in the block
For I=1, M                                    // Guarantee 11100, 11010, 10110, 01110, 11001, 10101,
        Read I=1                                        // 01101, 10011, 01011, 00111 states among any 5 bit-lines
        Write I=0                                       // of the M bit-lines in the block
        Read I=0
                For J=I+1, M
                        Read J=1
                        Write J=0
                        Read J=0
                        Write J=1
                End
        Write I=1
        Read I=1
End
```

but the read operation only involved one word-line. Defects are evaluated that affect the capacitance and resistance of the bit-lines, with an emphasis on the two main origins of coupling capacitance: between the bit-lines connected to the same SA and between the bit-lines belonging to different SAs. In addition, the effect of the capacitance to ground and bridging faults between the bit-lines are examined. For all the mentioned cases, CRFs are shown to be a subset of *NPS* and the worst case patterns are ascertained. Generating the worst case patterns is not difficult if the physical layout of the DRAM plane is known, otherwise an exhaustive test is needed. To limit the complexity of test pattern generation, pseudo-exhaustive test sets are applied that detect the faults that are most likely to occur within a realistic neighborhood with a size of three and five pairs of bit-lines. Two algorithms are developed for test generation based on these guidelines. The complexities of the algorithms are 18 M and O(M^2), where M is the number of bit-lines pairs and $M^2 \approx N$, the number of individual bits.

The strength of this paper is in relating the analytical study to the simulation results, and the development of a practical tests to detect *CRFs*. We expect that as the size of technology feature size decreases, the same test pattern generation should still apply. However, further study is needed to explore the possibility of other problems that may be caused by the smaller feature sizes.

Appendix I

Derivation of ΔV Across the Sense Amplifier

We start with the equations given in Section 3 in conjunction with Fig. 5:

$$G_{P1}\left(V_2^i - V_{DD}\right) = G_{N1}V_2^i + C_1\frac{dV_1^i}{dt} + C_C\frac{d}{dt}\left(V_1^i - V_2^i\right) - C_{d1}\frac{d}{dt}\left(V_2^{(i-1)} - V_1^i\right) \quad \text{(I.1)}$$

$$G_{P2}\left(V_1^i - V_{DD}\right) = G_{N2}V_1^i + C_2\frac{dV_2^i}{dt} - C_C\frac{d}{dt}\left(V_1^i - V_2^i\right) + C_{d2}\frac{d}{dt}\left(V_2^i - V_1^{(i+1)}\right) \quad \text{(I.2)}$$

where, the notation $(i-1)$ and $(i+1)$ refer to the pairs on each side of pair i of bit-lines. To simplify the notation, we will ignore the sub-note "i" and only use V_1, V_2 to denote the voltage at the center pair. Obviously, there are four variables in the two differential equation groups if $V_2^{(i-1)}$ and $V_1^{(i+1)}$ are treated as index parameters. To simplify the problem, $\frac{d}{dt}V_2^{(i-1)}$ and $\frac{d}{dt}V_1^{(i+1)}$ are treated as driving forces and denoted as $f_1(t)$ and $f_2(t)$, and are therefore decoupled from Eqs. (I.1) and (I.2).

$$G_{P1}V_2 - G_{P1}V_{DD} = G_{N1}V_2 + C_1V_1' + C_CV_1' - C_CV_2' + C_{d1}V_1' - C_{d1}f_1(t) \quad \text{(I.3)}$$

$$G_{P2}V_1 - G_{P2}V_{DD} = G_{N2}V_1 + C_2V_2' - C_CV_1' + C_CV_2' + C_{d2}V_2' - C_{d2}f_2(t) \quad \text{(I.4)}$$

Rearrange (I.3) and (I.4),

$$(C_1 + C_C + C_{d1})V_1' = C_CV_2' + (G_{P1} - G_{N1})V_2' - G_{P1}V_{DD} + C_{d1}f_1(t) \quad \text{(I.5)}$$

$$(C_2 + C_C + C_{d2})V_2' = C_CV_1' + (G_{P2} - G_{N2})V_1' - G_{P2}V_{DD} + C_{d2}f_2(t) \quad \text{(I.6)}$$

Take derivative on (I.5) and (I.6),

$$(C_1 + C_C + C_{d1})V_1'' = C_CV_2'' + (G_{P1} - G_{N1})V_2' + C_{d1}f_1'(t) \quad \text{(I.7)}$$

$$(C_2 + C_C + C_{d2})V_2'' = C_C V_1'' + (G_{P2} - G_{N2})V_1' + C_{d2} f_2'(t) \tag{I.8}$$

Using (I.5), (I.6), (I.7) and (I.8), we can separate the variables to form the equations

$$\begin{aligned}&(C_1C_2 + C_1C_C + C_1C_{d1} + C_CC_2 + C_CC_{d2} + C_2C_{d1}\\&+C_CC_{d1} + C_{d1}C_{d2})V_1'' = C_C(G_{P1} - G_{N1}. + G_{P2} - G_{N2})V_1'\\&+(G_{P1} - G_{N1})(G_{P2} - G_{N2})V_1'\\&-G_{P1}(G_{P2} - G_{N2})V_{DD} + C_{d1}(C_2 + C_C\\&+C_{d2})f_1'(t) + C_{d2}(G_{P1} - G_{N1})f_2(t)\\&+C_CC_{d2}f_2'(t)\end{aligned} \tag{I.9}$$

$$\begin{aligned}&(C_1C_2 + C_1C_C + C_1C_{d1} + C_CC_2 + C_CC_{d2} + C_2C_{d1}\\&+C_CC_{d1} + C_{d1}C_{d2})V_2'' = C_C(G_{P1} - G_{N1} + G_{P2} - G_{N2})V_2''\\&+(G_{P1} - G_{N1})(G_{P2} - G_{N2})V_2 - G_{P1}(G_{P2}\\&-G_{N2})V_{DD} + C_{d1}(G_{P2} - G_{N2})f_1(t)\\&+C_CC_{d1}f_1'(t) + C_{d2}(C_1 + C_C + C_{d1})f_2'(t)\end{aligned} \tag{I.10}$$

By assigning simplification notations $A = (C_1C_2 + C_1C_C + C_1C_{d1} + C_CC_2 + C_CC_{d2} + C_2C_{d1} + C_CC_{d1} + C_{d1}C_{d2})$, $B = -C_C(G_{P1} - G_{N1} + G_{P2} - G_{N2})$ and $C = -(G_{P1} - G_{N1})(G_{P2} - G_{N2})$, Eqs. (I.9) and (I.10) can be simplified as

$$\begin{aligned}AV_1'' &+BV_1' + CV_1 = -G_{P2}(G_{P1} - G_{N1})V_{DD}\\&+(C_2 + C_C + C_{d2})C_{d1}f_1'(t) + C_{d2}(G_{P1}\\&-G_{N1})f_2(t) + C_CC_{d2}f_2'(t)\end{aligned} \tag{I.11}$$

$$\begin{aligned}AV_2'' &+BV_2' + CV_2 = -G_{P1}(G_{P2} - G_{N2})V_{DD}\\&+C_{d1}(G_{P2} - G_{N2})f_1(t) + C_CC_{d1}f_1'(t)\\&+(C_1 + C_C + C_{d1})C_{d2}f_2'(t)\end{aligned} \tag{I.12}$$

Note that the homogenous part of the these two equations are the same,

$$AV_i'' + BV_i' + CV_i = 0 \tag{I.13}$$

Subtracting (I.11) from (I.12) and define $V_1 - V_2 = \Delta V$ produces:

$$\begin{aligned}A\Delta V'' &+B\Delta V' + C\Delta V = (G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}\\&+C_{d1}(G_{N2} - G_{P2})f_1(t) + (C_2C_{d1}\\&+C_{d1}C_{d2})f_1'(t) - C_{d2}(G_{N1} - G_{P1})f_2(t)\\&-(C_1C_{d2} + C_{d1}C_{d2})f_2'(t)\end{aligned} \tag{I.14}$$

The generic solution of this equation is

$$\Delta V = \Delta V^+ e^{\lambda_1 t} + \Delta V^- e^{\lambda_2 t} \tag{I.15}$$

Here $\lambda_1 = \frac{-B+\sqrt{B^2-4AC}}{2A}$, $\lambda_2 = \frac{-B-\sqrt{B^2-4AC}}{2A}$ and ΔV^+, ΔV^- are constants that can be determined by the initial conditions of ΔV and $\Delta V'$. The explicit form of $\Delta V^+, \Delta V^-$ can also be expressed by the initial values of V_1 and V_2, but only if we solve the state equations in the frequency domain and transfer them back to the time domain. In a normal latch design that is close to its metastable state, there exists $G_N > G_P$, which means $A>0$, $B>0$ and $C<0$. This yields $\lambda_1>0$ and $\lambda_2<0$, so that the first exponential term will increase with time while the second term decays with time. If $G_{N1} = G_{N2}$ and $G_{P1} = G_{P2}$, then the DC term becomes zero. Without the coupling capacitance C_d, the driving terms will diminish as well. Under that condition, the latch stays in its metastable state.

Next we will include the coupling terms through the use of the definitions $f_1(t) = \frac{d}{dt}V_2^{(i-1)}$ and $f_2(t) = \frac{d}{dt}V_1^{(i+1)}$. Taking a first order approximation and using the generic solution as the expression of $V_2^{(i-1)}$ and $V_1^{(i+1)}$, the two driving force terms can be expressed as $f_1(t) = \lambda_1^{(i-1)}V_2^{+(i-1)}e^{\lambda_1^{(i-1)}t} + \lambda_2^{(i-1)}V_2^{-(i-1)}e^{\lambda_2^{(i-1)}t}$ and $f_2(t) = \lambda_1^{(i+1)}V_1^{+(i+1)}e^{\lambda_1^{(i+1)}t} + \lambda_2^{(i+1)}V_1^{-(i+1)}e^{\lambda_2^{(i+1)}t}$. By ignoring the decaying term, the driving terms can be further simplified as $f_1(t) = \lambda_1^{(i-1)}V_2^{+(i-1)}e^{\lambda_1^{(i-1)}t}$ and $f_2(t) = \lambda_1^{(i+1)}V_1^{+(i+1)}e^{\lambda_1^{(i+1)}t}$. Substitute this result into Eq. (I.14), to get:

$$\begin{aligned}&A\Delta V'' + B\Delta V' + C\Delta V = (G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}\\&+C_{d1}(G_{N2} - G_{P2})\lambda_1^{(i-1)}V_2^{+(i-1)}e^{\lambda_1^{(i-1)}t}\\&+(C_2C_{d1} + C_{d1}C_{d2})(\lambda_1^{(i-1)})^2V_2^{+(i-1)}e^{\lambda_1^{(i-1)}t}\\&-C_{d2}(G_{N1} - G_{P1})\lambda_1^{(i+1)}V_1^{+(i+1)}e^{\lambda_1^{(i+1)}t}\\&-(C_1C_{d2} + C_{d1}C_{d2})(\lambda_1^{(i+1)})^2V_1^{+(i+1)}e^{\lambda_1^{(i+1)}t}\end{aligned} \tag{I.16}$$

The solution of Eq. I.16 is a fault-free DRAM circuit and is different from a circuit with parameter fluctuations or defects from the manufacturing process. In a defect-free circuit, group (a), (b) and (c) have identical physical parameters and therefore $\lambda_1^{(i-1)} = \lambda_1^{(i+1)} = \lambda_1$. Define $f(D) = AD^2 + BD + C$, where λ_1 one solution of the characteristic equation and setting is $f(\lambda_1) = 0$, $f'(\lambda_1) = \sqrt{B^2 - 4AC}$. Therefore, the specific solution of $e^{\lambda_i t}$ can be obtained from the following equation.

$$\frac{1}{f(D)}e^{\lambda_1 t} = \frac{t}{f'(\lambda_1)}e^{\lambda_1 t} = \frac{t}{\sqrt{B^2 - 4AC}}e^{\lambda_1 t}$$

Thus the general solution of the Eq. (I.16) is,

$$\begin{aligned}\Delta V = {} & \Delta V^{+}e^{\lambda_1 t} + \Delta V^{-}e^{\lambda_2 t} \\ & -\frac{(G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}}{(G_{P1} - G_{N1})(G_{P2} - G_{N2})} \\ & +\frac{C_{d1}(G_{N2} - G_{P2})}{\sqrt{B^2 - 4AC}}\lambda_1 V_2^{+(i-1)} t e^{\lambda_1 t} \\ & +\frac{C_2 C_{d1} + C_{d1}C_{d2}}{\sqrt{B^2 - 4AC}}(\lambda_1)^2 V_2^{+(i-1)} t e^{\lambda_1 t} \\ & -\frac{C_{d2}(G_{N1} - G_{P1})}{\sqrt{B^2 - 4AC}}\lambda_1 V_1^{+(i+1)} t e^{\lambda_1 t} \\ & -\frac{(C_1 C_{d2} + C_{d1}C_{d2})}{\sqrt{B^2 - 4AC}}(\lambda_1)^2 V_1^{+(i+1)} t e^{\lambda_1 t} \quad \text{(I.17)}\end{aligned}$$

If due to process fluctuation, the electrical parameters of one group (say group i) is different from other groups, the timing of this group of SA and bit-line will be different from the rest of the array. Thus the characteristic equation and solution will be different from these neighborhood groups (the normal ones). Then the solutions of the characteristic equation will be different as well. As a result, λ_i is different from $\lambda_i^{(i-1)}$, $\lambda_i^{(i+1)}$. Therefore, the solution of Eq. 16 is in a different form since $f(\lambda_{io}) \neq 0$. Namely, $A\lambda_{io}^2 + B\lambda_{io} + C \neq 0$ where λ_{io} is the solution of a normal characteristic equation (such as $\lambda_i^{(i-1)}$, $\lambda_i^{(i+1)}$). A, B, C from the group are also different from their normal values. Thus, the specific solution of the exponential driving term is

$$\frac{1}{f(D)}e^{\lambda_1 t} = \frac{1}{f(\lambda_i)}e^{\lambda_1 t}$$

Thus the general solution is

$$\begin{aligned}\Delta V = {} & \Delta V^{+}e^{\lambda_1 t} + \Delta V^{-}e^{\lambda_2 t} \\ & -\frac{(G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}}{(G_{P1} - G_{N1})(G_{P2} - G_{N2})} \\ & +\frac{C_{d1}(G_{N2} - G_{P2})}{A\lambda_1^{(i-1)^2} + B\lambda_1^{(i-1)} + C}\lambda_1^{(i-1)} V_2^{+(i-1)} e^{\lambda_1^{(i-1)} t} \\ & +\frac{(C_2 C_{d1} + C_{d1}C_{d2})}{A\lambda_1^{(i-1)^2} + B\lambda_1^{(i-1)} + C}\left(\lambda_1^{(i-1)}\right)^2 V_2^{+(i-1)} e^{\lambda_1^{(i-1)} t} \\ & -\frac{C_{d2}(G_{N1} - G_{P1})}{A\lambda_1^{(i+1)^2} + B\lambda_1^{(i+1)} + C}\lambda_1^{(i+1)} V_1^{+(i+1)} e^{\lambda_1^{(i+1)} t} \\ & -\frac{(C_1 C_{d2} + C_{d1}C_{d2})}{A\lambda_1^{(i+1)^2} + B\lambda_1^{(i+1)} + C}\left(\lambda_1^{(i+1)}\right)^2 V_1^{+(i+1)} e^{\lambda_1^{(i+1)} t} \quad \text{(I.18)}\end{aligned}$$

Appendix II

Derivation of ΔV Across the Sense Amplifier

For the Case of Shorted Bit-lines

Adding the bridging resistor with conductance G between bit-line 1 and its complemented, bit-line 2, the current conservation equations are modified to be:

$$\begin{aligned}G_{P1}(V_2 - V_{DD}) = {} & G_{N1}V_2 + C_1\frac{dV_1}{dt} + C_C\frac{d}{dt}(V_1 - V_2) \\ & +G(V_1 - V_2) - C_{d1}\frac{d}{dt}\left(V_2^{(i-1)} - V_1\right) \quad \text{(II.1)}\end{aligned}$$

$$\begin{aligned}G_{P2}(V_1 - V_{DD}) = {} & G_{N2}V_1 + C_2\frac{dV_2}{dt} - C_C\frac{d}{dt}(V_1 - V_2) \\ & -G(V_1 - V_2) + C_{d2}\frac{d}{dt}\left(V_2 - V_1^{(i+1)}\right) \quad \text{(II.2)}\end{aligned}$$

Similarly the following equations can be obtained by elimination:

$$\begin{aligned}& (C_1C_2 + C_1C_C + C_1C_{d1} + C_CC_2 + C_CC_{d2} + C_2C_{d1} \\ & +C_CC_{d1} + C_{d1}C_{d2})V_1'' = C_C(G_{P1} - G_{N1} \\ & +G_{P2} - G_{N2})V_1' + (G_{P1} - G_{N1})(G_{P2} - G_{N2})V_1 \\ & -(C_2 + C_{d2})G(V_1' - V_2') + (G_{P1} - G_{N1}) \\ & \times G(V_1 - V_2) - G_{P1}(G_{P2} - G_{N2})V_{DD} \\ & +C_{d1}(C_2 + C_C + C_{d2})f_1'(t) \\ & +C_{d2}(G_{P1} - G_{N1})f_2(t) + C_CC_{d2}f_2'(t) \quad \text{(II.3)}\end{aligned}$$

$$\begin{aligned}& (C_1C_2 + C_1C_C + C_1C_{d1} + C_CC_2 + C_CC_{d2} + C_2C_{d1} \\ & +C_CC_{d1} + C_{d1}C_{d2})V_2'' \\ & = C_C(G_{P1} - G_{N1} + G_{P2} - G_{N2})V_2' \\ & +(G_{P1} - G_{N1})(G_{P2} - G_{N2})V_2 \\ & +(C_1 + C_{d1})G(V_1' - V_2') - (G_{P2} - G_{N2}) \\ & G(V_1 - V_2) - G_{P1}(G_{P2} - G_{N2})V_{DD} \\ & +C_{d1}(G_{P2} - G_{N2})f_1(t) + C_CC_{d1}f_1'(t) \\ & +C_{d2}(C_1 + C_C + C_{d1})f_2'(t) \quad \text{(II.4)}\end{aligned}$$

Subtracting (3) from (4) and using the same simplification parameters A, B, C, we get (II.5)

$$\begin{aligned}& A\Delta V'' + [B + G(C_1 + C_2 + C_{d1} + C_{d2})]\Delta V' \\ & +[C + (G_{N1} - G_{P1} + G_{N2} - G_{P2})G]\Delta V\end{aligned}$$

$$= (G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD} + C_{d1}(G_{N2} - G_{P2})f_1(t) + (C_2C_{d1} + C_{d1}C_{d2})f_1'(t) - C_{d2}(G_{N1} - G_{P1})f_2(t) - (C_1C_{d2} + C_{d1}C_{d2})f_2'(t) \quad \text{(II.5)}$$

Assign $B\prime = [B + G(C_1 + C_2 + C_{d1} + C_{d2})]$, $C\prime = [C + (G_{N1} - G_{P1} + G_{N2} - G_{P2})G]$ and substituting the expressions for f_1 and f_2 from Appendix I, we get:

$$\begin{aligned} A\Delta V'' + B'\Delta V' + C'\Delta V &= (G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD} \\ &+ C_{d1}(G_{N2} - G_{P2})\lambda_1^{(i-1)}V_2^{+(i-1)}e^{\lambda_1^{(i-1)}t} \\ &+ (C_2C_{d1} + C_{d1}C_{d2})\left(\lambda_1^{(i-1)}\right)^2 V_2^{+(i-1)}e^{\lambda_1^{(i-1)}t} \\ &- C_{d2}(G_{N1} - G_{P1})\lambda_1^{(i+1)}V_1^{+(i+1)}e^{\lambda_1^{(i+1)}t} \\ &- (C_1C_{d2} + C_{d1}C_{d2})\left(\lambda_1^{(i+1)}\right)^2 V_1^{+(i+1)}e^{\lambda_1^{(i+1)}t} \end{aligned} \quad \text{(II.6)}$$

If the characteristics of the lines differ from normal line pairs, the solution is

$$\begin{aligned} \Delta V &= \Delta V^+ e^{\lambda_1 t} + \Delta V^- e^{\lambda_2 t} \\ &- \frac{(G_{N1}G_{P2} - G_{P1}G_{N2})V_{DD}}{(G_{P1} - G_{N1})(G_{P2} - G_{N2})} \\ &+ \frac{C_{d1}(G_{N2} - G_{P2})}{A\lambda_1^{(i-1)^2} + B'\lambda_1^{(i-1)} + C'}\lambda_1^{(i-1)}V_2^{+(i-1)}e^{\lambda_1^{(i+1)}t} \\ &+ \frac{(C_2C_{d1} + C_{d1}C_{d2})}{A\lambda_1^{(i-1)^2} + B'\lambda_1^{(i-1)} + C'}\lambda_1^{(i-1)^2}V_2^{+(i-1)}e^{\lambda_1^{(i+1)}t} \\ &- \frac{C_{d2}(G_{N1} - G_{P1})}{A\lambda_1^{(i+1)^2} + B'\lambda_1^{(i+1)} + C'}\lambda_1^{(i+1)}V_1^{(i+1)}e^{\lambda_1^{(i+1)}t} \\ &- \frac{(C_1C_{d2} + C_{d1}C_{d2})}{A\lambda_1^{(i+1)^2} + B'\lambda_1^{(i+1)} + C'}\lambda_1^{(i+1)^2}V_1^{(i+1)}e^{\lambda_1^{(i+1)}t} \end{aligned} \quad \text{(II.7)}$$

Where $\lambda_1 = \frac{-B'+\sqrt{B'^2-4AC'}}{2A}$, and $\lambda_2 = \frac{-B'-\sqrt{B'^2-4AC'}}{2A}$, and $\lambda_1^{(i-1)}, \lambda_1^{(i+1)} = \frac{-B+\sqrt{B^2-4AC}}{2A}$.

If the bridging resistor has very high resistance namely $G \to 0$, there exist $B' \to B$ and $C' \to C$. Therefore, Eq. (II.7) degrades into Eq. (I.18) of Appendix I. If the resistance is very small, such as 1Ω, the initial voltage difference between bit-lines 1 and 2 is almost zero. More importantly, λ_1 and λ_2 are negative and thus the characteristic terms decay rapidly. The value of ΔV remains zero even in the presence of coupling voltages from the neighborhood bit-lines.

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References

1. R. Anglada and A. Rubio, "An approach to crosstalk effect analysis and avoidance techniques in digital CMOS VLSI circuits," *Int. J. Elect.*, Vol. 65, No. 1.9–17, pp. 9–17, 1988.
2. T. Sakurai, "Closed-Form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSI's," *IEEE Transaction of Electron Devices*, Vol. 40, No. 1, pp. 118–124, 1993.
3. A. Vittal and M. Marek-Sadowska, "Crosstalk Reduction for VLSI," *IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 3, pp. 290–298, 1997.
4. E. Sicard and A. Rubio, "Analysis of Crosstalk Interference in CMOS Integrated Circuits," *IEEE Transaction on Electromagnetic Compactibility*, Vol. 34, No. 2, pp. 124–129, 1992.
5. A. Rubio, N. Itazaki, X. Xu, and K. Kinoshita, "An Approach to the Analysis and Detection of crosstalk Faults in Digital CMOS VLSI circuits," *IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 3, pp. 387–394, 1994.
6. W. Chen, S.K. Gupta, and M.A. Breuer, "Analytical Models for Crosstalk Delay and Pulse Analysis Under Non-Ideal Inputs," *Proceeding of International Test Conference*, 1997, pp. 809–818.
7. Z. Yang and S. Mourad, "Deep Submicron on Chip Crosstalk," *Int'l Measurement and Instrumentation Conf.*, Venice, Italy, pp. 35–42, 1999.
8. Y. Konishi et al. "Analysis of coupling Noise between adjacent bitlines in megabit DRAM's," *IEEE Journal of Solid State Circuits*, Vol. 24, No. 1, pp. 35–42, 1989.
9. D. Takashima et al. "Open/Folded Bitline Arrangement for Ultra-High-Density DRAM's," *IEEE Journal of Solid State Circuits*, Vol. 29, No. 4, April 1994.
10. J. Rabaey, *Digital Integrated Circuits, A Design Perspective*, Prentice-Hall, 1996.
11. Z. Yang and S. Mourad, "Crosstalk in Deep Submicron DRAMs," *Records of IEEE workshop on Memory Technology, Design and Test*, pp. 125–129, 2000.
12. Wilson Tan, etc. "Poly-3 Bitline Crack," 5th *International Symposium on the Physical & Failure Analysis on Integrated Circuits*, pp. 206–211, 1995.
13. Adrian Chan, etc. "Electrical failure analysis in high density DRAMs," in *Records of IEEE workshop on Memory Technology, Design and Test*, pp. 26–31, 1994.
14. C. Lee, etc. "Analysis of serious bitline failure on 0.19 μm 64M DRAM with STI technology," in *Proceedings of SPIE*, pp. 92–102, 2000.
15. Chin-Te Kao, etc. "A case study of failure analysis and guardband determination for a 64M-bit DRAM," in *9*th *Asian Test Symposium*, pp. 447–451, 2000.
16. J.P. Hayes, etc. "Detection of pattern-sensitive faults in random access memory," *IEEE Trans. Comput.*, Vol. C_34, pp. 150–157, 1975.
17. Dong S. Suk, etc. "Test Procedures for a class of pattern sensitive faults in semiconductor random access memories," *IEEE Trans. Comput.*, Vol. C-29, pp. 419–429, June 1980.
18. B.F. Cockburn, "Deterministic tests for detecting single V-coupling faults in RAMs," *Journal of electronic testing: Theory and Applications*, Vol. 5, pp. 91–113, 1994.
19. Ad. J. van de Goor, *Testing Semiconductor Memories: Theory and Practice*, Gouda, The Netherlands: COMPTEX Publishing.
20. A.J. van de Goor, etc. "Converting March tests for bit-Oriented memories into Tests for word-oriented," *Records of IEEE workshop on Memory Technology, Design and Test*, pp. 46–52, 1998.
21. Ad. J. van de Goor and Zaid Al-Ars, "Functional Memory Faults: A Formal Notation and a Taxonomy,", *Proceedings of 18*th *IEEE VLSI Test Symposium*, pp. 281–289, 2000.
22. Zaid Al-Ars and Ad. J. van de Goor, "Transient faults in DRAMs: Concept, analysis and impact on tests," *Records of IEEE workshop on Memory Technology, Design and Test*, pp. 59–64, 2000.

23. Said Hamdioui, Zaid Al-Ars, and Ad J. van de Goor, "Testing Static and Dynamic Faults in Random Access Memories" *Proc. IEEE VLSI Test Symp*., pp. 395–400, 2002.
24. S. Flannagan, "Synchronization Reliability in CMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. SC-20, No. 4, pp. 880–882, Aug. 1985.
25. Mary Sue Haydt and Samiha Mourad, "The Effect Of Feedback Characteristics On Metastability In CMOS Latches," *Symposium on Microelectronic Manufacturing*, pp. 56–61, Sep. 2000.
26. Shahdad Irajpour, etc. "Analyzing Crosstalk in the Presence of Week Bridge Defects," *Proc. IEEE VLSI Test Symp*, pp. 385–392, 2003.

Zemo Yang is a senior engineering manager in S3 Graphics Inc. in Fremont, California. He has fifteen years of experience in electrical modeling and signal integrity analysis, IC packaging, high-speed module design, and IC product and test engineering. Zemo received his M.S. degrees in physics and electrical engineering from the University of Arizona in 1988 and 1991 respectively. He is currently PhD candidate at Santa Clara University.

Samiha Mourad is the William and Janice Terry Professor of Engineering at Santa Clara University where she chairs the Electrical Engineering Department and conducts research in ASIC Design and Testing. Prior to joining Santa Clara University, she spent several years as a research associate at the Center for Reliable Computing of Stanford University. She has authored and coauthored over 100 conference and journal papers, and three books. Her latest book, Principles of Testing Digital Systems, was published by Wiley and Sons in 2000.