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# Memristive computing devices and applications

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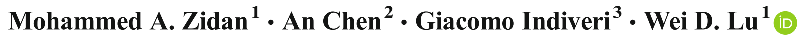

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**Abstract** Advances in electronics have revolutionized the way people work, play and communicate with each other. Historically, these advances were mainly driven by CMOS transistor scaling following Moore's law, where new generations of devices are smaller, faster, and cheaper, leading to more powerful circuits and systems. However, conventional scaling is now facing major technical challenges and fundamental limits. New materials, devices, and architectures are being aggressively pursued to meet present and future computing needs, where tight integration of memory and logic, and parallel processing are highly desired. To this end, one class of emerging devices, termed memristors or memristive devices, have attracted broad interest as a promising candidate for future memory and computing applications. Besides tremendous appeal in data storage applications, memristors offer the potential to enable efficient hardware realization of neuromorphic and analog computing architectures that differ radically from conventional von Neumann computing architectures. In this review, we analyze representative memristor devices and their applications including mixed signal analog-digital neuromorphic computing architectures, and highlight the potential and challenges of applying such devices and architectures in different computing applications.

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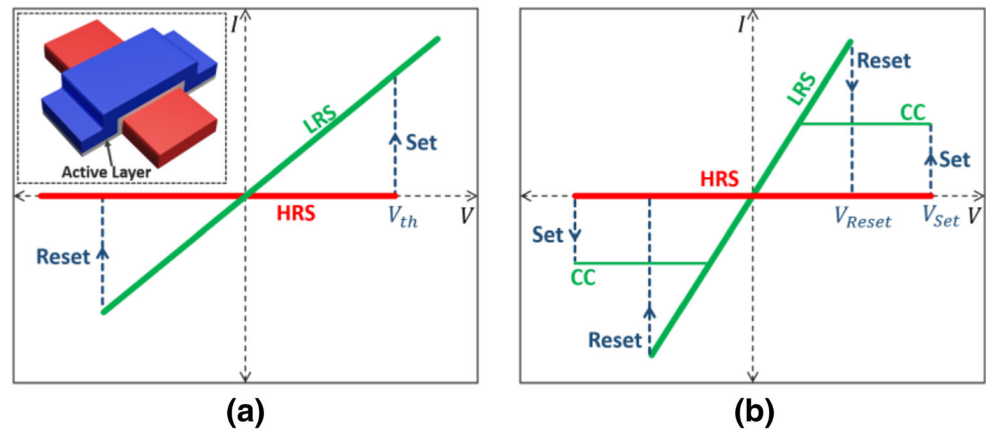
## 1 Introduction

As we approach the end of a computing era, the search for futuristic alternatives is on high gear. Historically, computers steadily achieve better performance over time through Moore's law scaling of the basic logic device – silicon transistor. However, continued performance gains through simple device scaling can no longer be sustained after hitting the heat wall and the memory wall in the early 2000s, while transistor scaling itself will also soon reach fundamental physical limits [1–4]. Moreover, current computers are not optimized for many of today's applications which typically involve large amounts of and demand high throughput and/or low power. To fulfill these new demands, the development of new driving technologies at the device level and new computing paradigms at the system level needs to occur concurrently. In recent years, an emerging class of devices, termed memristors (memristive devices), have gained strong interest as a promising candidate for future data storage and efficient parallel computing paradigms [5–9]. At the device level, memristor-based memories and logic circuits have already shown great potential to help extend the lifetime of classical computing architectures [6, 10]. At the system level, a new class of analog/digital neuromorphic architectures has emerged [9, 11–13], which can exploit the physics of such resistive devices to directly and naturally implement brain-inspired computing paradigms [5, 14–16], making them extremely attractive for efficient computing systems that can attack data-intensive tasks in both the near term and the long term.

Memristors are two-terminal devices that store their state in the form of different values of resistance (Fig. 1(a)) [17, 18].



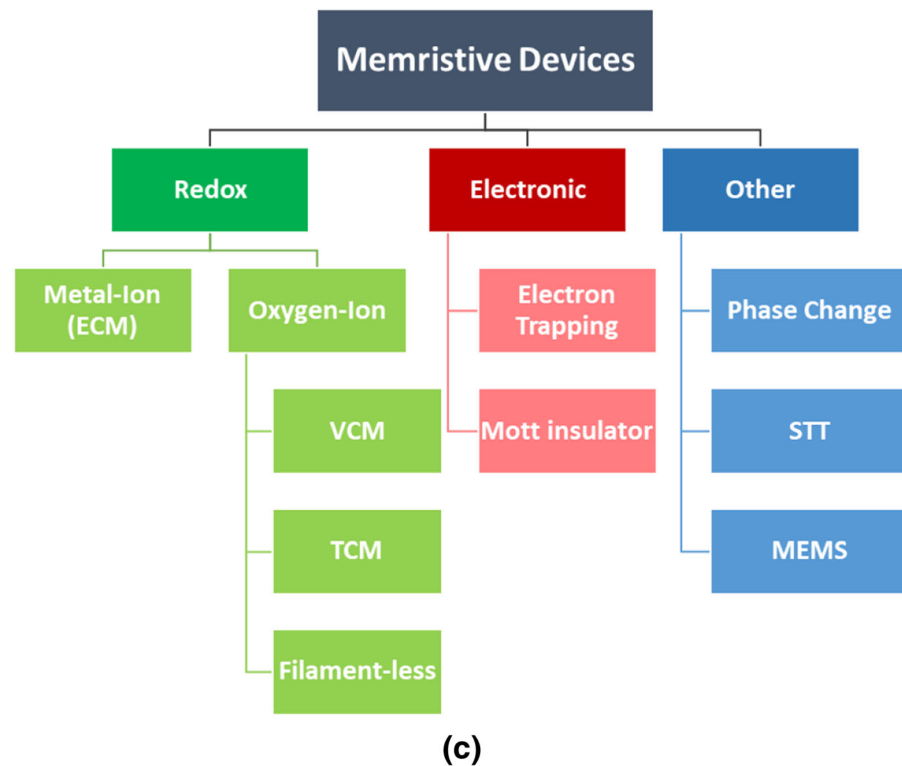




**Fig. 1** (**a**) Bipolar switching behavior of a memristive device. (Inset) Crosspoint structure of the two-terminal device. (**b**) Categories of memristive devices based on the memory effect mechanism

In a typical device, the resistance state can be changed from a high-resistance state (HRS) to a low-resistance state (LRS) when the bias voltage is above a threshold voltage during a so-called SET process. The device will maintain the new resistance value, until it is subjected to a RESET process where the resistance can be switched back to the HRS, and vice versa (Fig. 1(b)). This capability enables such devices to serve as memory elements and simultaneously as (two-terminal) switches. The resistive memory effect has been demonstrated based on different switching mechanisms, as summarized in Fig. 1(c). Specifically, redox devices rely on an oxidation/reduction mechanism of ionic species to change the local chemical composition and physical properties of the switching layer, typically in the form of creating and annihilation of a conductive filament, leading to reversible changes of local resistivity and overall device resistance [19–21]. Devices based on electronic effects depend on effects such as electron trapping [22] and insulator-metal transition processes in a Mott insulator [23–25]. Phase change (PCM) devices rely on changing the phase, either amorphous (high resistance) or crystalline (low resistance) of the material [26, 27]. Spin torque transfer (STT) devices rely on the switching of the relative magnetic orientation of a spin valve, with parallel orientation leading to LRS and antiparallel orientation leading to HRS [28]. Finally, MEMS-based devices depend on mechanical movements that bring the electrodes closer (LRS) or further apart (HRS) [29]. Each of these devices offers a set of strengths and weakness that may fit specific applications. However, in this review we will focus on redox devices, which has generated intense research interest due to their

generally promising resistive switching properties, CMOS compatibility and their proven ability to integrate within computing systems. PCM devices will also be discussed briefly, since they mostly share the same application domains as redox devices and are technically more mature at the current stage and hence may potentially lead to early applications.

The organization of the review is as follows. We will first introduce the different memristive device technologies (focusing on redox and PCM types), followed by discussions on the role of such new device technologies in classical memory and digital logic systems. Next, we discuss the potential of memristive devices to enable emerging computing approaches, including neural networks, analog computing, and stochastic computing. Each of the considered computing application is assessed based on the required device performance metrics including endurance, variability, nonlinearity, ON/OFF ratio, power consumption, and switching behavior. Finally, we relate the application requirements to what the current device technology can offer. By performing the device- and system-level analysis, the goal is to hopefully provide an insight into the status of the memristor device research and the required future developments to meet the applications challenges.

## 2 Memristive devices based on redox processes

The most widely studied memristive devices are the ones based on redox processes that involve active cation or anion species. A redox device is typically fabricated in a metal-insulator-metal (MIM) structure, where the insulator is a thin dielectric layer (typically a few nanometers thick) within which the resistive switching (RS) takes place. At these nanoscale dimensions the dielectric layer can act as a solid electrolyte system for the ionic species, rather than a conventional insulator [30]. Specifically, even a moderate voltage drop can create a large enough electric field that in turn leads to an exponential speedup effect on the ionic oxidation, migration and reduction processes [30]. With the electrolyte's ability to dissolve and conduct ions it facilitates a series of electrochemical reactions that lead to the oxidation/reduction and migration of the cations or anions, and subsequently a modification of the local chemical compositions of the film and changes of the film's physical properties including its resistance. In most redox devices, the memory effect is driven by the formation and modulation/annihilation of a localized conductive filament, although it RS based on interface effects also have been observed. The two main types of redox-based memristive devices, depending on the nature of the active ionic species (cation or anion), are specifically discussed below.

### 2.1 Metal-ion based devices

The Metal-ion (M-ion) based devices are generally known as Conductive Bridge RAM (CBRAM) or Electrochemical Metallization Cell (ECM). The device structure is asymmetric, with one active metal (typically Ag or Cu) electrode and an inert metal electrode in the MIM structure. Applying a high enough positive voltage to the active electrode oxidizes the metal atoms into ions and subsequently dissolves the metal ions into the thin film electrolyte. Under the applied electric field, the metal ions then migrate through the electrolyte film and finally become reduced into metal atoms that eventually form metallic clusters, schematically shown in Fig. 2(a). These sequential processes lead to the nucleation and continued growth of the (metallic) filament until the two electrodes become connected, and the device resistance abruptly drops to the LRS. This process corresponds to the SET process. Afterward, the filament can be erased by applying a negative voltage to the active electrode, which will reverse the electrochemical processes and lead to the rupture of the filament, corresponding to the RESET process. Figure 2(b) and (c) show transmission electron microscopy (TEM) images verifying the formation of a complete filament after SET and the rupture of the filament after RESET [32].

The dynamic growth of the metallic filament can be affected by the ion mobility ($\mu$) and the redox rate ($\Gamma$), as discussed in Ref. [33]. The expansion and shrinkage of the metal clusters depend on the supply of the ions that facilitates the filament formation. The ions supply, in turn, is determined by the redox rate (oxidation and reduction rates) as well as the speed of the ion migration in the electrolyte (the ion mobility). Different growth modes have been observed experimentally and can be successfully explained by the relative strength of the two dynamic factors ion mobility ($\mu$) and the redox rate ($\Gamma$), as shown in Fig. 3. The values of ($\mu$) and ($\Gamma$) can be tuned by the careful selection of the electrode material and the switching materials, as well as the operating conditions since both of them can be strongly affected by the applied electric field. Typically, Cu and Ag are the materials of choice for the active electrode due to their ability to dissolve in thin film electrolytes at low electric fields and their high ionic mobility [33]. For the solid electrolyte layer, a very wide range of materials have been explored, including oxides [21], chalcogenides [34], and organic materials. Originally, chalcogenides were chosen due to the high diffusivity of the active metal species in these films. However, these devices normally suffer from high programming current and very low RESET voltage (comparable to the thermal voltage) that increases accidental reset error, along with material compatibility issues [35]. As a result, recent studies on CBRAM devices have focused on conventional insulator-based MIM structures that also offer promising device performance.

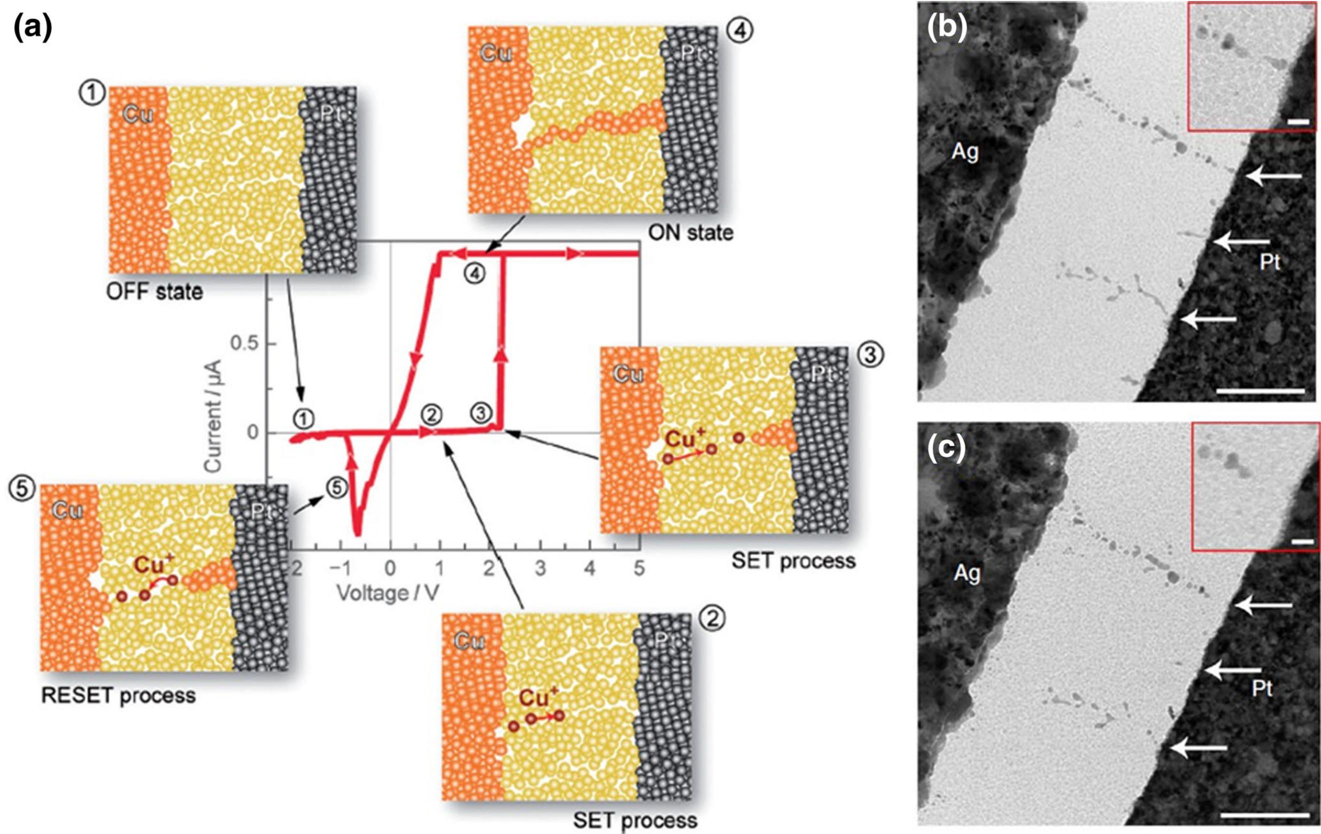



**Fig. 2** (**a**) Stages of filament formation and annihilation in an M-ion device (Ref. [31]). (**b**–**c**) TEM images of a lateral device showing the creation (**b**) and rupture (**c**) of nanoscale filaments (Ref. [32])

M-ion based devices have shown several key strengths including high scalability, fast switching time, low SET and RESET voltage, low current, high ON/OFF, and CMOS compatibility [19, 36–38]. However, device variability and endurance may pose challenges in some applications [38, 39]. The source of the variability is the stochastic nature of the filament creation, where the filament shape and the contact point may not be consistent over switching cycles. A tradeoff has been observed between the switching voltage and the variability based on the electrolyte material selection [35]. The endurance issue originates from the fact that the conductive filament is composed of foreign ionic inclusions from the active metal, which may cause stress to the dielectric film and can eventually lead to permanent plastic deformation if programming conditions are not optimally set

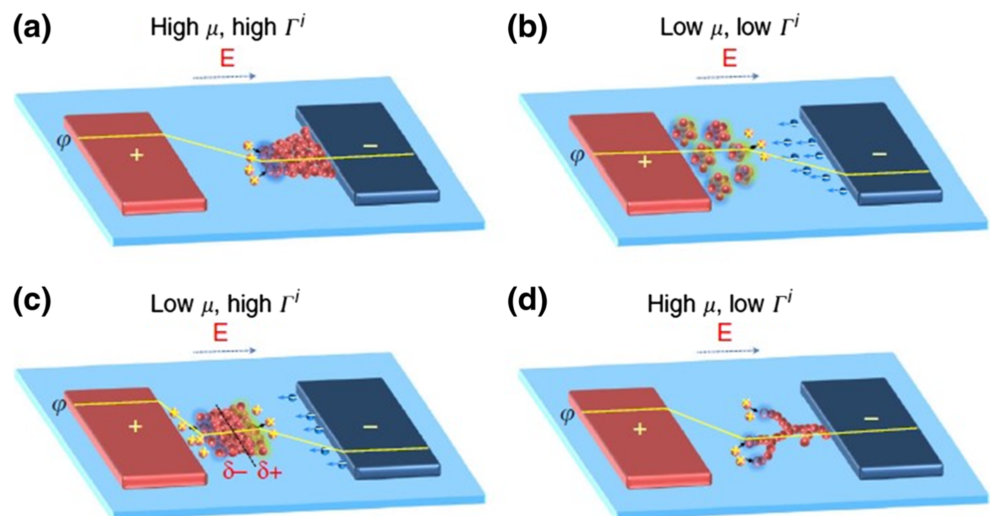



**Fig. 3** Dependence of the filament growth dynamics on the ion mobility ($\mu$) and the redox rate ($\Gamma$). Both parameters are also dependent on the applied electric field (Ref. [33])

[40]. As a result, a typical M-ion based device can reach $10^6$ SET/RESET cycles that are sufficient for data storage, but further improvements of the cycling (e.g. $10^{15}$) to that required for a main memory (e.g. DRAM) will require extensive material and system optimizations. Table 1 summarizes the set of materials used to fabricate M-ion devices and their key features.

### 2.2 Oxygen-ion based devices

Besides metal ions, the redox and migration processes of anions, most commonly oxygen-ions (and subsequently oxygen-vacancies, $V_O$s) are also widely used to build memristive devices. There are three types of oxygen-ion (or oxygen vacancy) based redox devices, the valency change memory (VCM), thermochemical memory (TCM) and filament-less (interface-type) devices. In VCM and TCM, switching relies on the creation and annihilation of an $V_O$-rich filament. While VCM is electric-field driven and exhibits a bipolar electrochemical switching behavior, TCM relies on a thermochemical fusing and anti-fusing process and thus exhibits unipolar switching behavior. Filament-less devices rely on interface effects to modulate a Schottky or tunnel barrier between the switching layer and an electrode. Out of the three oxygen-ion based redox devices, VCM is generally considered as the most promising as TCM devices suffer from higher power consumption needed to create the temperature rise and lower integration density due to thermal interference among neighboring cells, while interface-type devices normally suffer from shorter-retention time. As a result, we will be focusing our discussions on VCM memory here.

In contrast to M-ion devices, oxygen-ion devices, including VCM, normally use inert electrodes and the active species (i.e. oxygen ions) are native to the switching layer, typically a transition metal oxide. Active metals are not employed in VCM memory to avoid metal-ion migration that complicates the programming process. An asymmetry is typically built-in the device, such that one of the oxide/electrode interfaces has high $V_O$ concentration and serves as a reservoir for oxygen vacancies during RS, while the oxide film near the other interface is close to be stoichiometric and thus exhibits high resistance [38]. Under an applied electrical field, oxygen vacancy diffusion from the reservoir layer and associated redox processes can increase the local $V_O$ concentration in the switching layer. These localized oxygen vacancy-rich regions serve as conducting channels (filaments) and can be subsequently reset and set again through applied bias voltages [57]. A forming process may be required to create the initial high-density oxygen vacancy regions for a device in the initial state. Figure 4(a) and (b) show the steps of the conductive filament formation process in a typical VCM, along with TEM evidence of a localized region with substantial oxygen-ion concentration change. After forming, repeated switching can be obtained by modulating the $V_O$ concentration in the filament region. It is also common to fabricate VCM devices using two oxide layers, with one containing higher $V_O$ concentration than

**Table 1** Materials, mechanism, and properties of the Redox and PCM device

| | Electrode 1 | Electrode 2 | Switching layer | Mechanism | Strengths | Weaknesses |
|---|---|---|---|---|---|---|
| M-Ion (ECM) | Active metal (ex: Ag [36], Cu [19]) | Ohmic Contact (metal [34, 36] or polysilicon [19]) | Insulators (ex: $Al_2O_3$ [21], a-Si [41], $SiO_2$ [42], $Ta_2O_5$ [43]), Chalcogenides [34] (eg: GeS [36]), Organic materials [44] | Oxidation and reduction of metal-ions to create/remove a metallic filament | Low Current, Low Voltage, Small feature size, Fast switching, Forming Free, Excellent Retention, High ON/OFF ratio [19, 36–38]. | Lower Endurance ($10^8$), Higher Variability [38, 39] |
| O-Ion (VCM) | Inert metal (ex: Ta [20], Pt [45]) | Ohmic contact [20] | Mainly oxygen deficient oxides (ex: $TaO_x$ [20], $TaO_x$ [46], $TiO_x$ [18], $SrTiO_x$ [47], $AlO_x$ [48]) | Modulation of oxygen-vacancy concentration in a localized filament region | High Endurance ($10^{12}$), Excellent Retention, Small feature size, Fast switching, Analog switching [38, 49–52] | Higher Current and Variability [38, 52] |
| PCM | Ohmic contact | Ohmic contact | Chalcogenides (ex: GST [26, 53], GeTe/$Sb_2Te_3$ [53, 54] & AIST [53]) | Material phase change between amorphous & crystalline states | Unipolar switching, low voltage, multi-level operation, More mature [26, 55] | Unipolar switching, High Current, Lower Endurance ($10^9$), High power consumption, Large feature size [26, 55, 56] |

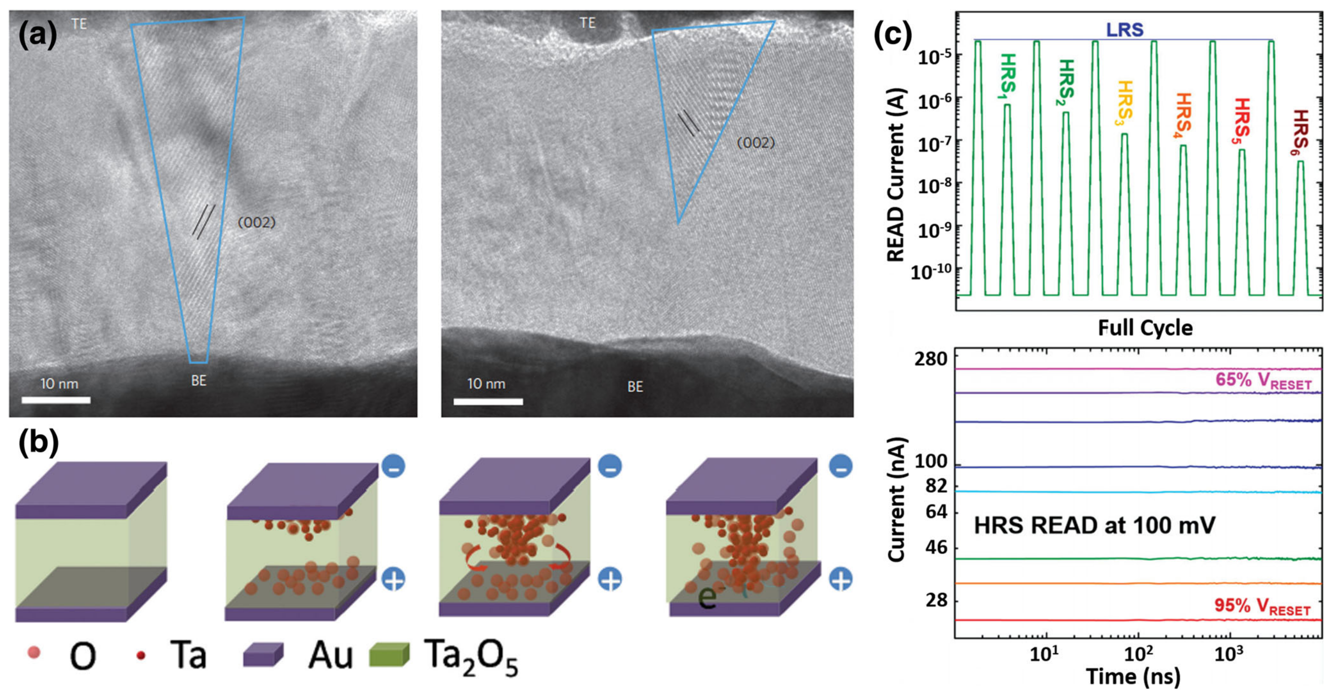



**Fig. 4** (**a**) TEM images showing the creation of a localized region ($Ti_4O_7$) with lower Ti valency in a $TiO_2$ film (Ref. [58]). (**b**) Schematics showing the creation and annihilation of an oxygen vacancy-rich filament (Ref. [59]) (**c**) Multi-level switching for a $SrTiO_3$ device. (Ref. [60])

the other [61]. The filament is created in the low $V_O$ density layer, while the other layer acts as a source for the oxygen vacancies.

Recent progresses in VCM research have led to devices with desirable memory characteristics including excellent scaling, fast switching, and high endurance ($10^{12}$). Additionally, these devices can switch in an analog or multi-level fashion enabling multilevel state representation, as shown in Fig. 4(c). The incremental resistance change is desirable for applications such as neuromorphic computing, as will be discussed later in Section 5.1. However, further development is still needed to improve the device variability and lower the programming current. In particular, considering VCM devices typically show lower on/off (e.g. 10–100) compared to M-ion based devices (> $10^3$) controlling the device variability is particularly important for large-scale applications of VCM. Reducing the programming current to μA or even lower will also further improve the power efficiency of the memory and computing circuits based on VCM devices. Oftentimes, tradeoffs can be made by improving one performance parameter at the expense of others by tuning the programming conditions [62].

## 3 Phase change devices

PCM devices change their resistance based on the microstructural re-arrangement of a chalcogenide layer, being either amorphous or crystalline [55]. The device exhibits high resistance in the amorphous phase, and low resistance in the crystalline one. Several chalcogenide materials have been explored as phase change candidates, where currently GST (Germanium-Antimony-Tellurium) is the most widely used [26, 53]. The state change of the PCM material is normally driven by a thermal process, through melting and fast quenching (during RESET) into the amorphous state, and slow crystalline nucleation and growth (during SET) into the crystalline phase. The basic PCM device structure consists of a phase change layer sandwiched between two metal electrodes, where the electrodes act as Ohmic contacts to the chalcogenide film. Practical PCM devices include a heater layer beneath the phase change material, where localized heating is used to confine the heat transfer that improves the device performance. Nanoscale heaters can be utilized to localized the phase change effect and improve the device energy consumption and scalability [63]. To program a PCM, short, high current pulses RESET the device to the high resistance amorphous phase, while long, low current pulses crystallize the phase change material and reduce its resistance, as shown in Fig. 5. It should be noted here that the crystal state of the chalcogenide layer also affects its reflectivity, a reason why phase change materials are widely utilized by the industry of optical storage media [53].

State-of-the-art PCM devices can switch within 100 ns with a bias of few volts [26]. This is considered an advantage over classical Flash memories. However, PCM consumes more energy per bit compared to Flash and redox based devices [26]. Table 1 compares the performance of PCM with ECM and VCM based redox memories. Considerable efforts and resources have been put in PCM research to improve the device

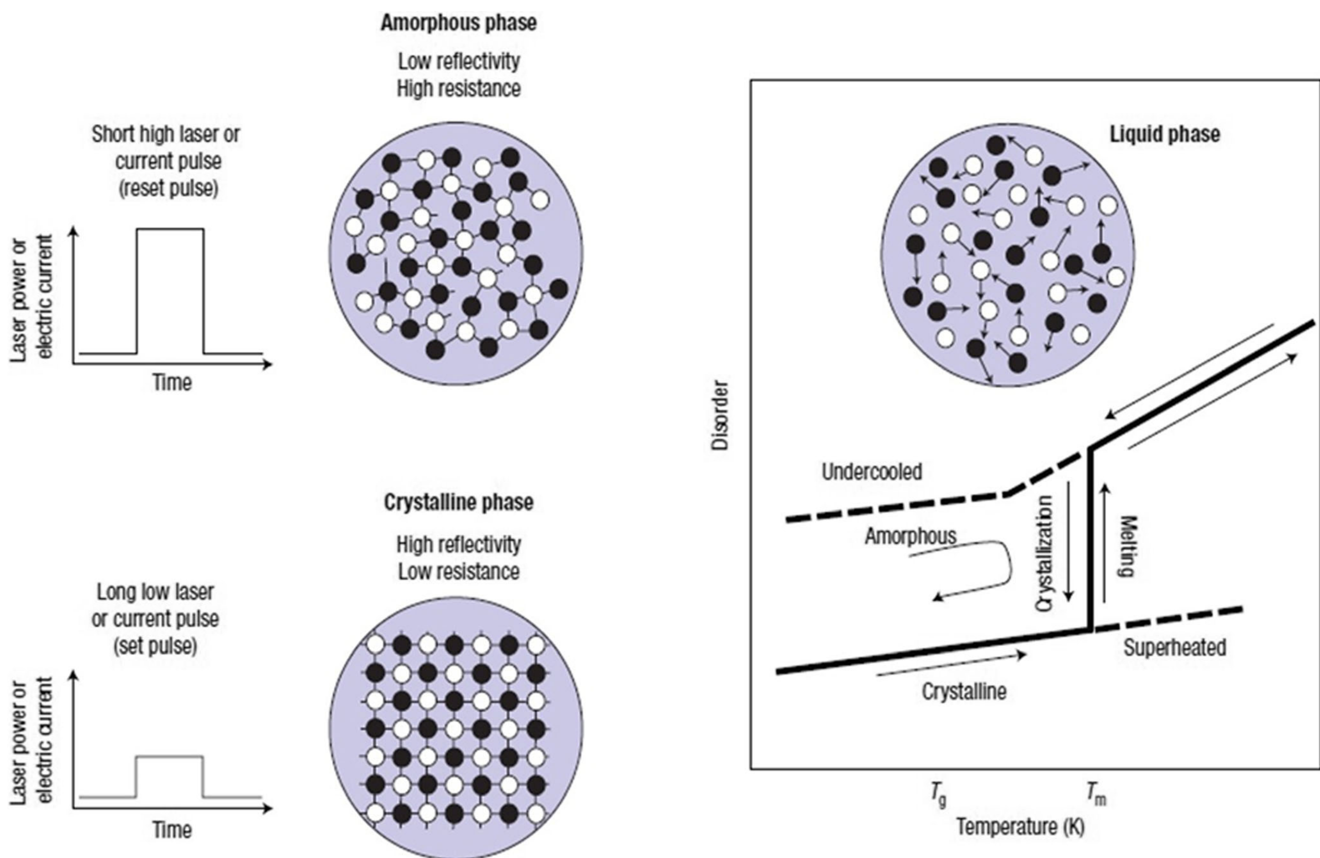



**Fig. 5** SET and RESET processes of a PCM device, where the amorphous phase represents the OFF state and the crystalline phase represents the ON state. (Ref. [53])

reliability and yield. Due to its maturity PCM may be the first "emerging" memory technology to see its applications in new memory or computing architectures in the short term. However, in the long-term redox devices (ECM or VCM) can lead to better memory products and potentially offer a more natural fit with emerging computing systems such as neuromorphic computing due to their bipolar, field-driven programming nature, lower power consumption, and higher integration density.

## 4 Memristive device applications: classical computing systems

The first application of memristive devices may arrive in the form replacing memory and logic elements in classical computing systems, which are facing multiple challenges at both the architecture and device levels. At the system level, the memory bottleneck associated with the conventional von Neumann architecture degrades the overall system performance [64]. While at the device level CMOS transistor scaling is expected to reach fundamental physical limits in around a decade [3, 4]. As a memory element, memristive devices offer many attractive properties that help address the memory and storage challenges of classical computers, as discussed below.

### 4.1 Memory and storage

Memory and data storage systems are major bottlenecks today limiting the classical computing system performance [64], a problem particularly exemplified in the current big data era. The speed and energy cost associated with data communication adds an extra dimension to the problem and led to the so-called memory wall [1, 2]. In the last decade, redox memristive devices in the form of resistive memories (RRAMs) have emerged as a promising candidate for ultra-high density data storage (e.g. solid-state drives, SSDs) and random access memory (RAM) applications [38, 46, 65, 66]. As discussed in Section 2, RRAM offers excellent scalability, fast access, low power, and wide memory margin [38, 67]. For example, RRAMs are overall much faster than traditional hard disk drives and Flash storage, and allow random write, read, and erase [38, 51]. These attractive properties make it possible to create a simpler and flatter memory system compared with the complex pyramid memory hierarchy used today [65]. In addition, RRAM fabrication requires a low thermal budget, enabling RRAM arrays to be directly integrated on conventional CMOS circuitry or other types of 3D integration of the memory with processor [68], as shown in Fig. 6. This high-density 3D integration of processor and memory can provide a

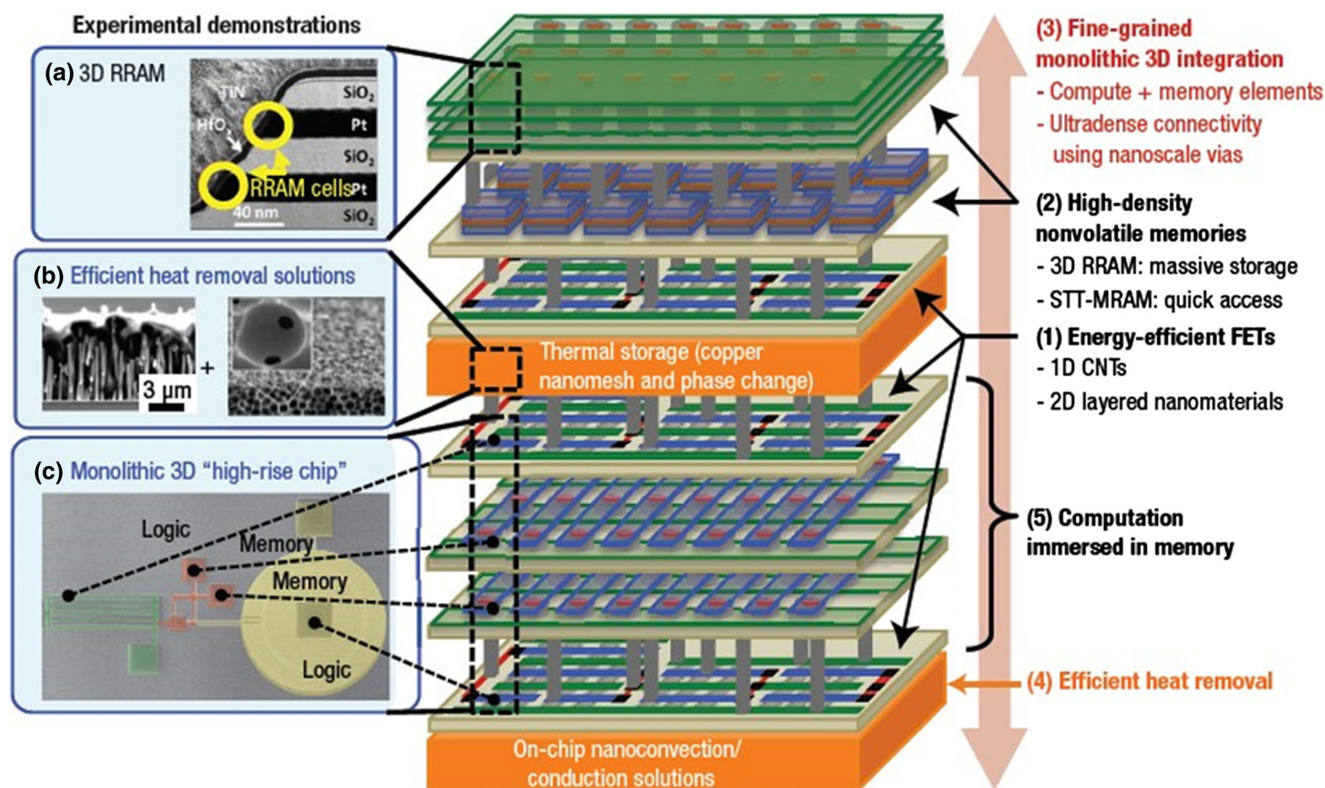



**Fig. 6** Schematic showing potential 3D monolithic integration of RRAM and digital logic on the same chip (Ref. [69])

significant boost to the computing system performance by addressing the communication bottleneck between memory and processors. Additionally, RRAM can be directly used in in-memory vector and hyperdimensional computing approaches [9, 70]. Altogether, this new device technology can extend the life of the von-Neumann computer architecture and enhance the system's ability to store and process large amounts data more efficiently.

However, a number of challenges still remain. The density advantage of RRAM originates from the simple crossbar structure, where a memristive device is formed at each crosspoint and can be used to store a binary bit of data (Fig. 2(a)). From a device perspective, fast access and wide ON/OFF margins are desirable, while a low write (erase) current is also needed to reduce power consumption during programming of large arrays. However, the low power memristive devices may be prone to high fabrication or runtime device variabilities. Additionally, while memory and data storage systems share many requirements, the tradeoffs between device retention and cycling endurance are considerably different in the two systems. A storage system requires years of retention but can survive with a low number of endurance cycles, as the case of Flash memories. On the other hand, memory systems can tolerate shorter retention with the aid of refresh cycles, but demands much longer write/erase cycles. Recent advances seem to suggest memristive devices may be better suited for storage type applications with lower fabrication cost, higher density, long data retention time but comparatively shorter endurance cycle compared to other memory technologies, namely, spin-transfer torque magnetic random-access memory (STT-MRAM), although continued material and device optimizations may lead to continued improvements in write/erase endurance to make RRAM better suited for DRAM or SRAM-like memory applications. Additionally, system-optimizations that utilize the retention properties of the devices may help alleviate the endurance requirement by reducing the number of refresh cycles, while other techniques similar to wear leveling typically used in Flash memories can also be utilized to improve the effective system endurance [71].

Another major challenge facing memristive devices as high-density memory elements is the sneak path problem [66, 72–75]. Unlike other potential applications, accessing memory/storage array is typically performed in a row-by-row fashion. In a passive crossbar structure, the read and write currents can pass through (possibly large amounts of) unselected devices in the crossbar, which can diminish the read/write margins as shown in Fig. 7. Sneak current also significantly increases the total current driving requirement of the circuitry and in turn, creates a practical limit on the size of the crossbar array. Different biasing techniques can be used to reduce the severity of the problem during read (at the expense of power consumption), but these techniques may not be efficient for practical array sizes [66]. Recent studies have shown

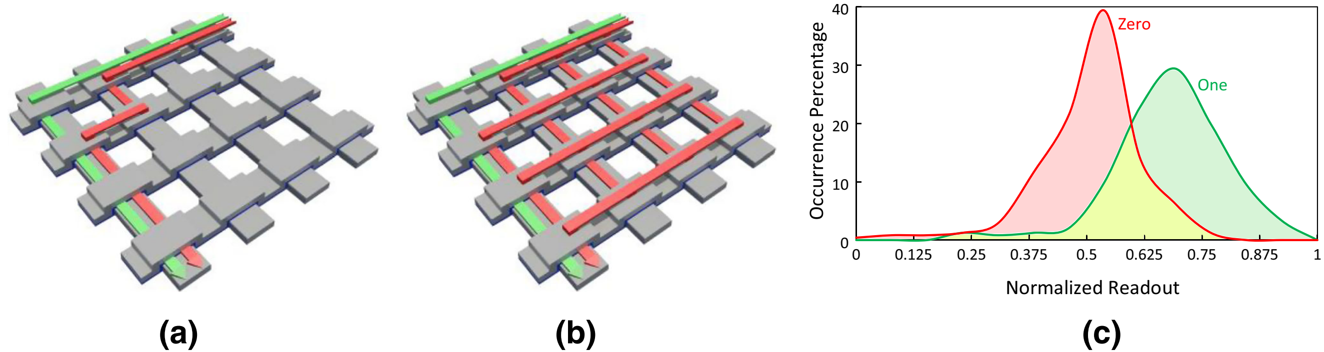



**Fig. 7** (**a**, **b**) Undesired sneak-paths in a passive crossbar array, (**c**) Readout distribution showing the loss of read margin with sneak current (Ref. [66])

that circuit level approaches can be adopted to mitigate the sneak-paths effect [66, 67, 73, 75]. Another approach is to add nonlinearity in the crossbar, either through memristive devices with intrinsic nonlinear I-V characteristics or more practically, through a serially connected "selector" element that offers a high I-V nonlinearity [76, 77] to eliminate the parasitic current effects [74]. The latter approach offers a modular design strategy, where the selector device is optimized for high nonlinearity and the memory element is tuned to meet the memory requirements. Typically, the two devices are stacked over each other to minimize device size [78]. Conventional transistors can also be used to reduce sneak currents in the 1-transistor 1-resistor (1T1R) memory cell structure [52, 79], although two-terminal selectors are more desirable for very high-density memory and storage applications.

### 4.2 Digital logic circuitry

Another area of study within the conventional computing architecture is to utilize memristive devices as MOS transistor replacements in a digital logic circuitry [10, 80–83]. Memristive logic circuits are reconfigurable and have a built-in memory functionality. Hoverer, to have any chance of being competitive memristive logic need to be as reliable and as fast as their CMOS counterparts, and offer better scalability and energy consumption. These requirements can be fulfilled only by low-power and fast memristive devices. Like their memory counterparts, digital logic circuitry cannot tolerate high device variability. The specific retention and endurance requirements depend on the adopted circuit scheme. For instance, implication, programmable logic-in-memory, and ratioed logic circuits [10, 82, 84, 85] use writing operation to implement the output function, thus will require very high device endurance. On the other hand, reconfigurable table [86] circuitry require writing only in the configuration stage and thus can use devices with limited endurance cycles. Similarly, one promising application for RRAM devices is using them as switching elements for programmable circuitry and FPGAs (Field-Programmable Gate Arrays) [87–89]. Here, the devices are used to connect the computing circuitry rather than performing the real computing. Since RRAMs can act both as switches and as memory, it can result in a much-improved circuitry from the area and power consumption perspective. Moreover, RRAM devices have much smaller footprints compared to its SRAM and FLASH counterparts commonly used in such types of circuits. On the other hand, programmable applications expect extremely high ON/OFF ratios from its switches and very long retention for practical applications.

## 5 Applications in emerging computing architectures

Perhaps the most intriguing aspect of memristive devices is their potential in emerging computing architectures. These architectures aim to address the computing challenges presented by today's applications, especially cognitive, data-centric, and smart sensor networks. Classical computers were originally designed to handle vast amounts of arithmetic operations with high speed and high precision. For example, the first known microprocessor chip Intel 4004 was developed for a calculator [90]. Conversely, many of today's applications involve the processing of visual, auditory, or other types of sensory data that can be affected by noise, and can in turn tolerate some amount of imprecision during computation. While some of the neural network and computational concepts being used for such tasks are not necessarily new, recent advances in hardware, including memristor-based devices and circuits, dramatically changed the landscape of the co-design and implementation of these emerging computing.

### 5.1 Neuromorphic computing

Neuromorphic computing is one such example. Neural networks have already demonstrated an extraordinary ability to carry out pattern recognition and inference in real-world applications, with much better efficiency and throughput than classical computing techniques [91–93]. However, these implementations are mostly based on conventional computing hardware that still suffers from the von Neumann bottleneck,

while the real potential of neuromorphic systems will only be realized after drastically re-designed hardware systems can be built that allow efficient mapping and operations of the neural networks [6, 15, 94, 95]. Neuromorphic hardware architectures typically comprise hybrid analog/digital circuits that implement physical models of neural computing systems, using computational principles analogous to the ones used by real nervous systems [11]. Below we provide a brief introduction of neuromorphic hardware systems, first based on mixed-signal CMOS implementation, followed by discussions on memristive-device implementations.

When implemented in analog VLSI technology, neuromorphic circuits use, to a large extent, the same physics used in real neural systems (e.g. they transport majority carriers across the channel of transistors by diffusion processes, very much like neurons transport ions inside or outside cell bodies through their proteic channels). Given the analogies at the single channel level, larger scale neuromorphic circuits share the same physical constraints of their biological counterparts (given by noise, temperature dependence, inhomogeneities, etc.) at the macroscopic level. Therefore, while these architectures often have to use a range of different strategies for optimizing robustness to noise, which in many cases are analogous to the ones used in biology, they also exhibit desirable features similar to those of real neural computing systems, such as very low power consumption, low size, low latency, and a high degree of fault tolerance. It is these very features that make neuromorphic circuits and systems optimally suited for integration with memristive devices [16].

Topologically, the memristive crossbar can be readily mapped into an interconnected network, thus allowing straightforward mapping of neural networks with each memristive device acting as a synapse connecting a pair of neurons (Fig. 8) [49, 96]. Figure 8(a) and (b) shows an example of a single memristor device acting as a synapse and reproducing the Spike-Timing Dependent Plasticity (STDP) behavior of biological synapses. Like a biological synapse, a memristor device stores and processes information at the same physical location concurrently. This is possible because the device's memory is represented by the two-terminal resistance, which in turn regulates information (current) flow between the pair of neurons connected to it. The excellent scalability of memristive devices further allows the implementation of high-density networks [38] and provide enough synaptic connections for practical applications.

Memristive networks have already been shown capable of performing different forms of neuromorphic tasks including pattern classification, feature extraction, analog sparse coding, and recognition, an example is shown in Fig. 8(c) [15, 97–101]. Neural networks are also natural applications for memristors due to the networks' ability to tolerate even very large device variations [102]. Device runtime stochasticity, often encountered in aggressively scaled memristive devices, can be even used as a useful property [14, 103, 104]. Neural networks may also help alleviate the tradeoff between device endurance and retention, as hours long retention can be sufficient for a neural network to operate. Write/erase cycles are encountered during the network training phase, which is typically infrequent during the lifetime of the network as most operations can be mapped into a read operation. On the other hand, most neural network learning algorithms rely on the use of "analog" devices whose conductance can be updated in an incremental, instead of binary fashion [49]. The linearity and symmetry of the incremental conductance (synaptic weight) update have also been shown to have a strong impact on network performance and need to be optimized [ 98]. Devices that can operate at low current is also desired to allow the realization of large networks. Such set of requirements imposes different challenges for the device design and fabrication, compared to memory and logic devices.

From a system point of view, several custom multi-chip and multi-core neuromorphic computing systems that support the implementation of large-scale neural networks have already been proposed using mixed-signal CMOS technologies [94, 105–108]. These systems, however, have all been designed and optimized to use standard memory technologies, such as on-chip SRAM or off-chip DRAM, and are still affected, to a large extent, by the von Neumann memory bottleneck problem [64]. Memristive devices offer a new solution to this problem, when integrated in neuromorphic computing architectures. An example of a recent neuromorphic VLSI device that is based on a multi-core distributed architecture that can exploit the desirable features of memristive devices is shown in Fig. 9. This device comprises massively parallel arrays of analog neuron and synapse circuits, and employs multiple routing strategies combining heterogeneous memory structures distributed across and within cores to configure the neuron networks of arbitrary topology, and to transmit the spikes among the neurons and synapses (S. Moradi et al. 2017, under review). Although the VLSI device of Fig. 9(a) makes use of capacitors, conventional CAM cells, and standard SRAM latches to implement the distributed memory elements, the architecture that this device embodies was designed to implement in-memory computing, with the goal of supporting the use of memristive devices as both digital and synapse-like memory elements (S. Moradi et al. 2017, under review). Indeed, the CMOS circuits implemented in this device are compatible with oxygen-ion based memristive device specifications (e.g. as those described in Section 2.2), which could be used as compact single-bit memory elements in place of the large CAM and SRAM circuits, and as dynamic synapse elements in place of the corresponding capacitors and subthreshold analog circuits.

The analog neuron and synapse circuits used in the device have been described and fully characterized in [13]., where adaptive integrate-and-fire spiking neuron models, and first-

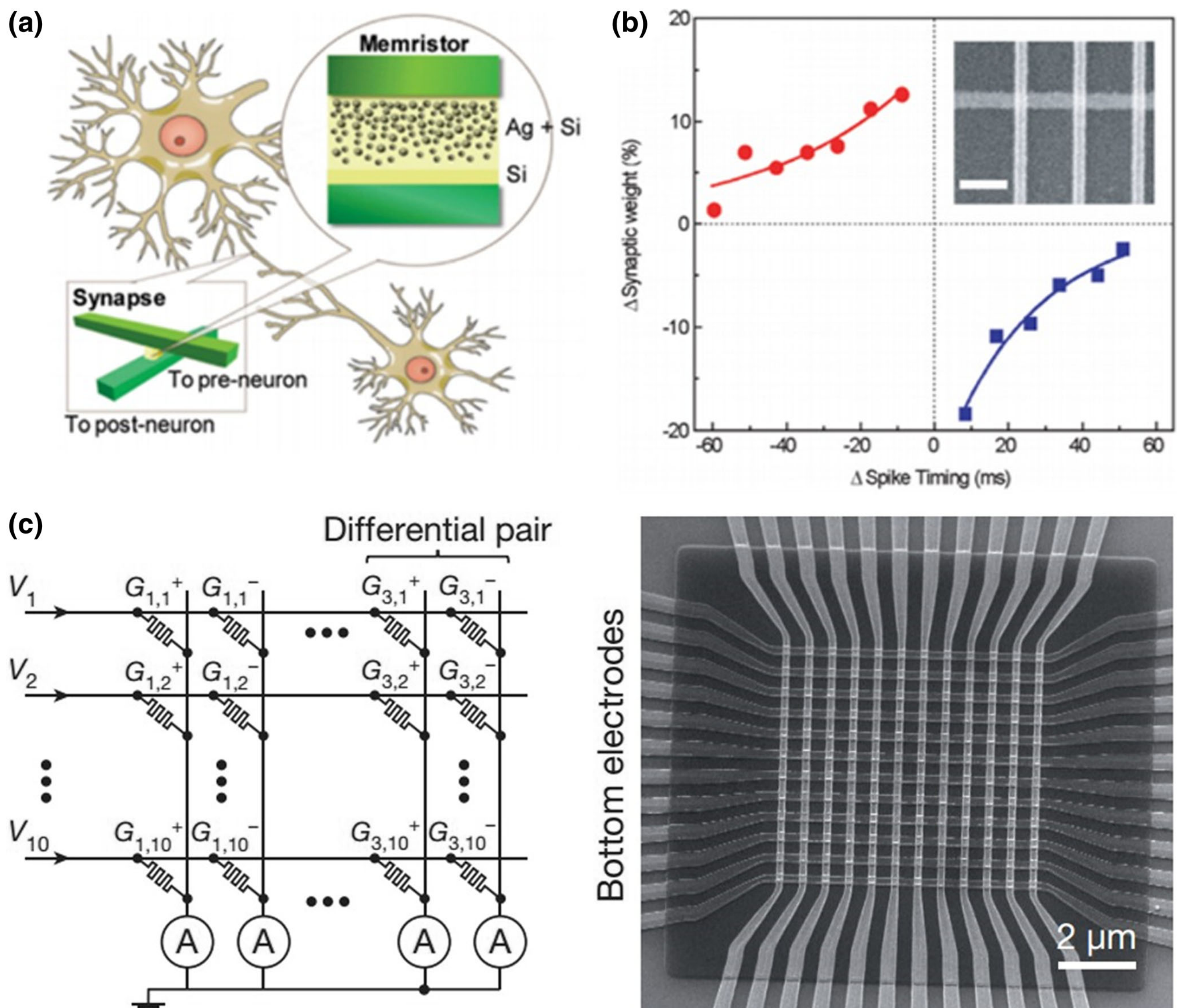



**Fig. 8** (**a**) Mimicking the biological synapse using a single memristor device. (Ref. [49]) (**b**) Measured STDP behavior from a memristor. (Ref. [49]) (**c**) Mapping neural networks into a crossbar structure, where a memristor is formed at each crosspoint and both stores and processes information (Ref. [15])

order dynamic synapse models were used. The digital circuits implement asynchronous event-based transmission modules that distribute the spikes produced by the neurons in real-time, without the need of any clock circuitry. Specifically, each neuron in a core transmits its output spikes to a local asynchronous router instantaneously, at the time in which they are produced. The router directly connected to the neurons, denoted as R1 in Fig. 9(b), can broadcast events back to the source core neurons and multicast events to other four possible cores. Connectivity among neurons, and specific network configurations (such as multi-layer, recurrent, convolutional, etc.) can be programmed by setting the appropriate bits in the CAM and SRAM circuits distributed within the cores and in the routers. The inter-core multi-cast event-based communication is managed by a different set of routers, denoted as R2 in Fig. 9(b). The R2 routers are distributed among the cores in a hierarchical way to implement a tree-based routing strategy. At the lowest level of this hierarchy, R2 routers distribute events to the four cores immediately connected to it. Events that need to be sent to more distant cores follow the hierarchy using higher level R2 routers. The block diagram of Fig. 9(b) shows an example of a multi-core chip with 64 cores, interconnected via three levels of an R2 router hierarchy. The architecture supports communication of spikes also across chip boundaries. To transmit events to neurons on different chips, a third router block, denoted as R3, is used. In this case, the routing strategy adopted is that of mesh-routing. The combination of different routing schemes (e.g., broadcast, multicast, tree-based, or mesh-based routing) allowed us to design an architecture that minimizes both the system-level bandwidth

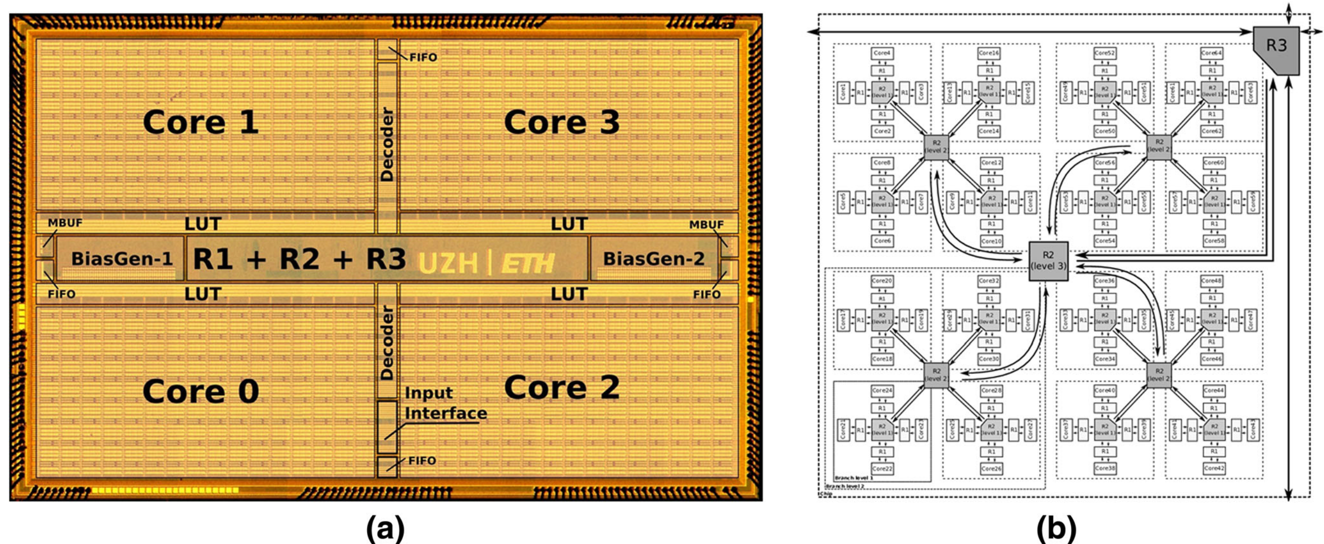



**Fig. 9** (**a**) Micrograph of a scalable multi-core neuromorphic processor with hierarchical on-chip digital routing circuits and subthreshold analog synapse and neuron circuits that reproduce biophysically realistic neural dynamics. (**b**) block diagram of an equivalent architecture with 64 cores, and five levels of routers (one for R1 routers, three for R2 routers, and one for R3 routers – see text for details). These chips were implemented using mixed-signal CMOS but the simple principle can be applied to hardware systems employing memristive networks

requirements for communicating spikes among neurons and the total (distributed) memory requirements for supporting a wide range of neural network topologies that can exhibit complex synaptic dynamics (S. Moradi et al. 2017, under review). This architecture has already been shown to support the implementation of Convolutional Neural Networks in real-time low-latency spatiotemporal pattern discrimination tasks [109], using CMOS circuits as programmable synaptic elements, with synaptic weights that are fixed (e.g. determined by an off-line training procedure and set at run-time configuration). Future integration with memristive devices will allow designers to implement synaptic weight learning mechanisms directly on-chip, both for implementing conventional machine learning algorithms such as Convolutional Neural Networks as well as more bio-inspired, spiking-based networks. Indeed, memristive devices have been shown to be able to faithfully reproduce spike-based learning mechanisms, for example, based on Spike-Timing Dependent Plasticity (STDP) learning rules.

### 5.2 Analog computing

Another promising application for memristive devices is analog computing. While the concept of analog computing itself is, in fact, older than the binary one, implementation of analog circuits at large scale is always challenging. The advances of memristor devices, however, may help speed up the development of efficient analog computing systems. For instance, the crossbar structure can natively execute the analog dot product operation - a core operation that can be found in many computing algorithms [110, 111]. Specifically, an analog vector-matrix multiplication requires a single execution step on a crossbar system, without moving data between a separate memory and processor, compared to sequential execution on classical computing architectures that demand frequent data movements. To some degree, the analog dot product operation can be considered as a generalized form of the synaptic function in a memristive synaptic network (Fig. 10). However, for arithmetic applications, the operation requires precise representation of the resistance levels and do not tolerate high variability. Also, analog computing devices should have higher endurance compared to their neuromorphic counterparts due to the need to repeatedly update the stored values and thus requires further device and material optimizations. In this sense, from a device perspective analog computing can be considered as the next step of neuromorphic computing. It is also worth mentioning here that memristors have also been explored for other interesting forms of analog computing approaches, such as in bio-inspired coupled oscillators [112, 113] and in finding the shortest path in a maze [114–116], where each of these applications can pose its own set of device requirements.

### 5.3 Stochastic computing and security applications

Stochastic computing utilizes basic logic gates to perform a complex arithmetic operation with the aid of randomly generated bit sequences [117]. Typically, this is realized with the help of PRNGs (Pseudo Random Number Generators) which unfortunately is expensive to implement in hardware. Recently, restive devices have been explored to replace the PRNGs circuits in stochastic computing [8, 118] by utilizing

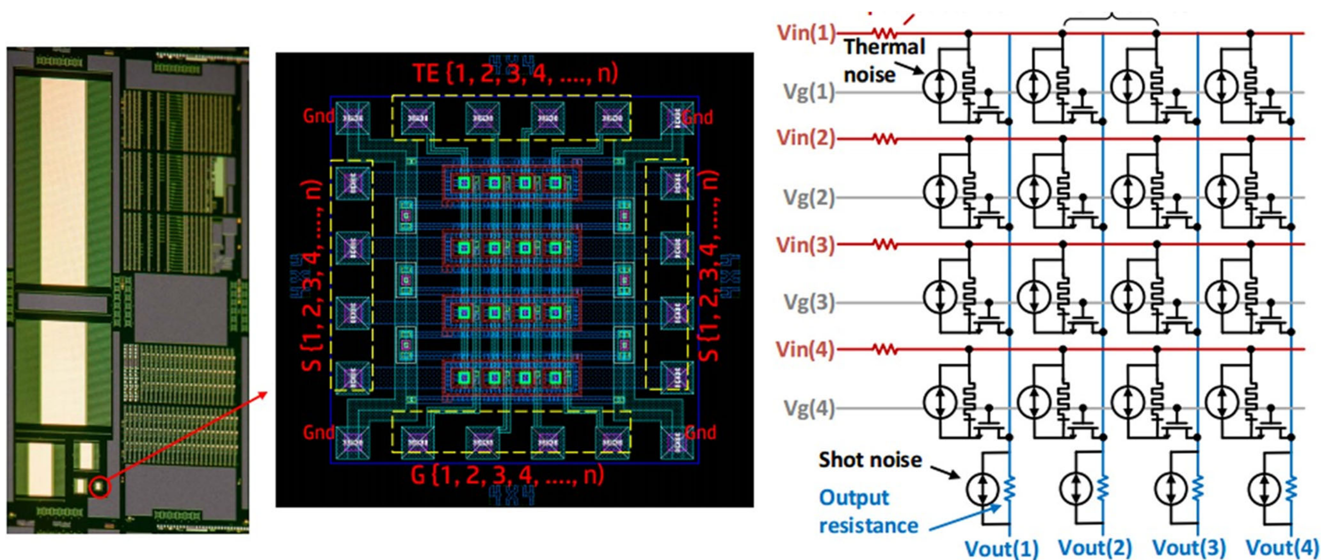



**Fig. 10** Example of a memristor-based analog dot-product engine (Ref. [110])

the native device runtime variability as a source of stochasticity. For instance, at a given switching voltage, the device will switch after a random time period following a Poisson distribution. Hence, a fixed wait time can be utilized to transform the memristive device into a compact RNG. In this case, devices with higher temporal variability (i.e. stochastic switching) are favorable. However, stringent spatial variability control is still needed to ensure different device follow the same distribution and programmable PRGN characteristics. Additionally, since the random sequence is generated by successive switching events, very high write/erase endurance is also required for such applications.

Some stochastic behaviors of RRAM are undesirable for memory applications, but could be utilized as entropy sources for hardware security features that embrace truly random variations. These behaviors include variability of RRAM device parameters (e.g., resistance, switching voltage), noise in read signal (e.g., random telegraph noise, RTN), and probabilistic switching (i.e., switching yield controlled by operation conditions). These random behaviors can be utilized to generate hardware security primitives, including True Random Number Generator (TRNG) and Physical Unclonable Function (PUF). For example, controlled switching of RRAM with a probability of 50% leads to an equal chance of a device falling in "0" or "1" states afterward. This behavior can be utilized to create a TRNG, which has been demonstrated experimentally with the proof of randomness [119]. Alternatively, the strong RRAM RTN signal has been used to generate random numbers in a simple circuit [120]. PUF utilizes the physical randomness to generate unclonable instance-specific security features and can be used as "fingerprint" for identification or authentication [121]. The variability of RRAM provides a unique source of randomness for PUF implementation. Unlike manufacturing variation exploited in most PUF implementations that is fixed post-fabrication, RRAM variability is intrinsic in physical mechanisms, less process dependent, and potentially reconfigurable [122]. RRAM-based PUF has been demonstrated experimentally using cell-to-cell resistance variation in a 1T1R RRAM array [123]. The reliability of RRAM-based PUF is strongly affected by the non-ideal behaviors of RRAM, including reading instability, thermal dependence of RRAM resistance, and retention loss [124]. Therefore, RRAM-based PUF needs to be optimized through material and device engineering to address these reliability issues. With significantly smaller footprint than other Si-based PUFs and lower power, RRAM PUF is more suitable for light-weight security applications, e.g., in Internet of Things (IoT).

## 6 Discussions

As discussed in sections 4 and 5 earlier, each potential computing applications pose a set of requirements to be fulfilled, whereas different memristive devices may offer different strengths and weaknesses. Some of the device shortfalls can be compensated at the architecture level, while others still require additional research efforts to improve the device performance. For example, the lack of device nonlinearity could be compensated by adding a selector element to the cell, while system level optimizations can alleviate data retention requirements by introducing refresh cycles (at the expense of device endurance and system total energy consumption). The same principle applies to runtime variability, where write-verify schemes can be adopted to reduce the programming error rate, at the cost of speed, endurance, and power consumption. Though some device properties can be traded off for others at the system level to fit a specific application requirement,

this rule does not apply to all device aspects. For instance, endurance, ON/OFF ratio, speed, and analog/binary behavior are permanent properties of the device.

We summarize the computing application requirements and the properties of the memristive devices as Radar charts shown in Fig. 11. It also highlights that some of the device shortfalls can be improved at the circuit and system levels (e.g. improved to the dashed lines). It is evident that there likely is no "universal" device that can meet the requirements of all applications. Instead, a particular device technology may be more suitable for a given set of applications. For example, data storage applications require high nonlinearity and large ON/OFF ratio to facilitate reliable data retrieval. Additionally, low power consumption is needed to support a competitively large array size under constraints imposed by the current delivering circuitry. Excellent retention is needed, while extremely long endurance is not necessary. From the device perspective, ECM is an excellent fit for storage applications, with its low programming current, excellent retention and high ON/OFF ratio. On the other hand, memory applications require much longer write/erase endurance cycles are needed and VCM devices with further material and device optimizations may be suited for this need.

The set of properties required for digital computation is also shown Fig. 11. Analog switching, device nonlinearity, or long retention is not essential in most of the cases. However, memristive digital computing needs to consume very low power, and offer excellent uniformity, endurance, and ON/OFF ratio to compete with its CMOS counterparts. These requirements are very challenging for the current state of memristive devices and demand extensive development at the material and device level. FPGA and programmable circuits share many requirements as digital computing systems, except for the tradeoff of high endurance with long retention. On the other hand, neuromorphic computing systems are very forgiving on many device properties include uniformity, retention, endurance, nonlinearity and ON/OFF margins. Yet it requires excellent analog switching properties to represent analog synaptic weight updates (during learning), and low power consumption to facilitate large networks. It thus appears that VCM devices are better suited for systems that require online learning thus analog weight updates, while ECM devices may be applied in systems that utilize off-line trained weights. Continued device optimizations are still needed to improve device variability, linearity of the weight updates, and power consumption. Similarly, analog computing systems, which could be considered as a generalized form of the neural networks, rely on dot product operations but may pose more stringent device uniformity requirements. Finally, some of the non-ideal effects in memristive devices, such as temporal variations, may be used as features in applications such as stochastic computing, whereas new requirements, such as very high endurance, need to be satisfied in these cases.

## 7 Conclusion

In conclusion, great strides have been made in the last a few years in the development of memristive devices and new computing architectures that can efficiently exploit the properties of such devices. In this review, we focused on the state-of-the-art memristive device performance and tried to map different devices to different potential computing applications. We

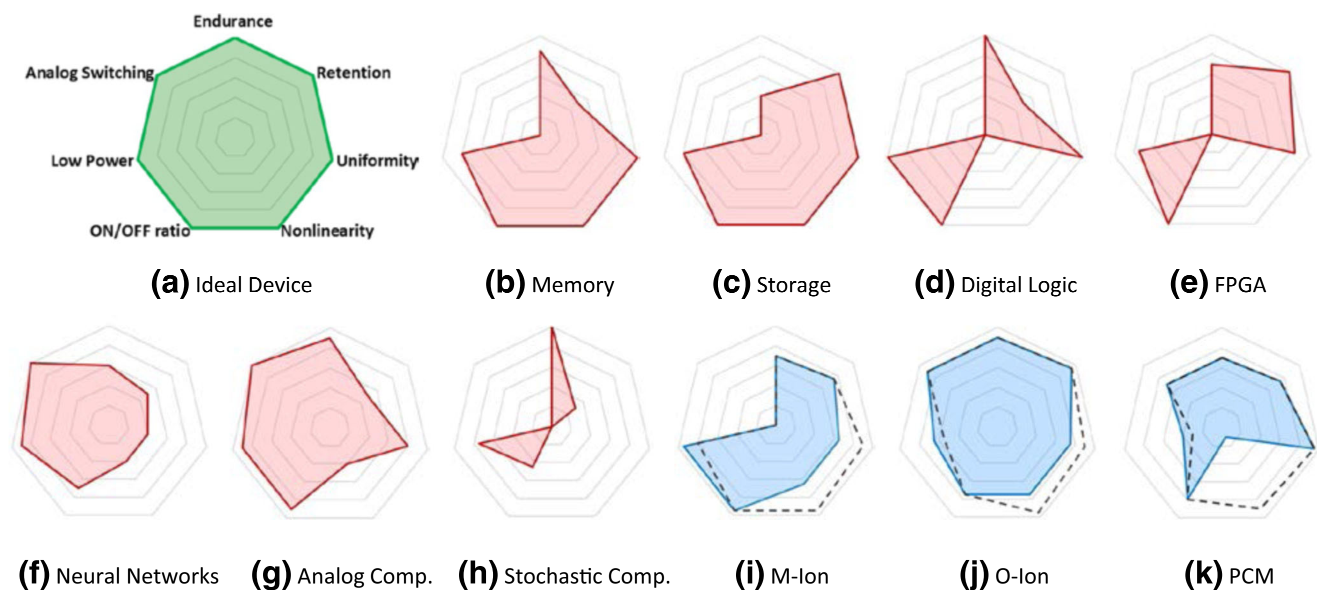



**Fig. 11** Qualitative Radar charts showing (**a**) ideal device characteristics. (**b-h**) Device properties required by each of the potential computing applications. (**i-k**) The current state-of-the-art redox and PCM device properties, and how they can be improved at the system level (dashed line)

briefly discussed the basic switching mechanisms of redox and PCM devices, as well as their strengths and weakness. From the application perspective, we believe redox-based memristive devices can help deliver computing hardware that is naturally suited for efficient, non-conventional computing architectures, although continued device and material optimizations are still needed. Finally, we note that the device properties can be more efficiently utilized and weaknesses mitigated, through synergistic research and co-design at both the device level and the architecture level. These types of multidisciplinary research, branching materials, devices, architecture and algorithm, is in urgent need to ensure that the continued performance improvements in electronics we have enjoyed over the last decades can be extended in to the foreseeable future.

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