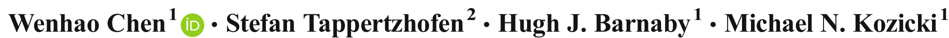
J Electroceram (2017) 39:109–131
DOI 10.1007/s10832-017-0070-5

SiO_2 based conductive bridging random access memory


Wenhao Chen[1] · Stefan Tappertzhofen[2] · Hugh J. Barnaby[1] · Michael N. Kozicki[1]

Received: 11 August 2016 / Accepted: 6 February 2017 / Published online: 15 March 2017
© Springer Science+Business Media New York 2017

Abstract We present a review on the subject of Conductive Bridging Random Access Memory (CBRAM) based on copper- or silver-doped silicon dioxide. CBRAM is a promising type of resistive non-volatile memory which relies on metal ion transport and redox reactions to form a persistent conducting filament in a high resistance film. This effect may be reversed to return the device to a high resistance state. Such control over resistance can be used to represent digital information (e.g., high =0, low =1) or produce multiple discrete or even continuous analog values as required by advanced storage and computing concepts. Many materials have been used in CBRAM devices but we concentrate in this paper on silicon dioxide as the ion conducting layer. The primary benefits of this approach lie with the CMOS process compatibility and the ubiquity of this material in integrated circuits which greatly lower the barrier for widespread usage and permit integration of memory with silicon-based devices. Our discussion covers materials and electrochemical theory, including the role of counter charge in these devices, as well as the current understanding of the nature of the filament growth. Theory of operation is supported by descriptions of physical and electrical analyses of devices, including in-situ microscopy and impedance spectroscopy. We also provide insight into memory arrays and other advanced applications, particularly in neuromorphic computing. The radiation tolerance of these devices is also described.

✉ Wenhao Chen
wchen113@asu.edu

[1] School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ 85287-5706, USA

[2] Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, UK

Keywords CBRAM · Resistive switching · SiO2 · Cu · Ag · Emerging memory

1 Introduction

In the era of information explosion, the sharing, storage and analysis of information is happening all the time at every corner of the world. The increasing popularity of virtual reality (VR), artificial intelligence (AI) and Internet of Things (IoT) also pose great challenge for efficient data manipulating. The desire for high density, fast speed and low power non-volatile memory has never been greater. Conventional magnetic hard disk drives (HDDs) are being relegated to back-up duty in data centers as their inherent high latency, high power consumption, considerable bulk, and fragility mean that they are less able to play in the new mobile markets [1]. NAND Flash bests HDDs in terms of latency and portability [2]. The scaling anxiety of planar NAND has been greatly relieved because of recent breakthroughs in 3D integration [3]. However, the programming speed and endurance of NAND Flash still cannot meet the requirements of many applications. In addition, the lack of ionizing radiation immunity of floating gate technology hinders its usage in the realm of medical equipment and space-based systems where radiation tolerance is required [4]. The reliability of NAND flash becomes even worse with continuous shrinking of device size since less than hundred electrons are stored in the floating gate for 1× nm technology node, single electron loss will introduce great variations in gate threshold voltage.

Resistive switching random access memory (RRAM or ReRAM) is a type of emerging non-volatile memory (NVM) technology. The resistive switching phenomenon that was first reported as early as the late 1960s [5] in binary oxide-based devices [6, 7]. It was reported that the device resistance was

tunable after a relatively high field dielectric soft breakdown. The device performance at that time was not good enough for memory applications. However, due to the advances in modern micro/nano fabrication and thin film deposition technology, the device performance was greatly improved and it gained significant attention from both academy and industry [8–10]. RRAM device has a simple metal-insulator-metal (MIM) structure in which an insulating thin film is sandwiched between two metal electrodes. The resistance of the sandwiched insulating layer can be changed between high and low resistance states by externally applied voltage, thereby the bit information, i.e. "0" and "1", is represented. Many models have been proposed to explain the resistance switching behavior, among which the 'filament' model is the most popular [11]. In the 'filament' model, the change in resistance is associated with the formation and dissolution of conductive filament in an otherwise insulating material. Due to its numerous merits [12], such as fast programming speed (in nanoseconds), excellent endurance (up to 10^{12} cycles), lower power consumption (~ 1 pJ/bit), RRAM is recognized to be one of the most promising alternative to Flash.

Based on the 'filament' model, three distinct switching mechanisms have been identified for the RRAM devices, i.e., a unipolar switching RRAM, a bipolar switching RRAM with conducting oxide filament and a bipolar switching RRAM with metallic filament [10]. NiO based devices are usually unipolar switchable [13], unipolar means that the device can be programmed and erased by voltage with the same polarity. It is believed that Joule heating plays an important role in switching process [14], the large switching current of NiO RRAM is not desirable for low power memory applications. Many transition metal oxides have been tried for resistive switching including both binary oxides, such as HfO_x [15–17], TaO_x [18, 19] and TiO_x [20, 21], and complex oxides such as $SrTiO_3$ [22–24], in which a bipolar switching characteristic is often observed. Different from unipolar RRAM, the programming and erasing of bipolar RRAM is achieved by applying voltage with opposite polarity. The conductive filament in bipolar RRAM is composed of a highly reduced oxide phase in which the metal valance state deviates from its stoichiometric value. Such oxygen deficient phases can be generated and recovered through a field induced drift of oxygen anions [25]. The need for oxygen transport (or change of metal valance state) in switching process has led to this technology known as OxRAM (or VCM, valance change memory) [26]. The third RRAM type has a similar switching mechanism to the second one in terms of its voltage requirement. It also requires voltage with opposite polarity for programming and erasing. However, instead of oxide filament, it has metallic filament which relies on electrochemical redox reactions and the transport of metal ions (typically Ag or Cu ions) [27]. This type of RRAM is called conductive-bridging RAM (CBRAM), programmable metallization cell (PMC), or electrochemical metallization (ECM) memory. As has been discussed, CBRAM and OxRAM have many similarities. For example, both of them are bipolar type memory and rely on ion transport to form the conductive filament(s). However, a key difference between them is that in OxRAM both electrodes are inert while one electrode in CBRAM has to be electrochemically oxidizable in order to supply metal ions for filament formation. The active electrode is usually made of Ag or Cu while the inert electrode can be W, TiN, Pt, etc. The thin solid electrolyte layer in between can be chalcogenide glass, oxides, amorphous Si, or a multi-layered film. Examples of solid electrolyte used in CBRAM are presented in Table 1. The underlying electrochemical interactions in CBRAM is generally reviewed in Section 2 and a discussion of electrochemical process for CBRAM composed of different materials system is also provided in [28]. Chalcogenide based CBRAM has been commercialized in the form of discrete non-volatile memory components, indicating that the operating characteristics of the technology are sufficiently robust for demanding markets [29, 30].

Whereas chalcogenide based CBRAM devices have proven to be viable replacements for certain types of non-volatile memory devices, there is still some unwillingness, particularly with major integrated circuit foundries, to incorporate these materials into back-end-of-line (BEOL) processing. Ironically, a potential solution to the reticence surrounding "new materials" lies with Cu diffusion in deposited silicon dioxide films, as both materials are commonplace in advanced ICs. Cu migration in dielectrics has been a persistent problem for semiconductor manufacturers who wished to adopt Cu interconnect [31] but Cu-SiO_2 based CBRAM exploits this "problem" to enable controlled transport of Cu and metallic bridge switching in the SiO_2. This approach has drawn increasing attention in recent years since the devices exhibit similar switching characteristics to those based on chalcogenide glasses while possessing inherently greater CMOS compatibility. In this paper, we present a review of the developments in SiO_2 based CBRAM using either Cu or Ag as active electrode.

Table 1 Examples of material systems used in CBRAM devices

Chalcogenide glasses (ChG)	Dielectrics	Layered
Ge_xSe_y [32–40]	SiO_2 [52–59]	Cu_xS/SiO_2 [76]
Ge_xS_y [29, 36, 41–47]	Ta_2O_2 [60–64]	$Ge_{0.2}Se_{0.8}/Ta_2O_5$ [77]
Ge-Te [48]	WO_3 [65–67]	CuS/CuO [78]
Ge-Sb-Te [49]	Al_2O_3 [68–72]	Ge_xSe_{1-x}/SiO_2 [79]
As_2S_3 [50]	a-Si [73, 74]	
Zn_xCd_{1-x} S [51]	GdO_x [75]	

2 Physicochemical principles and materials

2.1 Filament growth in SiO_2 CBRAM

The filament growth in chalcogenide based CBRAM has been well described in many works [9, 80]. It is generally accepted that a metallic filament grows from inert electrode towards active electrode, resulting in a conical shape with a thicker body near inert electrode and a thinner body near active electrode. However, due to the low ion mobility in many oxides, the direction of filament growth in SiO_2 based CBRAM may be different. Some of recent works suggest that the filament in thin film oxide grows from active electrode towards inert electrode, therefore, a reversed conical filament is formed [81–83]. Based on these works, a filament growth model for Cu-SiO_2 CBRAM has been proposed and is depicted in Fig. 1.

First, one should notice that the line with solid circle marker in Fig. 1 is a typical switching curve of Cu-SiO_2 CBRAM. The x-axis is the applied voltage, which is referenced from the Cu top electrode to the inert metal bottom electrode. The y-axis is the corresponding current through the two terminal device. In the initial high resistance state (i), it has only small amount of Cu ions close to the Cu electrode which could be due to incidental incorporation of Cu during device fabrication. Under positive bias the Cu electrode will lose electrons through an oxidization process and generates Cu ions ($Cu \rightarrow Cu^{2+} + 2e^{-}$). Cu ions in SiO_2 will drift towards the inert electrode along the electric field. Different from ions in chalcogenide materials, the Cu ion moves much slower in SiO_2, thus, the reduction of Cu ion occurs before it reaches inert electrode by capturing electrons tunneling through thin SiO_2 film ($Cu^{2+} + 2e^{-} \rightarrow Cu$). As long as there are enough electrons tunneling through and reducing Cu ions, a filament will start growing from the active electrode towards inert electrode (ii) until a bridge between the terminals is formed (iii). At this point, the device is switched to a low resistance state (LRS) and the current increases dramatically until limited by current compliance. This HRS to LRS transition is also known as the set process which is marked by the arrow on right side of the figure. Since the ion concentration close to Cu electrode is higher than the reset of SiO_2 film, the formed filament has a thicker body at Cu electrode and thinner body at inert electrode resulting in a reversed conical shape. Reset is essentially an opposite process of the set process. The conductive filament will be oxidized and dissolved into the SiO_2 matrix if a negative voltage is applied, then it switches back to HRS (iv). The reset process is initiated at the inert electrode/oxide interface which is the weakest part of the filament. The LRS to HRS transition is marked by the blue arrow on left side of the figure.

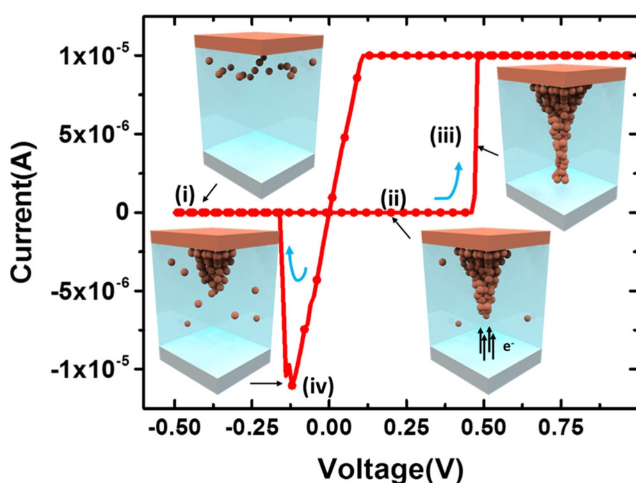


Fig. 1 Schematic of filament growth and dissolution in Cu-SiO_2 CBRAM. © 2015 IEEE. Reprinted with permission from Ref. [87]

It should be noted that the above model illustrates only one out of many possible mechanisms for filament growth in thin film oxides, but it is good enough to explain the common approach of resistive switching and the primary redox reactions in SiO_2 based CBRAM. Indeed, due to the variations in thin film properties, fabrication conditions and characterization environment, inconsistent filament morphology and growth direction have been reported across different works. Some in-situ microscopy of oxide based CBRAM also show a reversed filament growth, i.e. from inert electrode towards active electrode [84, 85]. In addition, recent electrochemistry studies point out that water moisture in SiO_2 may affect the growth dynamics in significant way [86]. A detailed discussion on this will be provided in a later section.

2.2 Cation conduction in SiO_2 thin films

Classical solid electrolytes such as silver iodide (AgI) show essentially no electronic conduction. In contrast, higher chalcogenides can be doped to become mixed ionic-electronic conductors (e.g. Ag-GeS [88] or Ag-GeSe [89]). Oxides such as SiO_2, Ta_2O_5 or Al_2O_3 are not considered as classical electrolytes but at the nanoscale they can conduct cations. This is exploited in oxide based CBRAMs. The diffusion coefficient of singly ionized cations in bulk SiO_2 has been measured by capacitance-voltage measurements and Rutherford backscattering spectroscopy [90]. When extrapolated to room temperature, the diffusion coefficient of Cu^+ and Ag + would be $D_{Cu} \approx 10^{-21}$ cm^2/s and $D_{Ag} \approx 10^{-23}$ cm^2/s respectively. With the ion drift velocity for high-field ionic drift given as

$$v_D = \frac{Dze}{k_B T} E_0 \exp\left(\frac{E}{E_0}\right), \tag{1}$$

a typical switching voltage of $V_{SET} = 0.5$ V and a SiO_2 film thickness of 20 nm (i.e., an electric field of $E = 250$ kV/cm), one would calculate a switching time of more than a year. Here, k_B is the Boltzmann constant and $E_0 = 1$ MV/cm [91].

Even if the effective length of cation migration is reduced to 1 nm, the calculated switching time is still orders of magnitude higher than observed in experiments. It is difficult to explain higher diffusion coefficients by Joule heating in SiO_2 based CBRAMs (in contrast to OxRAMs based on the Valence Change Mechanism [92]), as switching is reported even in the pA-range [93]. Recently, redox reactions of Ag or Cu at the interface with SiO_2 [53, 58] have been studied by cyclic voltammetry (CV) and the estimated diffusion coefficients are much higher than reported for bulk materials.

Figure 2 depicts exemplary cyclic voltammograms (1st cycle of a pristine cell and a subsequent cycle) of a Cu/SiO_2/Pt CBRAM device. The current peaks j_p are attributed to anodic and/or cathodic redox reactions. As a three-electrode configuration is difficult to use in vertical thin film structures, specific redox reactions cannot simply be identified by the peak positions. However, we can use the standard redox potentials (Table 2) to discuss which reactions are most likely to be observed [53, 94]. For the pristine device (no cations present), Cu is at first oxidized to Cu^{2+} given this reaction is thermodynamically more favourable and $j_{p,ox(1)}$ is attributed to this reaction. The oxidation to Cu^+ takes place at higher absolute voltages. When the voltage direction is changed, Cu^+ is reduced to Cu ($j_{p,red(2)}$) and afterwards Cu^{2+} to Cu ($j_{p,red(1)}$). There might be also a reduction of Cu^{2+} to Cu^+ at even lower voltages. Some Cu^+ ions may not be reduced during the first cycle and an oxidation to Cu^{2+} takes place at the beginning of the second cycle ($j_{p,ox(2)}$, which is not observed in the first cycle). Apparently both cation species can be found in SiO_2. X-ray absorption spectroscopy reveals that Cu^{2+} is the more mobile ion species than Cu^+, thus Cu^{2+} is believed to dominate the switching effect [95]. From the CV-curves the ion concentration and diffusion coefficient can be estimated [96].

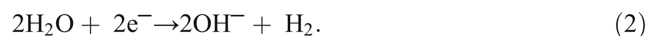
In contrast to AgI the ion concentration in SiO_2 depends on the device operation. When the voltage sweep rate ν is high, only a short time to generate ions is available, and thus the ion concentration c_{ion} is lower compared to low sweep rates (c_{ion} accounts for all ion species, including cations and counter charges, see below). Due to ion-ion interactions similar to what is observed in concentrated solution conditions, the effective diffusion coefficient of the ions depends on c_{ion} [53]. Figure 3 depicts the ionic diffusion coefficients of Ag and Cu based SiO_2 and Ta_2O_5 cells, respectively. Note that the diffusion coefficient shown here is that of the limiting ionic species. As there is a difference between Ag and Cu based cells (assuming similar redox reactions at the counter electrode) D_{ion} is most likely the diffusion coefficient of Ag or Cu ions, respectively.

Table 2 Standard redox potentials of some selected redox reactions [94]

Reaction	Me = Cu	Me = Ag
Me^+/Me ($E^{\varphi,1}$)	0.52 V	0.8 V
Me^{2+}/Me ($E^{\varphi,2}$)	0.34 V	-
Me^{2+}/Me^+ ($E^{\varphi,3}$)	0.16 V	1.98 V
$2H^+ + 2e^- \rightarrow H_2$	0 (exactly)	
$O_2 + 4H^+ + 4e^- \rightarrow 2H_2O$	1.23 V	

2.3 Electrochemical reactions and the role of counter charge

Early simplified switching models [99] only accounted for the anodic oxidation at the active electrode and the role of the counter electrode was almost ignored. When no cations at the filament tip or at the counter electrode are available, a counter reaction is required to compensate the reaction at the opposite electrode. Electro-neutrality is given by either a redox reaction at the counter electrode and/or counter charges including hydroxide ions OH^- or electrons. Surprisingly, the compensation of the anodic oxidation just by electrons (leakage current) has been found to be less likely by various switching studies in variable atmospheres [86]. The electrode reaction may therefore be represented by



$$2H_2O + 2e^- \rightarrow 2OH^- + H_2. \quad (2)$$

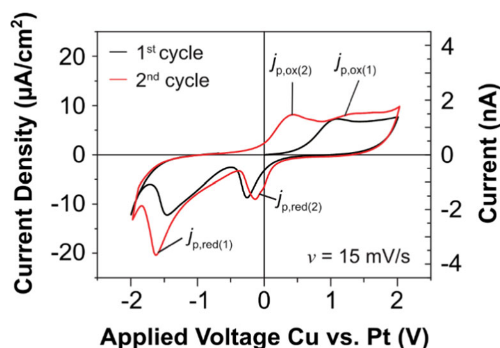


Fig. 2 Cyclic voltammetry of a Cu/SiO_2/Pt CBRAM device (reproduced from Ref. [53] with permission by the Royal Society of Chemistry)

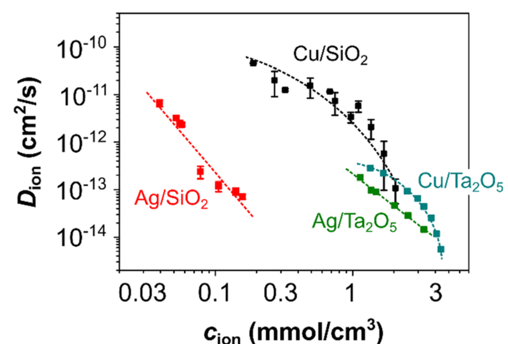


Fig. 3 Ionic diffusion coefficient of Ag and Cu based SiO_2 (data from Ref. [53, 97]) and Ta_2O_5 (data from Ref. [98]) CBRAMs

In Eq. 2, the OH¯ are the counter charges. As previously mentioned, the overall ion concentration c_{ion} consists of all involved ions and the contribution of cations c_{Me^+} and OH¯ c_{OH^-} cannot be clearly separated by measurement (assuming no electronic conductivity):

$$c_{\mathrm{ion}} = c_{\mathrm{Me}^+} + c_{\mathrm{OH}^-} \quad (3)$$

However, for Ag-based devices $c_{\mathrm{Me}^+} \approx [\mathrm{Ag}^+] \approx c_{\mathrm{OH}^-}$ and for Cu-based devices $2\, c_{\mathrm{Me}^+} \approx 2\, [\mathrm{Cu}^{2+}] \approx c_{\mathrm{OH}^-}$ is a reasonable approximation.

Knorr et al. first reported the impact of water on switching in organic thin film junctions [101], followed by experiments for Ta_2O_5 and SiO_2 based devices [100, 102]. While Tsuruoka et al. reported on the strong impact of the ambient humidty on the SET voltage V_{SET} of Cu/SiO_2/Pt devices, no effect is observed for Ta_2O_5 based devices (Fig. 4(a)). FT-IR studies revealed that for Ta_2O_5, incoporated water is not removed in vacuum [100]. However, in a recent study, Mannequin et al. showed that the sensitivity to the water partial pressure $p\mathrm{H_2O}$ depends on the deposition conditions [103].

The influence of the ambient atmosphere on SiO_2 devices is not due to a water-triggered increase of the ion mobility. Figure 4(b) depicts CV-curves for a Cu/SiO_2/Pt CBRAM for variable $p\mathrm{H_2O}$ [86]. The electrochemical response is increased by the increase of $p\mathrm{H_2O}$, and so is the ion concentration while the diffusion coefficient remained nearly constant. More importantly, the electromotive force (emf) depends strongly on $p\mathrm{H_2O}$ (Fig. 5(a)) [86]. In a high input-impedance emf measurement, the impact of the ion mobility is completely supressed. The cell voltage V_{Cell} is directly linked to the emf-voltage by the ratio of the ionic and electronic transfer numbers [105]. By tuning $p\mathrm{H_2O}$, V_{Cell} can be reproducibly increased and decreased (inset Fig. 5(a)). The more hydroxide ions can be formed, the more cations are injected into the oxide. Thus, c_{ion} depends on the catalytic activity of counter electrode material. Electrodes like Pt, Ir or Ni show a high ion concentration compared to electrode materials like Zr or Ti as expected from their hydrogen evolution potential [104].

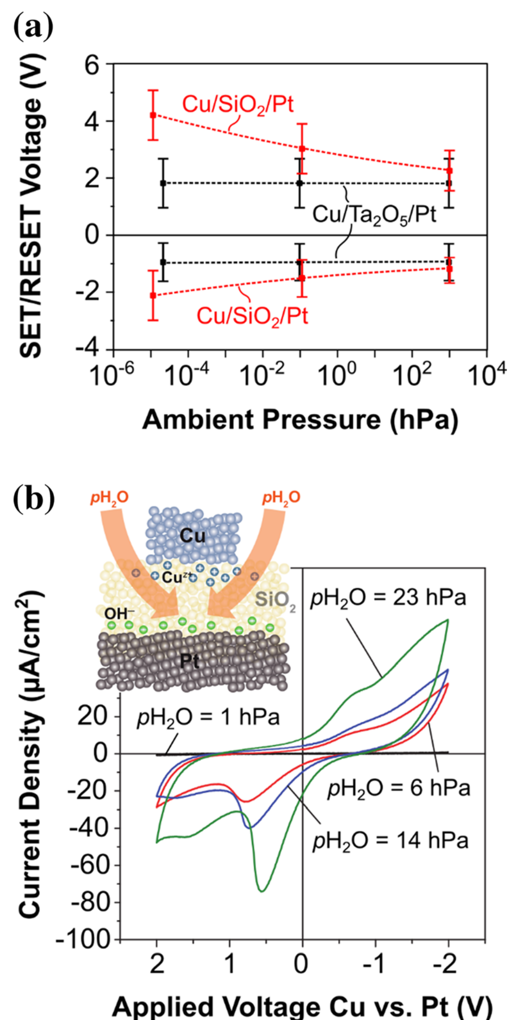


Fig. 4 Impact of (**a**) the ambient pressure on the resistive switching characteristics of SiO_2 and Ta_2O_5 based systems (reproduced from Ref. [100] with permission by John Wiley and Sons), and (**b**) the impact of the water partial pressure $p\mathrm{H_2O}$ on CV curves of Cu/SiO_2/Pt CBRAMs (reproduced from Ref. [86] with permission by the American Chemical Society)

3 Device characterization

3.1 Recent advances and challenges in in-situ electron microscopy

The filamentary model was proposed based on the electrical characteristics of the device, including the dramatic change in current and the observation that the on-state resistance does not scale with electrode size [38]. However, direct evidence of filament existence is required to support such hypothesis. Electron microscopy (EM) is a versatile technology to monitor the filament in CBRAMs and to characterize the switching in-situ (or *in-operando*). There are three EM techniques to be distinguished:

- Scanning Electron Microscopy (SEM)
- Transmission Electron Microscopy (TEM)
- Scanning Transmission Electron Microscopy (STEM)

The first ex-situ images of conductive filaments in CBRAM-type switches were reported by Guo et al. in 2007 in a Ag/H_2O/Pt system [106], in which the conductive filament after switching were analysed by SEM. Since then, this simple but efficient technique has been widely adopted to image filaments grown in many CBRAMs, including SiO_2 based CBRAM [82, 107]. Figure 6 shows a SEM image of filament growth in Ag/SiO_2/Pt planar CBRAM. As shown in

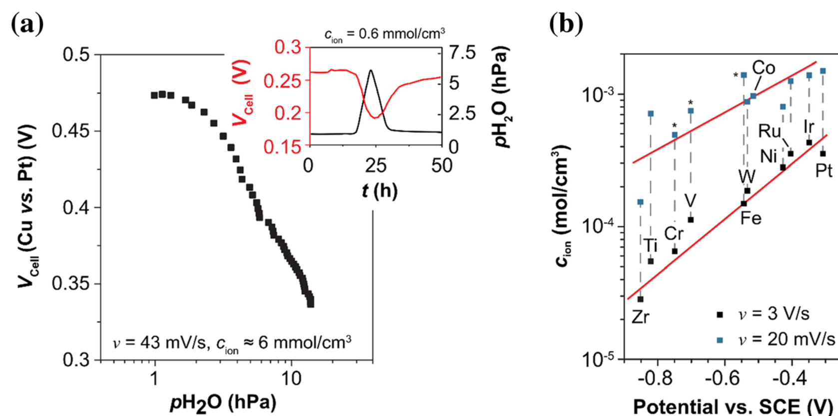


Fig. 5 Role of OH⁻ on redox reactions in SiO_2 based CBRAMs. (**a**) Impact of pH_2O on the cell voltage V_{Cell}, and thus, on the emf-voltage. The cell voltage can be reproducibly increased and decreased (shown in inset). Reproduced from Ref. [86] with permission of the American Chemical Society. (**b**) Impact of the ion concentration on the counter electrode materials' hydrogen evolution potential (reproduced from Ref. [104] with permission by the Royal Society of Chemistry)

Fig. 6(d), a Ag filament appears after 30 V voltage applied on Ag electrode for 210 s. The filament has a conical shape with a thicker part close to Ag electrode. Rather than a continues metallic filament usually observed in chalcogenide based CBRAM [108], the filament in SiO_2 shown in Fig. 6 is composed of many discrete Ag particles distributed on the surface or penetrated into SiO_2 layer. This granulated filament can be a result of low ionic mobility and redox reaction rate in SiO_2 material.

An early TEM imaging of physical filament was reported by Zhi et al. in which real-time filament growth in a Ag/Ag_2S/W CBRAM was characterized in-situ [109]. Later, ex-situ TEM studies on the growth of filaments in Ag/SiO_2/Pt were reported by Yang et al. [82]. In contrast to the devices studied by Zhi et al., the authors fabricated planar structures with a lateral gap in between the Ag and Pt electrode (gap length ≈ 200 nm). A pristine device, the device after switching and after erase are shown in Fig. 7(a–c), respectively. Figure 7(d, e) depict the *I*/*V* curves for switching and erase. Interestingly, more than one filament is formed (indicated by arrows) in the gap. Moreover, the filament grows from the Pt electrode towards the Ag electrode, which is consistent with the classical electrochemical theory [10]. In another device, where the authors studied the formation of the metal bridge by ex-situ SEM, the filament appears to grow from the Ag electrode towards the inert electrode.

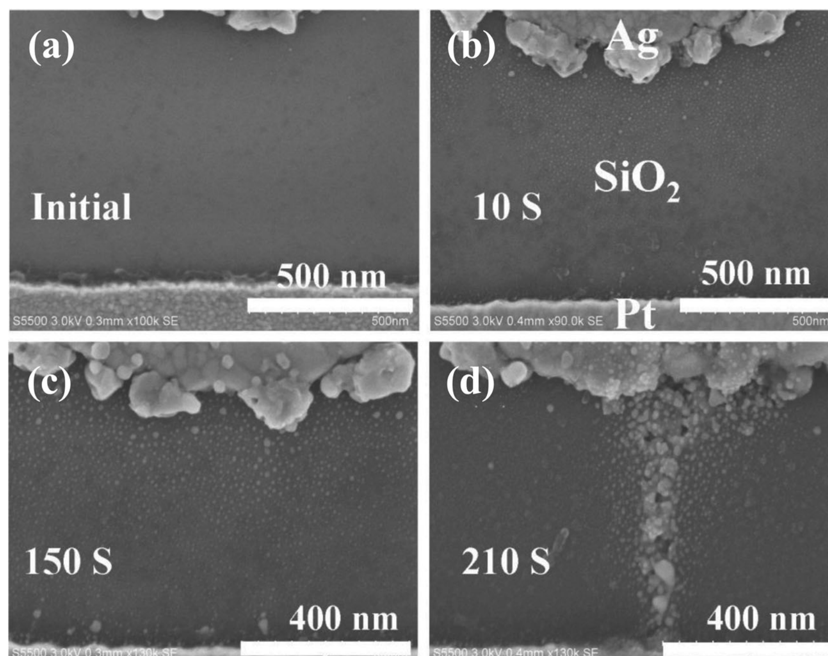


Fig. 6 Dynamic filament growth in planar Ag/SiO_2/Pt CBRAM. (**a**) as-fabricated device, (**b**–**d**) stressed for 10s, 150 s, 210 s at 30 V with compliance current of 10uA. Reprinted by permission from John Wiley and Sons: Advanced Functional Materials, Ref [107]

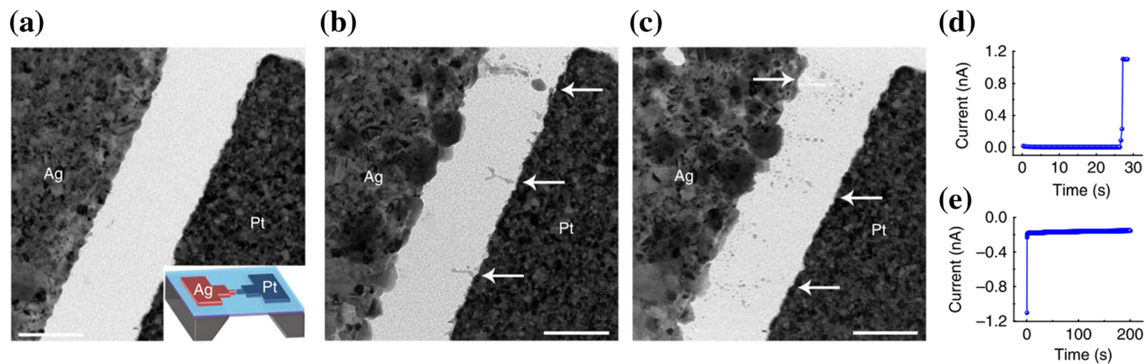


Fig. 7 Ex-situ resistive switching of a Ag/SiO_2/Pt lateral device on suspended Si_3N_4 TEM windows. The scale bar for a-c is 200 nm. (**a**) Pristine state of the device after fabrication. The device structure is shown in the inset. (**b**) Device after resistive switching and (**c**) after erase. (**d**) and (**e**) depict the *I*/*V* curves for switching and reset, respectively. Reprinted by permission from Macmillan Publishers Ltd.: Nature Communication, Ref. [82], copyright 2012

More recently, Yang et al. published a study on resistive switching analysed by in-situ TEM [110]. In this study, the authors deposited a thin layer (~ 10 nm) of SiO_2 on a sharp and movable W-tip to contact the oxide with a Ag wire forming a W/SiO_2/Ag layer structure. The in-situ observations indicate a growth of the Ag filament (within the oxide) towards the W electrode and part dissolution of the filament upon reset. However, the current response during the switching looks significantly different from what is typically observed in crossbar devices in ambient conditions. Again, this could be contributed to the absence of OH^- ions acting as counter charges. In the same study, the authors fabricated Au/SiO_2/Au devices by FIB-cut with Ag, Cu, Pt and Ni particle inclusions in the oxide matrix. By applying a voltage between the Au electrodes, the particles migrate within the oxide. The authors concluded that their observations can be best explained by dynamic nanoparticles within the oxide which are formed and migrate depending on a complex interplay between the redox rate (i.e., how fast ions are generated) and the ion mobility (see Fig. 8). This interplay could not only explain the different growth directions observed for CBRAMs but also the different sizes and shapes of filaments observed by in-situ and ex-situ TEM. Furthermore, the redox rate and ion mobility may be different on the local scale and subject to the ambient conditions as well.

It stands to reason that the electron perturbation into the switching material during in-situ TEM could affect the formation, reduction and migration of cations (and could even act as counter charges). With a typical TEM electron-beam current well below $I = 1$ μA ($n_e = I/e \approx 6 \times 10^{12}$ electrons per second), an acceleration energy of E = 200 keV = $m_0 v^2/2$ and the electron mass m_0 = 9.12 × 10^{-31} kg, the electron velocity is $v \approx 2\text{x}10^8 \text{ms}^{-1}$. Each electron is then separated on average by $v/n_e \approx 30$ μm, and thus, with a sample thickness usually below 100 nm statistically less than one electron is found in the specimen at a given moment. Hence, unintentional interactions of the electron-beam with cations might seem to be a minor problem. However, especially at low switching currents below 100 nA, electron-beam induced artefacts might be inevitable.

A more serious concern is the device geometry. For purely lateral devices where the electrodes are patterned by electron-beam lithography for example, the switching gap distance (e.g. 200 nm [82]) is significantly larger than for vertical devices (usually below 20 nm). Furthermore, devices prepared by FIB cut can suffer from ion-beam induced damage [111]. In most cases, the geometry and surface to volume ratio is different from that of vertical devices and filaments could be formed (in part at least) at the surface of the oxide matrix rather than inside. For lateral devices the electrodes might be also affected by unintentional surface oxidation during device fabrication, which results in a chemically different electrolyte/active electrode interface. Moreover, switching in high-vacuum is reported to be different from switching in ambient conditions for many CBRAM and even VCM systems [100, 112, 113], in particular SiO_2 based devices [86]. Thus, environmental electron microscopy should be considered for further research in more realistic conditions.

3.2 In-situ spectroscopy

Besides monitoring the filament growth by electron microscopy, in-situ spectroscopy would also be highly desirable. However, most spectroscopic techniques like X-ray photoelectron spectroscopy [86] (XPS) or X-ray absorption spectroscopy [95] (XAS) require large device areas (in the order of ≈ 50 μm × 50 μm for example) and are generally not sensitive enough to study the formation of a filament with an area of $\pi(5\text{ nm})^2 \approx 100\text{ nm}^2$. In the case of XPS, ultra-high-vacuum conditions are required and the X-rays can interact with the switching material and cations as well.

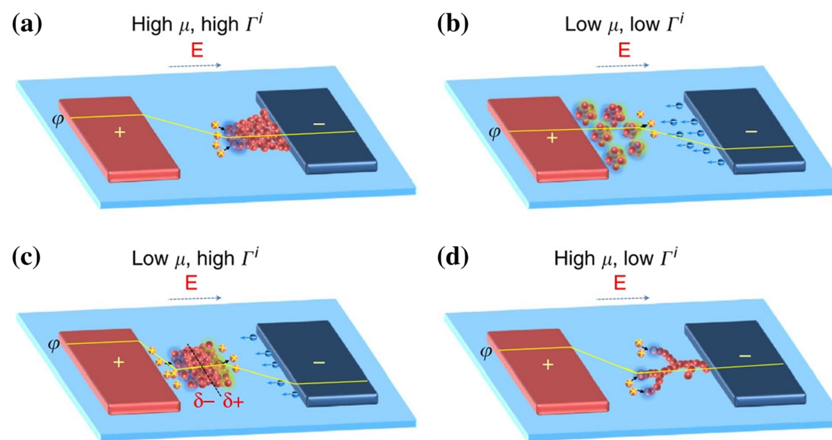


Fig. 8 Model to explain the effective growth direction of the filament and the filament shape depending on the redox rate Γ^i and ion mobility μ of a particular ion i (i.e. Ag^+ or OH^-). (**a**) For a high mobility and high redox rate, a thick filament grows from the inert electrode towards the active electrode. (**b**) In case both mobility and redox rate are small, the nanoparticles intrusion is only a few nanometer while the ions are sufficiently fast reduced by electrons. (**c**) For low mobility and a high redox rate, larger clusters are formed within the oxide and appear to migrate while the driving force is applied. (**d**) For a high mobility but low redox rate, a thin filament dendrite is formed growing again from the inert electrode towards the active electrode. Reprinted by permission from Macmillan Publishers Ltd.: Nature Communication, Ref. [110], copyright 2014

Recently, Di Martino et al. reported on a new spectroscopic technique, namely Nanoscale Plasmon-Enhanced Spectroscopy (NPES), which allows study of the switching process in ambient conditions by the interaction of incident light with the filament and electrodes which form a plasmonic system [114]. These interactions affect the spectra of the backscattered light and are advantageously very sensitive to atomic reconfigurations in the switching gap. Another advantage of this technique is that nanoscale vertical crossbar structures, similar to those in practical memory arrays, can be analysed with a simple measurement setup. The authors could in-situ probe the resistive switching of an $Ag/SiO_2/Au$ device and the results indicate that filament particles remain in the gap during reset and the filament can grow at different positions from cycle to cycle. However, the drawback of the technique is that the interpretation of the backscattered spectra is challenging as it is not a direct imaging of the filament within the insulator. The choice of the electrodes is also limited to materials (like Au and Ag) which allow sufficient interactions with the incident light.

3.3 Impedance spectroscopy

Impedance spectroscopy (IS) is a simple but powerful electrical method that has been extensively used to investigate electrochemical systems, such as batteries, electroplating, corrosion, etc. [115]. In impedance spectroscopy the characteristics of interfaces and electrolytes can be equivalent to electrical circuits of capacitor, resistor and inductor combination [116]. In recent years this non-destructive method has been widely employed to explore the materials and electrical properties of resistive switching devices and numerous meaningful results have been obtained including: a percolation network identified in a Ag/a-Si CBRAM [117], a layered electrolyte with high and low doped region found in aAg/Ge_xSe_y CBRAM [118], and a filament model observed for a TiO_2 based OxRAM [119].

The impedance response of Cu-SiO_2 CBRAM was also reported in [57]. Figure 9(a) shows the IS results of as-fabricated Cu-SiO_2 CBRAM devices with different sizes [57]. The as-fabricated devices were not being electrically switched; thus it is basically a well preserved MIM capacitor with no physical damages in the dielectric layer. The IS results are presented in a Cole-Cole plot format, in which the abscissa is the real part and the ordinate is the imaginary part of the measured impedance. As shown in Fig. 9(a), the experimental results (symbols) are well fitted to a parallel RC network (red lines). The extracted resistance and capacitance values for devices with different sizes are shown in Fig. 9(b). The extracted resistance and capacitance values agree well with the classical resistance (R_{ideal}) and capacitance (C_{ideal}) theory, respectively, i.e., resistance changes inversely with area and capacitance is proportional to area. The extracted dielectric constant is ~5, which is slightly greater than pure bulk SiO_2 (3.9). This could be attributed to the incorporation of Cu atoms into SiO_2 during device fabrication [120]. In addition to as-fabricated devices, programmed devices were also IS characterized. Figure 10 gives the IS results obtained on a $500 \times 500\ \mu m^2$ device that has been programmed into a range of resistance states (from 230 Ω to 55 kΩ) prior to IS measurement. By inputting the programmed resistance and capacitance values of the as-fabricated device into the above parallel RC circuit model, the fitting results can be obtained. As can be seen in Fig. 10, the fitting curves (red lines), which show excellent agreement with the experimental data (symbols), indicate that the device capacitance is independent of

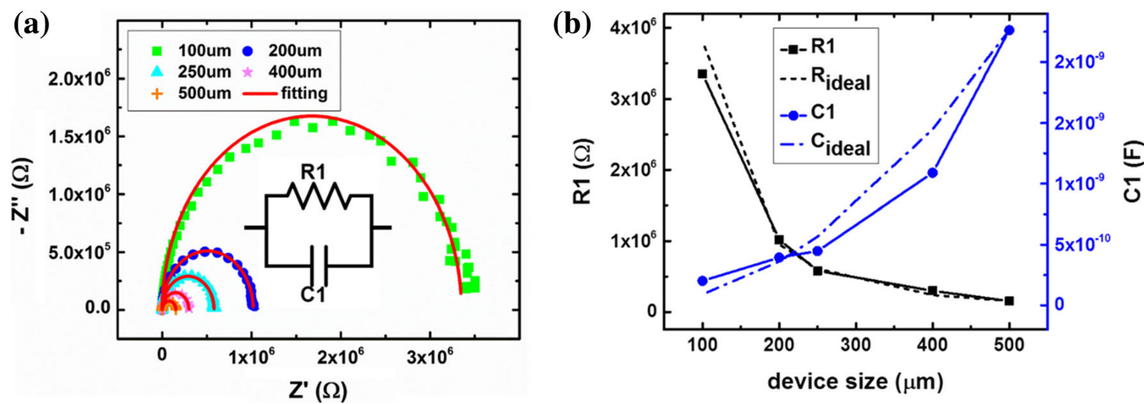


Fig. 9 (a) Impedance spectra of virgin-state Cu/SiO_2 CBRAM with different sizes, symbols are experimental data and solid lines are simulation data, inset picture shows the equivalent RC circuit used for fitting. (b) Extracted resistance and capacitance value vs. device size. © 2016 IEEE. Reprinted with permission from Ref. [57]

resistance states. This non-correlation between resistance and capacitance indicates that the multilevel resistive switching occurs only in localized conducting region, which has negligible size compared to the device. The change of resistance state is attributed to the modulation of filament dimension and/or number.

4 Device performance

4.1 Technology comparison

Research on novel non-volatile memory devices is mainly driven by the slow programming and high voltage of state-of-the-art Flash memories. The aim is to achieve ultra-fast programming times, preferably below 20 ns. Furthermore, reduction of the power consumption is important for mobile applications and logic-in-memory.

NAND Flash is currently dominating the memory market and has replaced NOR Flash in many applications. The difference between NOR and NAND Flash is different circuitry between individual memory cells, making NAND Flash dense and NOR Flash relatively quick to access. To achieve a low programming energy consumption NAND Flash exploits Fowler Nordheim tunneling of electrons into the floating gate [126]. However, to maintain a high retention time of the logic states (in the order of 10 years), programming by Fowler Nordheim tunneling is significantly slower than hot electron injection used for NOR Flash. Nevertheless, NAND and NOR Flash are clearly outperformed by CBRAM and VCM devices in terms of the programming speed (Table 3). Other drawbacks of NAND Flash are high programming voltages (17–19 V [122]) and the inferior endurance of only a few ten thousand cycles [127]. These drawbacks preclude the use of Flash as components emulating binary logic [128] (logic-in-memory) or the use in neuromorphic applications.

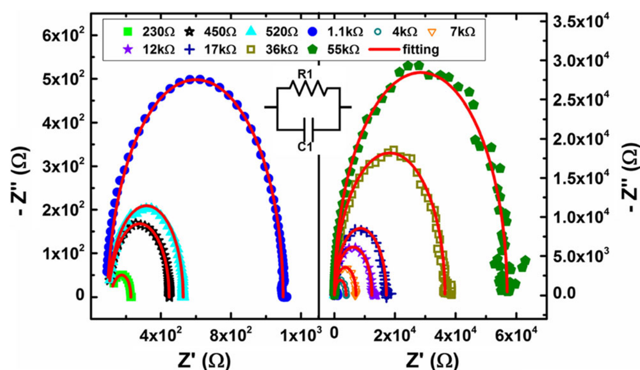


Fig. 10 Impedance spectra of a 500 × 500 μm^2 Cu/SiO_2 CBRAM switched to various resistance states, inset picture shows the equivalent RC circuit used for fitting. © 2016 IEEE. Reprinted with permission from Ref. [57]

Figure 11 gives an overview of the switching times (i.e., programming times) of a variety CBRAM devices. CBRAMs, including SiO_2 based CBRAM, have in common a non-linear relationship between the applied pulse amplitude required to switch the device and the measured switching time (i.e., the transition time between two logic resistance levels). Menzel et al. pointed out that the non-linear voltage-time relationship originates from the exponential term in the equations of electrochemical processes for filament formation, including nucleation, charge transfer and mixed charge/ion drift [124, 129, 130]. This non-linear switching kinetics is expressed by slow switching times for voltages typically below 0.5 to 1 V and fast switching times for voltages typically between 1 V and 5 V. This behaviour is beneficial for practical applications as it avoids unintended switching when small voltages (e.g., read voltage) are applied over an extended time and is the prerequisite for the non-volatile nature of CBRAMs. Figure 11 also indicates that SiO_2 based CBRAM can achieve very fast programming speed with slightly elevated voltage supply.

Apparently, it is difficult to compete against the programming energy of NAND Flash. Generally speaking, experimental values for CBRAM switching energies is around 100 fJ/bit

Table 3 Comparison of critical performance parameters of NAND and NOR Flash, and CBRAM and VCM cells, respectively. For Flash switching speed and energy are usually termed as programming speed and energy, respectively

	Cell size (in F^2)	Switching speed (ns)	Switching energy (pJ/bit)
NAND Flash [121]	4 to 6[2)]	10^4 to 10^5	< 0.01 [122] to 0.1
NOR Flash [121]	6 to 11	10^4	100
CBRAM[1)]	4 to 6 [123]	< 10 [69, 124]	0.1 [122] to 0.7[69]
VCM[1)]	4 to 6 [123]	< 1 [125]	1 [122]

[1)] The footprint $4F^2$ (with F being the minimum feature size) is based on a complementary resistive switching configuration [123]

[2)] The cell size does not consider any overhead circuitry

to 700 fJ/bit, which are usually well below those measured for VCM-type RRAMs [122] (with the exception of e.g. Ref. [125]). Such a small switching energy is notably still about 100 times larger than the energy to operate a two-input logic NAND gate [131] However, Flash is slow which restricts its application as a universal memory that would combine the advantages of static RAM (SRAM), dynamic RAM (DRAM) and non-volatile solid state memories [132]. The energy consumption of 4G DDR4 DRAM (accounting for refresh cycles, background power, etc.) is about 1 to 5 pJ/bit [133] with an access time of 2 to 10 ns [134], compared to ≈ 100 fJ/bit [135, 136] for high-speed SRAMs (with access times below 1 ns). Some of recent works show promisingly low energy consumption of resistive memory in single cell level. Ielmini et al. extrapolated a switching energy of 10 fJ/bit for HfO_2 VCM devices and a switching time of $t_{SET} = 5$ ns [137]. It is reasonable to assume this to be similar for SiO_2 based CBRAMs (assuming V_{SET} = 3.5 V, I_{CC} = 1 μA and t_{SET} = 10 ns for SiO_2, see Fig. 12). The SiO_2 based CBRAM also has been proved to have better performance in low current regime than its counterparts [138]. Nevertheless, above energy extrapolation is overly simplified without including overhead circuits, more works on benchmarking the energy consumption of SiO_2 based CBRAMs and other CBRAMs/OxRAM technology at circuit and/or product level is necessary for systematic understanding of their power consumption attribute.

Compared to competing non-volatile memory technologies such as Spin-Transfer Torque Magnetoresistance RAM (STT-MRAM) CBRAMs including SiO_2 based CBRAM offer a high scalability [134]. Quantized conductance levels measured in SiO_2-based CBRAMs [130, 150] suggest an ultimate scalability reaching the atomic level. The most important advantage of SiO_2 based CBRAM over other CBRAM variants is that the SiO_2 is a well-known material which has been adopted by semiconductor foundries long time ago. Another important advantages of this technology its large resistance window, i.e., the difference between the resistances of the logic states R_{OFF}/R_{ON}, of usually 100 to 10^5. This allows multilevel programming, that is, the storage of multiple bit in one device by a number of distinguishable resistance levels for identification of the logic states. While for many VCM systems R_{OFF}/R_{ON} < 100 and for STT-MRAM the resistance window is even given in percent. As memory cells are integrated in a memory array, it is not sufficient to look at the performance of a single memory cell but also to consider the overall performance when integrated memory cells are interacting. For STT-MRAM and VCM devices, the small resistance window [135] and the variability [134] are problematic. In fact, Calderoni et al. recently reported that the

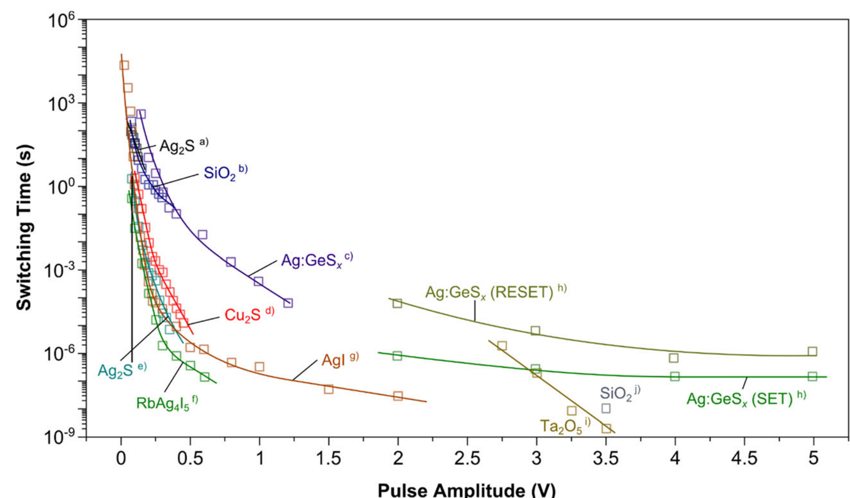


Fig. 11 Switching time versus pulse amplitude of several CBRAM devices. The data is extracted for (**a**) from Ref. [139, 140], (**b**) from Ref. [141], (**c**) from Ref. [142], (**d**) from Ref. [143], (**e**) from Ref. [144], (**f**) from Ref. [145], (**g**) from Ref. [124, 146], (**h**) from Ref. [147], (**i**) from Ref. [148] and (**j**) from Ref. [149]

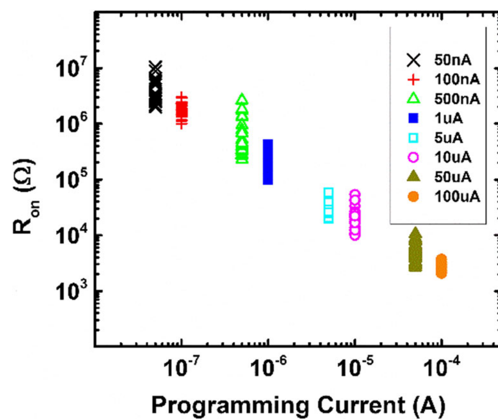


Fig. 12 On-state resistance of three 10 × 10 μm^2 Cu-SiO_2 CBRAM devices cycled for 10 times at each compliance current and the resistance values read at 100 mV. © 2015 IEEE. Reprinted with permission from Ref. [87]

small resistance window of VCM cells may hinder their use in dense memory arrays and therefore SiO_2 based CBRAM becomes more attractive in such applications [151].

4.2 Multi-level cell (MLC) operation

A generic property of resistive switching memory is multilevel operation capability. In multi-level switching, the on-state resistance, R_{ON}, can be modulated by the compliance current during the set operation. This property is also observable in SiO_2 based CBRAM. As shown in Fig. 12, the R_{ON} of CBRAM composed of Cu anode and SiO_2 electrolyte decreases monotonically with the increase of compliance current following the power law,

$$R_{ON} = A/I^n_{\text{prog}}, \quad (4)$$

where A is a constant with a unit of voltage and n is a dimensionless number close to 1. Multilevel programming capability is a critical feature for SiO_2 based CBRAM (as well as all other resistive switching memories) as it enables multibit data storage in single cells, thereby dramatically increasing data storage density.

In recent years, several mechanisms have been proposed to explain the multilevel switching phenomenon. In general, two regimes can be separated at a resistance of approximately 13 kΩ. This is because 13 kΩ is the maximum resistance before the break of a metal-metal contact, i.e., the resistance of a single atom point contact [152]. With a resistance state lower than 13 kΩ, the change of resistance can be explained by lateral filament growth [45]. Once the metallic filament is formed, further reduction causes a growth in filament radius. For higher programming current, more cations are produced and electrodeposited, resulting in a thicker filament. Another possible mechanism for resistance in this regime is based on multiple filaments and the reduction of resistance is attributed to an increase in number of filaments [153]. Of course, it is possible that both mechanisms can be presented and contribute to the low resistance value at the same time. On the other hand, there would be no complete bridging of the electrodes by a filament when the resistance is greater than 13 kΩ. The resistance change in this regime could be due to the modulation of tunneling gap between the filament tip and the electrode [129] and/or the adjustment of width of quantum-point-contact (QPC) like constriction region [154]. Since SiO_2 based CBRAM possess no macroscopic difference from its resistive switching variants, it is believed that the above mechanism also applies. Interestingly, the quantized atomic point contact phenomenon has been found in SiO_2 based CBRAM with a Ag anode [155], in which integer multiples of fundamental conductance ($G_0 = 2e^2h^{-1}$ which is approximately 1/12.9 kΩ) were observed. This resistance discretization serves as another viewpoint to support the metallic filament model for the multilevel resistance states.

4.3 Retention

Retention defines how long the stored information is maintained in a memory cell before a readout error occurs. In Flash memory, retention failure is usually due to the loss of electrons from the floating gate [156]. However, since the information stored in CBRAM is a form of physical filament, the retention of CBRAM is associated with the filament stability and movement of metal atoms away from the filament in the insulating layer. In general, the retention of low resistance state (LRS) is more of an issue than that of high resistance state (HRS) [35, 42]. This is because for a metallic filament formed in the LRS, the large concentration gradient between the filament (Cu or Ag) and its surrounding matrix (SiO_2) may create a significant driving force which assists the dissolution of the filament [157, 158]. Absorbed moisture in the SiO_2 may also play a role in filament stability. Recent cyclic voltammetry (CV) studies show that an electromotive force (emf) exists in the presence of moisture in the SiO_2 switching layer of CBRAM [86], and such emf generates an additional voltage which oxidizes the metallic filament and thereby deteriorates LRS retention [159]. An obvious way to improve the LRS retention is to reduce the diffusion of the metal filament either by doping SiO_2 switching layer with metal ions or by increasing the density of the SiO_2. However, optimized conditions exist for both methods. On one hand, excessive doping tends to lower the off-state resistance to unacceptable levels and under doping can result in poor LRS retention [160]. On the other hand, CBRAM's switching speed slows down and it tends to stuck in LRS if the SiO_2 layer is too dense. The HRS is generally more stable than LRS, even at elevated temperature, since no filamentary structure exists. However, a recent report demonstrated that the HRS resistance tends to decrease at high temperature if the reset operation is incomplete [161]. For

incomplete reset, some filament residues left in the insulating layer, at elevated temperature, these filament residues gradually dissolve into the surrounding oxide matrix which increases the oxide conductivity in a similar way to metal doping. In recent years, excellent retention has been illustrated for CBRAMs with different oxide switching layer [161–163]. CBRAM with a SiO_2 switching layer has been proved to possess good retention performance at high temperature. In a recent study of Cu-SiO_2 (PECVD) CBRAM [138], both HRS and LRS can maintain its programmed value for more than 10^4 s at 150°C without showing obvious degradation.

It should be noted that in certain circumstances bad LRS retention is even more favorable. CBRAMs with poor LRS retention exhibit volatile resistive switching [107, 164–167], in which the filament automatically breaks apart in a short amount of time if the holding voltage is small enough. Volatile switching is a desirable property for many applications such as low refresh dynamic memory, inherent selectors for non-destructive readout of complementary resistive switches [168], short-term-memory (STM) in neuromorphic application [169, 170], or threshold switches operating as selector devices in crosspoint arrays. Recent work on SiO_2 based CBRAM also shows that excellent volatile switching characteristics is achievable if the SiO_2 layer is properly engineered [171], details will be discussed in a later section.

4.4 Endurance

Endurance is determined by how many write-erase cycles a memory cell can perform before failure (stuck bits) occurs. Endurance is associated to programming energy and better endurance is generally achieved from smaller programming energy, i.e. lower programing currents and shorter voltage pulses. Endurance is also influenced by the control of damage during set process, the transient current spike, which usually arises from circuit parasitics, during programming can potentially damage a memory cell in a significant way [172–174]. An integrated 1 T-1R (1 transistor 1 resistive element) configuration effectively prevents this damaging current spike and leads to better endurance performance [175, 176]. The endurance of Cu-SiO_2 CBRAM with 1 T-1R configuration was investigated and reported in [138], where 10^4 cycles of programming/erase was achieved without obvious sign of degradation for both HRS and LRS. This result indicates that SiO_2 based CBRAM has no obvious shortage in terms of endurance performance when compared to its CBRAM counterparts [29, 36, 69, 75, 163, 177–179]. The excellent endurance performance suggests that SiO_2 based CBRAM has good potential to replace Flash memory, DRAM, or become a new type of memory solution in between. The endurance of Cu-SiO_2 CBRAM can be also improved through a better control of anodic metal (Cu or Ag) incorporation during set process. A copper alloy electrode instead of pure copper is reported to be able to limited the rate of Cu/oxide inter-diffusion which effectively eliminates the problem of over incorporation of copper during programming [180].

5 Circuits and applications

5.1 Memory arrays

In order to bring any memory technology to reality, the individual memory cells have to be connected to form arrays. At the array level, it is impossible to correctly store and retrieve information without good cell-to-cell isolation. "Sneak paths" between cells are one of the fundamental causes of reading and writing failures [123]. In order to overcome this challenge, an access device (AD) is typically integrated in series with each memory element. Access devices can be active elements, such as a transistor, or passive elements, such as a diode or other non-linear selector. Thereby, a one transistor and one resistive element (e.g. 1 T-1R) configuration forms the building block of active arrays, whereas a one selector and one resistive element (e.g. 1S-1R) configuration is the key for passive arrays.

5.2 Active arrays

1 T-1R active arrays have been demonstrated by various groups [29, 37, 68, 181–184]. A schematic of such an array is shown in Fig. 13. In this case, the active electrode of the storage cell is connected to the bit-line, the transistor gate is connected to the word-line, the cell's inert electrode and the transistor drain are tied together and the transistor source is connected to a reference voltage (V_s). With this configuration,

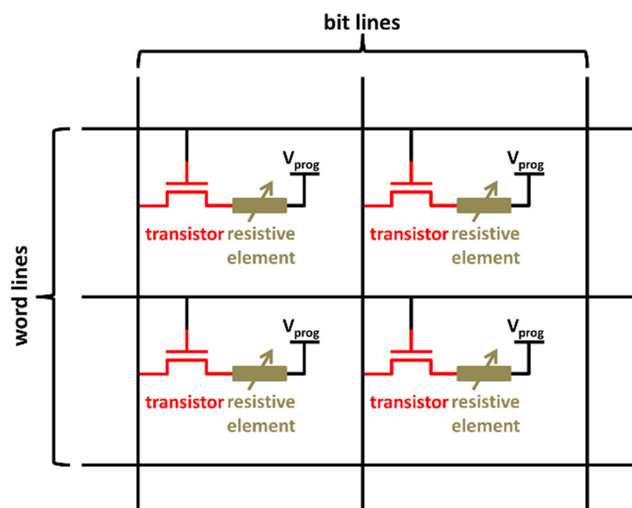


Fig. 13 Configuration of 1 T-1R active array. Each node consists of a resistive switching memory cell and a transistor

the cell can be randomly accessed by applying voltages on the addressed word-line and bit-line simultaneously. In order to program the cell, the bit-line voltage is set higher than the reference voltage (V_s in Fig. 13), while the cell can be erased by reversing the voltage polarity between bit-line and reference node.

Belmonte et al. studied 1 T-1R integrated Cu-SiO_2 CBRAM and compared its performance to Cu-Al_2O_3 CBRAM [138]. They found that CBRAM with a SiO_2 switching layer works better than its counterparts when programming current is small (< 10 μA). For the reason, the authors claimed that less current induced Joule heating is required to activate Cu movement in thin film SiO_2 because it has a higher ion mobility than Al_2O_3. This low power attribute of SiO_2 based CBRAM is desirable for low power applications. The paper also demonstrates other superior performance characteristics of Cu-SiO_2 CRBAM, for example, it can be repeatedly switched with pulses as short as 10 ns and both of its LRS and HRS were well maintained after baking at 150°C for hours. The above results show that CBRAM is promising data storage technology. However, considering that the area of an individual storage unit 1 T-1R is governed not by resistive switching element but by the selecting transistor, which is typically $20F^2$ to $6F^2$, CBRAM with 1 T-1R configuration loses its advantage when competing with NAND Flash ($4F^2$) for massive data storage, especially with the continuous maturation of 3D NAND technology. Nevertheless, due to the low power and fast programming/reading characteristics of 1 T-1R SiO_2 CBRAM, it is still an ideal alternative to NOR Flash for low power embedded system.

5.3 Passive arrays

A passive array differs from active array in that it employs a two terminal passive device instead of transistor to prevent the current sneak path. This passive device is also known as a selector which typically has a non-linear voltage-current relationship. Every selector has a non-zero characteristic voltage which is also known as threshold voltage, below this voltage, the selector is effectively off and the current is small, while above threshold voltage, the selector turns on and the current increases dramatically. Different from memory device, the LRS of selector devices is volatile, which means that it will switch back to HRS automatically once the applied voltage drops below the non-negative threshold value. The building block of passive array contains one resistive element and one selector with a 1S-1R configuration, shown in Fig. 14. Memory cell are connected in series with selector and it can be randomly accessed by applying voltages on corresponding word-line and bit-line. To program an individual cell, the programming voltage is applied to the bit-line while the word-line is grounded. Half the programming voltage is applied to all

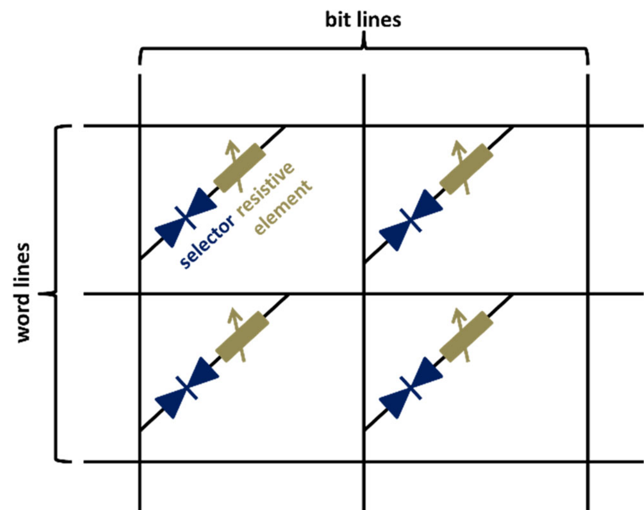


Fig. 14 Configuration of 1S-1R passive array. Each node consists of a resistive switching memory cell and a selector

non-selected lines. The selector's threshold voltage should be higher than half programming voltage but lower than the programming voltage. In this way, only the selected device with full programming voltage can be accessed while the rest of the cells are blocked by their selectors. The main advantage of the 1S-1R approach is that it eliminates the need for 3-terminal transistor, thus the most compact circuit layout ($4F^2$) is achievable. Moreover, a passive array can be stacked to create an ultra-dense 3D crosspoint memory array which may best 3D NAND Flash for massive data storage.

Several types of selectors have been proposed including the chalcogenide based Ovonic switch [185], transition oxide (VO_2 and NbO_2) based metal-insulator transition (MIT) based devices [186, 187], as well as a mixed-ionic-electronic-conduction (MIEC) selector technology [188, 189]. Except for the MIEC selector, the other two selectors (Ovonic, MIT) suffer a high-off state leakage current problem. Since CBRAM is a filamentary technology, the concentration gradient between the metal filament and the surrounding oxide matrix can be gigantic which may allow for fast filament dissolution. A CBRAM can therefore be engineered to be a selector by greatly enhancing the filament dissolution rate. Based on this, a SiO_2 based CBRAM has been fabricated with volatile switching property [55]. Figure 15 shows the typical volatile switching I-V curve of a 5 × 5 um^2 Cu/SiO_2/Pt CBRAM device. The device was swept with a range of compliance currents from 10 nA to 500 μA with a threshold voltage (V_{th}) between 0.5 V and 0.8 V. The LRS is maintained when the voltage is sufficiently large while it turns back to HRS spontaneously when removing the applied voltage. A rectifying ratio as big as 5×10^7 is obtained at ±0.8 V with a compliance current of 500 μA. Such a high rectifying ratio suggests the usage of this device as a sneak path blocking

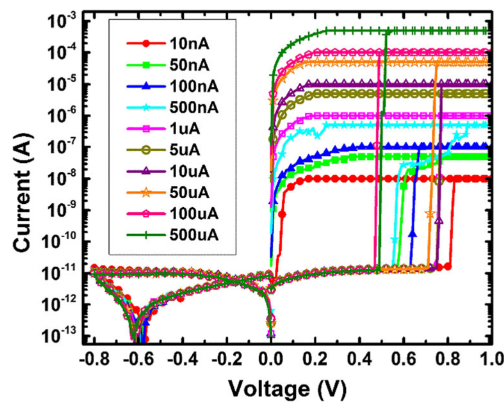


Fig. 15 Typical threshold switching I-V characteristics of Cu/SiO_2/Pt CBRAM. © 2016 IEEE. Reprinted with permission from Ref. [171]

selector. Considering that this device is strongly rectifying only for positive voltage, it would only be suitable for unipolar memories in which programing and erasing occurs at the same voltage polarity. Figure 15 also demonstrate that volatility of this specifically engineered Cu-SiO_2 CBRAM is independent of compliance current up to 500 μA, such high current is more than enough for the programming of phase change memory.

SiO_2 based CBRAM can be also engineered to have an inherent diode in conjunction with memory cell [190]. The contact made between Cu filament and a heavily doped silicon electrode forms a Schottky diode. This unique method provides a simple approach for cell isolation which requires no additional layer. The authors reported that the virgin-state resistance for this device is above 10GΩ, which is sufficient to prevent 'sneak' current flow in a sub-array. Upon switching, the reverse bias blocking resistance is approximately 300MΩ at half read voltage magnitude (−0.25 V) which is large enough to ensure correct reading operations. It should be mentioned that the diode's reverse leakage current was proportional to the LRS resistance as both are related to metal filament diameter. It is important that the device can be reset by negative voltage (about −4.6 V), which is a fundamental property required for it to be used in bipolar memory cells.

5.4 Neuromorphic systems

Bio-inspired neuromorphic computation has been gaining popularity as an alternative to the von Neumann based computing architecture for power efficient artificial intelligence applications. In human brain, there are about 20 billion neurons [191] connected together forming a gigantic neural network for learning and task operations. For every connection, there is a synapse which transmits signals between adjacent neurons. Biological learning occurs through gradually and continuously changing the strength (conductivity) of these synapses [192]. In order to emulate biological synapse, the electronic synapse must possess a similar plasticity, i.e., a gradual change of resistance. A CMOS based electronic synapse has been developed which contains tens of transistors and capacitors [193]. Given the number of synapses in a typical neuromorphic system, the chip's area cost would be unaffordable. In this respect, a two terminal RRAM based electronic synapse is highly desirable due to their structural simplicity and excellent scalability. Several OxRAM and CBRAM technologies have been demonstrated to be capable of changing resistance incrementally [74, 194–196]. CBRAM with a thermally doped SiO_2 layer also show promising synaptic behavior [55] and its inherent CMOS compatibility eases the adoption by current semiconductor foundries.

The resistance plasticity of Cu/Cu: SiO_2 CBRAM was characterized by quasi-static DC and transient pulses in [55]. As shown in Fig. 16(a), the resistance of the device decreases with an increase in positive bias, this represents the *potentiation* (P) in the synapse. Conversely, the resistance of a low resistance (programmed) device increases with an increase in negative bias, which corresponds to the *depression* (D) in a biological synapse (Fig. 16(b)). The ability to produce both potentiation and depression in Cu/Cu: SiO_2 CBRAM favors both online and offline training. Interestingly, all of the discrete incremental curves are generally contained within the dotted curve obtained from a full range voltage sweep, this property indicates that a complete sweep is equivalent to a combination of discrete sweeps. This combinational property is especially useful for learning speed adjustment. In addition to DC, the device resistance is also tunable with electric pulses, which is a more realistic evaluation of the synaptic performance. In pulse testing, groups of potentiating or depressing pulses were applied with 20 mV difference between two consecutive groups. In every pulse group, a pulse-train of 10 identical 10 μs pulses are applied. Figure 17(a) and (b) show the experimental waveforms for a sequence of potentiation and depression pulses, respectively. The amplitudes of applied pulse (V1) are differentiated by colored curves, while the black curves (V2) are the response pulses which represents the voltages across a serially connected resistor. Therefore, the resistance change of the CBRAM can be extrapolated from this voltage divider. It is observable that the magnitude of response pulses is continuously increased (or decreased) with the number of programming pulses, which implies that the device resistance is gradually changing. The calculated resistance ranges from 3 kΩ and 20 kΩ. This wide resistance window and dense distribution indicate that Cu/Cu: SiO_2 CBRAM is suitable for neuromorphic application. Furthermore, the tuning voltage is around 1 V for both potentiation and depression. This voltage is compatible with the supply voltage of most current CMOS chips, thereby eliminating the need for charge pumps.

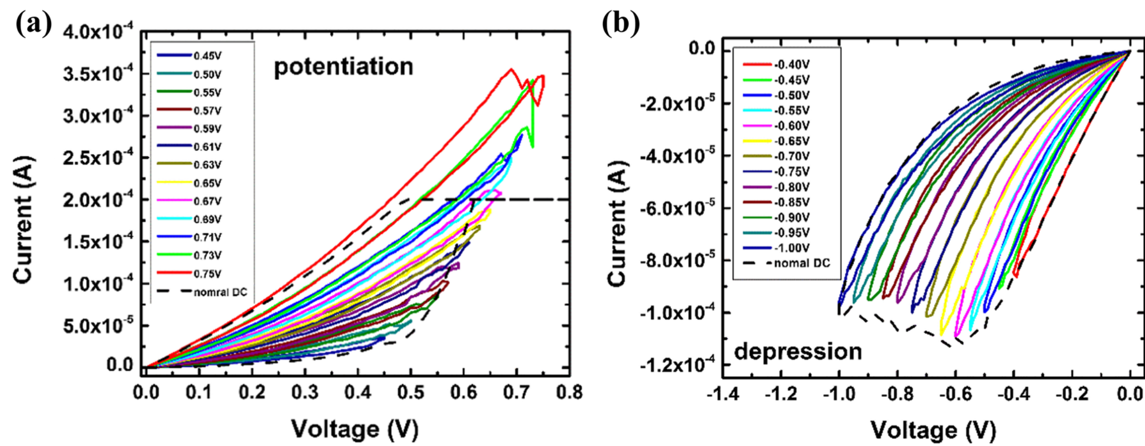


Fig. 16 DC characteristic of thermally doped Cu/Cu: SiO_2 CBRAM device showing gradual resistance change. (**a**) Potentiation, graduate resistance decrease, (**b**) Depression, gradual resistance increase [55]. © IOP Publishing. Reproduced with permission. All rights reserved

5.5 Radiation tolerant memory

Energetic particles, such as photons, electrons and protons, generate electron-hole pairs (ehps) when striking at solid-state materials. This effect causes total ionizing dose (TID) damage [197] which may degrade the performance of electronic devices over time. Since TID generally leads to excess charged defect buildup in solid state materials, conventional charge-storage based NVMs, such as Flash and EEPROM, are not desirable for medical electronics and space systems which are usually exposed to high doses of ionizing radiation [198]. Therefore finding aradiation tolerant NVM is critical for reliable operation of those kinds of applications. Owing to the fact that the operation of resistive switching memory is based on physical filament instead of charge, it has better radiation immunity than charge-storage based NVMs. Extensive studies have been performed to assess the TID response of resistive switching devices including cation based CBRAM [4, 199–202] and anion based OxRAM [203–206].

Chen et al. produced a comprehensive study of TID response of Cu-SiO_2 based CBRAM [87]. The devices were step exposed to ^{60}Co gamma-rays with a maximum TID of 7.1 Mrad(SiO_2). This TID dosage is well above the common dosage used for device sterilization in hospitals. Figure 18 illustrates the I-V curves of as-fabricated Cu-SiO_2 CBRAM before and after TID exposure. Three $10 \times 10\ \mu m^2$ and three $100 \times 100\ \mu m^2$ devices were tested. The voltage sweeps stopped at 100 mV to avoid any oxidization of Cu electrode, which eliminates the resistance change of SiO_2 caused by Cu incorporation. In addition, the TID effects on switched devices were also assessed. A set of ten $10 \times 10\ \mu m^2$ devices were cycled 10 times at different dosage. Figure 19 plots the cumulative probability distribution of HRS and LRS respectively. Based on the results shown in Figs. 18 and 19, the gamma-ray irradiation has negligible impacts on the resistances of as-fabricated device, its HRS as well as LRS.

The TID impacts on multilevel switching were also investigated since the reliability of intermediate resistance states is

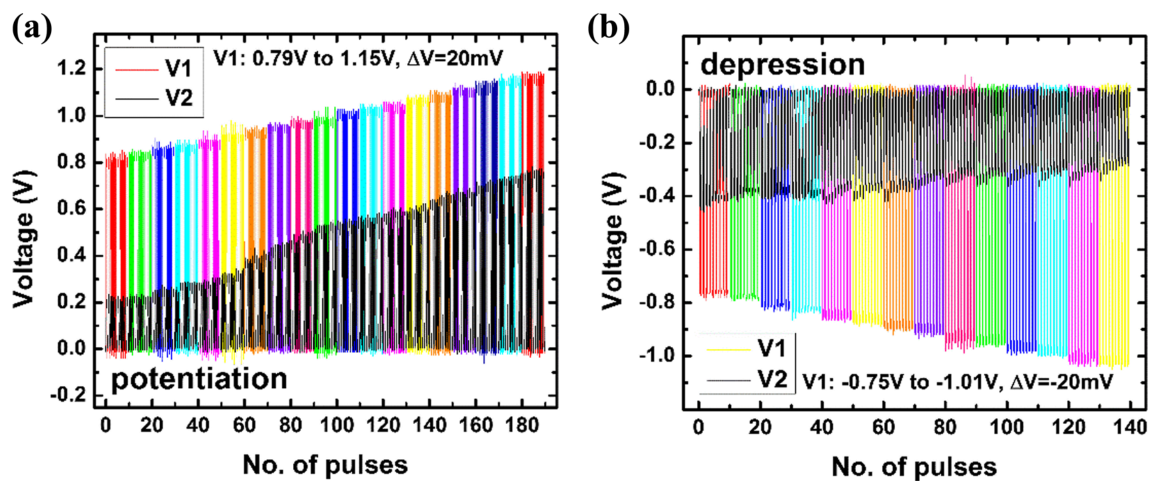


Fig. 17 Electrical pulse characterization of thermally doped Cu/Cu: SiO_2 CBRAM. (**a**) Potentiation, (**b**) Depression [55]. © IOP Publishing. Reproduced with permission. All rights reserved

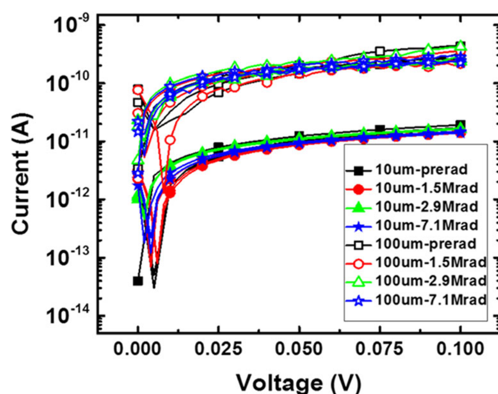


Fig. 18 I-V characteristics of virgin Cu-SiO_2 CBRAM with a size of 10 μm and 100 μm at different TID levels. © 2015 IEEE. Reprinted with permission from Ref. [87]

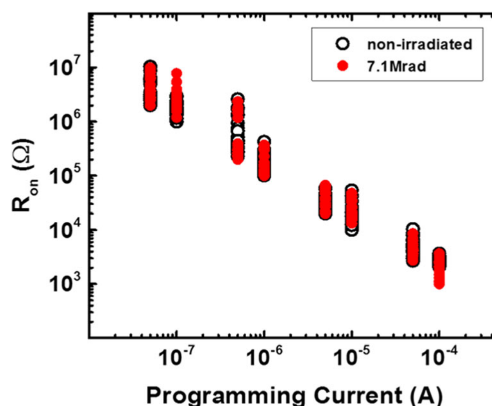


Fig. 20 TID impacts on multilevel programmability of Cu-SiO_2 CBRAM, comparison of R_{on} vs. I_{prog} before and after 7.1 Mrad(SiO_2) TID. © 2015 IEEE. Reprinted with permission from Ref. [87]

vital for multilevel cell (MLC) NVMs used for neuromorphic computing. In [87], three 10 × 10 μm^2 devices were switched over a range of compliance currents before and after gamma-ray exposure. The results are shown in Fig. 20. Again, no significant variation can be observed between irradiated and non-irradiated devices as both of them show similar the power-law dependence and the multilevel resistance curves are well overlapped with each other.

The authors believe that the ionizing radiation immunity of the HRS in SiO_2 based CBRAM devices may be attributed to the absence of photo-doping effects in e-beam evaporated SiO_2. The photo-doping phenomenon in chalcogenide glasses has been widely observed and is believed to be triggered by the interaction between active electrode (Ag or Cu) and the photo-generated electron-hole pairs (ehps). Since the bandgap of SiO_2 (~ 9 eV) is much larger than Ge_xSe_{1-x} (< 2 eV), considerably fewer ehps will be created in SiO_2 which reduces the rate of this interaction process. Moreover, different carrier traps present in SiO_2 as compared to the chalcogenide glasses may be another reason. DFT calculations predics that the majority trap in chalcogenide glasses is electron trap [207] while positively charged hole traps generally exist in SiO_2. The positively charged hole traps would repel rather than attract Cu ions which prevents its diffusion into SiO_2.

Besides the aforementioned applications, recent studies indicate that SiO_2 based CBRAM also holds great potentials for applications in another novel computing paradigm known as logic-in-memory [208, 209]. Logic-in-memory is a concept where a single device arranged in a dense array is capable to perform both logic and memory operations. A major benefit of this concept is that the energy wasted by interconnects during data transfer can be saved.

6 Challenges and perspectives

Even though significant progress has been achieved in SiO_2 based CBRAM, the omission of potential problems may greatly slow down its commercialization speed. For example, are those observed characteristics and obtained conclusions

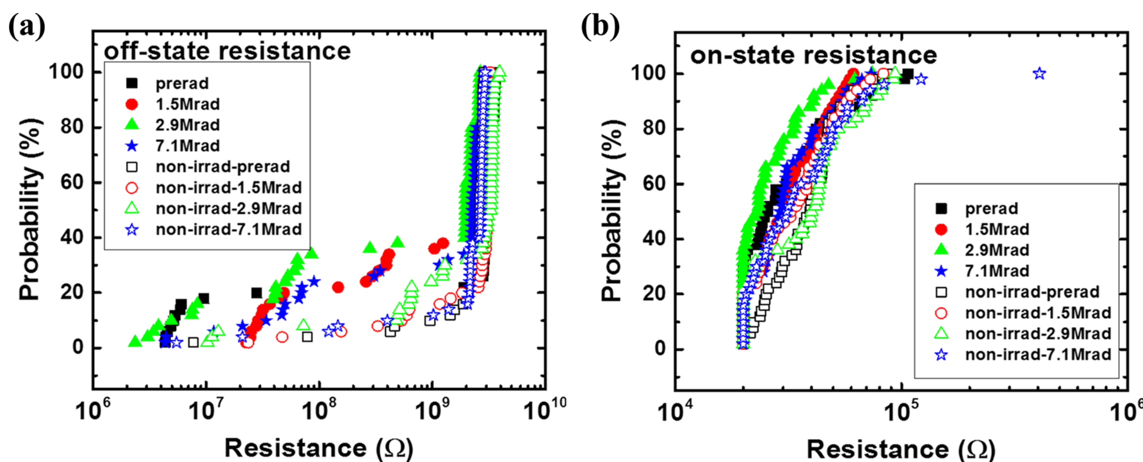


Fig. 19 TID impacts on ON- and OFF-state of Cu-SiO_2 CBRAM. (**a**) Cumulative probability of ON-state resistance at different TID, (**b**) cumulative probability of OFF-state resistance at different TID. © 2015 IEEE. Reprinted with permission from Ref. [87]

still valid for nanoscale devices? In such small scale, the filament size may be comparable to the size of device or even the entire device is a filament. The impact of Joule heating may be amplified and cannot be neglected in tightly enclosed nanostructure. Also, a slight difference in filament morphology (contact angle, number connecting atoms and branches) could lead to huge resistance variation at nanoscale, this problem is extremely fatal to MLC or neuromorphic applications in which a tight distribution of multilevel states is particularly required.

Apart from device variation, the process integration of SiO_2 based CBRAM is also a great challenge. Although Cu interconnect has been widely adopted in current back-end-of-line (BEOL) process and Cu diffusion can be well controlled by diffusion barriers, the migration of Cu can still happen between the CBRAM's side-wall and isolation layer where the diffusion barrier doesn't exist. This migration process may be even accelerated by the high surface energy of grain boundaries which potentially threats the device performance. In addition, compatible selector for this CBRAM type is still unavailable. An ideal selector should have low HRS current leakage, high endurance, large ON/OFF ratio, bipolar switchability and process compatibility. Furthermore, metal doping of SiO_2 is required in certain circumstances, thus, the thermal budget for the periphery circuits fabrication should reconsidered to avoid undesired transistor characteristics.

7 Conclusions

In this review we have examined Conductive Bridging Random Access Memory based on silicon dioxide films. CBRAM in general has shown considerable promise as non-volatile memory for devices powered by small batteries, such as wearable electronics and elements in the Internet of Things, because of its low voltage and low current operation. To date, most CBRAM development has involved higher chalcogenide materials, due to the attainable high metal ion mobility and consequent fast switching, but the process compatibility and ubiquity of silicon dioxide in CMOS integrated circuits increases the acceptability of the technology in production facilities, including semiconductor foundries.

Despite the operational similarities of oxide-based CBRAM with other variants of the technology, there are some fundamental differences. SiO_2 is not a "classical" electrolyte and metal ion mobility in bulk material is low compared to higher chalcogenide glasses. However, very thin films (in the order of a few nm to a few tens of nm thickness between electrodes) exhibit unusually high Cu ion mobility and this allows devices to switch in timescales that are acceptable for many NVM applications. The role of OH^- ions as counter-charge in the electrochemical reaction process is also interesting and is not generally considered in devices based on higher chalcogenide electrolytes. In addition, the shape of the filament and apparent growth direction, as shown by in-situ SEM analysis, can be different than chalcogenide-based devices due to the way that the metal ions supply the filament growth but electrical characterization, particularly impedance spectroscopy, has confirmed the general filamentary model for these structures.

Oxide based CBRAM devices exhibit sub-1 V switching and compare favorably with Flash memory in terms of speed and switching energy. The low energy and non-volatility of the technology allows it to be used for compact computation/logic functions as well as storage. They are capable of being programmed over a wide range of currents which in turn provide a considerable series of on-state resistance values. This allows SiO_2-based CBRAM to not only be used in multi-level cell storage but also in neuromorphic applications in which the controlled gradual decrease and increase in resistance can be used to represent potentiation and depression respectively. Resistance control is possible in both active and passive arrays, the latter being possible via an inherent diode selector device. Finally, the impressive radiation tolerance of the technology allows it to be used not only in aerospace and deep space missions but also in medical device applications where gamma ray sterilization or therapeutic radiation would otherwise adversely affect Flash memory devices.

Acknowledgements This work was funded in part by the Air Force Research Laboratory under grant no. FA9453-13-1-0288 (H.J.B.) and by the Defense Threat Reduction Agency under grant no. HDTRA1-11-1-005 (H.J.B. and M.N.K.). S.T. acknowledges funding by a DFG research fellowship under grant TA 1122/1-1. M.N.K. would also like to acknowledge the support of Axon Technologies Corp.

References

1. E. Grochowski, R.D. Halem, Technological impact of magnetic hard disk drives on storage systems. IBM Syst. J. **42**, 338–346 (2003)
2. P. Desnoyers, Empirical evaluation of NAND flash memory performance. ACM SIGOPS Oper. Syst. Rev. **44**, 50–54 (2010)
3. L. Crippa, R. Micheloni, 3D Charge Trap NAND Flash Memories, in *3D Flash Memories*, ed: Springer, 2016, pp. 85–127.
4. Y. Gonzalez-Velo, H. J. Barnaby, M. N. Kozicki, C. Gopalan, and K. Holbert, Total ionizing dose retention capability of conductive bridging random access memory. Electron Device Lett., IEEE, vol. 35, pp. 205–207, 2014.
5. J. Simmons, R. Verderber, New thin-film resistive memory. Radio Electron. Eng. **34**, 81–89 (1967)
6. G. Dearnaley, A. Stoneham, D. Morgan, Electrical phenomena in amorphous oxide films. Rep. Prog. Phys. **33**, 1129 (1970)
7. D. Oxley, Electroforming, switching and memory effects in oxide thin films. Act. Passive Electron. Compon. **3**, 217–224 (1977)
8. R. Waser, M. Aono, Nanoionics-based resistive switching memories. Nat. Mater. **6**, 833–840 (2007)

9. I. Valov, R. Waser, J.R. Jameson, M.N. Kozicki, Electrochemical metallization memories—fundamentals, applications, prospects. Nanotechnology **22**, 254003 (2011)
10. R. Waser, R. Dittmann, G. Staikov, K. Szot, Redox-based resistive switching memories–nanoionic mechanisms, prospects, and challenges. Adv. Mater. **21**, 2632–2663 (2009)
11. H. Pagnia, N. Sotnik, Bistable switching in electroformed metal–insulator–metal devices. Phys. Status Solidi (a) **108**, 11–65 (1988)
12. J.J. Yang, D.B. Strukov, D.R. Stewart, Memristive devices for computing. Nat. Nanotechnol. **8**, 13–24 (2013)
13. A. Beck, J. Bednorz, C. Gerber, C. Rossel, D. Widmer, Reproducible switching effect in thin oxide films for memory applications. Appl. Phys. Lett. **77**, 139–141 (2000)
14. D. Ielmini, C. Cagli, F. Nardi, Resistance transition in metal oxides induced by electronic threshold switching. Appl. Phys. Lett. **94**, 063511 (2009)
15. S. Yu, X. Guan, H.-S.P. Wong, Conduction mechanism of TiN/HfOx/Pt resistive switching memory: a trap-assisted-tunneling model. Appl. Phys. Lett. **99**, 063507 (2011)
16. R. Fang, W. Chen, L. Gao, W. Yu, S. Yu, Low-temperature characteristics of HfO x-based resistive random access memory. IEEE Electron. Device Lett. **36**, 567–569 (2015)
17. L. Goux, P. Czarnecki, Y.Y. Chen, L. Pantisano, X. Wang, R. Degraeve, et al., Evidences of oxygen-mediated resistive-switching mechanism in TiN\ HfO2\ Pt cells. Appl. Phys. Lett. **97**, 243509 (2010)
18. M.-J. Lee, C.B. Lee, D. Lee, S.R. Lee, M. Chang, J.H. Hur, et al., A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5− x/TaO2− x bilayer structures. Nat. Mater. **10**, 625–630 (2011)
19. Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, et al., Highly reliable TaOx ReRAM and direct evidence of redox reaction mechanism. in *2008 I.E. International Electron Devices Meeting*, 2008, pp. 1–4.
20. R.J. Kamaladasa, A.A. Sharma, Y.-T. Lai, W. Chen, P.A. Salvador, J.A. Bain, et al., In situ TEM imaging of defect dynamics under electrical bias in resistive switching rutile-TiO 2. Microsc. Microanal. **21**, 140–153 (2015)
21. J.J. Yang, M.D. Pickett, X. Li, D.A. Ohlberg, D.R. Stewart, R.S. Williams, Memristive switching mechanism for metal/oxide/metal nanodevices. Nat. Nanotechnol. **3**, 429–433 (2008)
22. M. Kubicek, R. Schmitt, F. Messerschmitt, J.L. Rupp, Uncovering two competing switching mechanisms for epitaxial and ultrathin strontium Titanate-based resistive switching bits. ACS Nano **9**, 10737–10748 (2015)
23. F. Messerschmitt, M. Kubicek, S. Schweiger, J.L. Rupp, Memristor kinetics and diffusion characteristics for mixed anionic-electronic SrTiO3-δ bits: the memristor-based Cottrell analysis connecting material to device performance. Adv. Funct. Mater. **24**, 7448–7460 (2014)
24. K. Szot, W. Speier, G. Bihlmayer, R. Waser, Switching the electrical resistance of individual dislocations in single-crystalline SrTiO3. Nat. Mater. **5**, 312–320 (2006)
25. D.-H. Kwon, K.M. Kim, J.H. Jang, J.M. Jeon, M.H. Lee, G.H. Kim, et al., Atomic structure of conducting nanofilaments in TiO2 resistive switching memory. Nat. Nanotechnol. **5**, 148–153 (2010)
26. H.-S.P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, et al., Metal–oxide RRAM. Proc. IEEE **100**, 1951–1970 (2012)
27. M. N. Kozicki, M. Mitkova, and I. Valov, Electrochemical metallization memories, *Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications,* pp. 483–514, 2016.
28. I. Valov and W. D. Lu, Nanoscale electrochemistry using dielectric thin films as solid electrolytes. Nanoscale, 2016.
29. C. Gopalan, Y. Ma, T. Gallo, J. Wang, E. Runnion, J. Saenz, et al., Demonstration of conductive bridging random access memory (CBRAM) in logic CMOS process. Solid State Electron. **58**, 54–61 (2011)
30. J. Jameson, P. Blanchard, C. Cheng, J. Dinh, A. Gallo, V. Gopalakrishnan, et al., Conductive-bridge memory (CBRAM) with excellent high-temperature retention. in *2013 I.E. International Electron Devices Meeting, IEDM 2013*, 2013.
31. G. Raghavan, C. Chiang, P.B. Anders, S.-M. Tzeng, R. Villasol, G. Bai, et al., Diffusion of copper through dielectric films under bias temperature stress. Thin Solid Films **262**, 168–176 (1995)
32. M. Mitkova, M. Kozicki, Silver incorporation in Ge–Se glasses used in programmable metallization cell devices. J. Non-Cryst. Solids **299**, 1023–1027 (2002)
33. M. N. Kozicki, C. Gopalan, M. Balakrishnan, M. Park, M. Mitkova, Nonvolatile memory based on solid electrolytes, in *Non-Volatile Memory Technology Symposium, 2004*, 2004, pp. 10–17.
34. C. Schindler, M. Meier, R. Waser, M. Kozicki, Resistive switching in Ag-Ge-Se with extremely low write currents, in *Non-Volatile Memory Technology Symposium, 2007. NVMTS'07*, 2007, pp. 82–85.
35. M. Kund, G. Beitel, C.-U. Pinnow, T. Rohr, J. Schumann, R. Symanczyk, et al., Conductive bridging RAM (CBRAM): an emerging non-volatile memory technology scalable to sub 20 nm, in *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.*, 2005.
36. M.N. Kozicki, M. Park, M. Mitkova, Nanoscale memory elements based on solid-state electrolytes. IEEE Trans. Nanotechnol. **4**, 331–338 (2005)
37. N.E. Gilbert, M.N. Kozicki, An embeddable multilevel-cell solid electrolyte memory array. IEE J. Solid-State Circuits **42**, 1383–1391 (2007)
38. R. Symanczyk, M. Balakrishnan, C. Gopalan, T. Happ, M. Kozicki, M. Kund, et al., Electrical C aracteri < ation of solid state 8onic memory elements, 2003
39. M.N. Kozicki, M. Mitkova, Mass transport in chalcogenide electrolyte films–materials and applications. J. Non-Cryst. Solids **352**, 567–577 (2006)
40. M. Kozicki, M. Mitkova, M. Park, M. Balakrishnan, C. Gopalan, Information storage using nanoscale electrodeposition of metal in solid electrolytes. Superlattice. Microst. **34**, 459–465 (2003)
41. M. N. Kozicki, M. Balakrishnan, C. Gopalan, C. Ratnakumar, M. Mitkova, Programmable metallization cell memory based on Ag-Ge-S and Cu-Ge-S solid electrolytes, in *Symposium Non-Volatile Memory Technology 2005.*, 2005, pp. 7–89.
42. R. Symanczyk, R. Bruchhaus, M. Kund, Investigation of the reliability behavior of conductive-bridging memory cells. IEEE Electron Device Lett. **30**, 876–878 (2009)
43. D. Kamalanathan, U. Russo, D. Ielmini, M.N. Kozicki, Voltage-driven on–off transition and tradeoff with program and erase current in programmable metallization cell (PMC) memory. IEEE Electron Device Lett. **30**, 553–555 (2009)
44. R. Bruchhaus, M. Honal, R. Symanczyk, M. Kund, Selection of optimized materials for CBRAM based on HT-XRD and electrical test results. J. Electrochem. Soc. **156**, H729–H733 (2009)
45. U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, M.N. Kozicki, Study of multilevel programming in programmable metallization cell (PMC) memory. IEEE Trans. Electron Devices **56**, 1040–1047 (2009)
46. M. Balakrishnan, M. Kozicki, C. Gopalan, and M. Mitkova, Germanium sulfide-based solid electrolytes for non-volatile memory, in *63rd Device Research Conference, DRC'05*, (2005)
47. D. Kamalanathan, S. Baliga, S. C. P. Thermadam, M. Kozicki, ON state stability of programmable metalization cell (PMC) memory, in *Non-Volatile Memory Technology Symposium, 2007. NVMTS'07* (2007), pp. 91–96

48. C.-J. Kim, S.-G. Yoon, K.-J. Choi, S.-O. Ryu, S.-M. Yoon, N.-Y. Lee, et al., Characterization of silver-saturated Ge-Te chalcogenide thin films for nonvolatile random access memory. J. Vac. Sci. Technol. B **24**, 721–724 (2006)
49. R. Pandian, B.J. Kooi, G. Palasantzas, J.T. De Hosson, A. Pauza, Polarity-dependent reversible resistance switching in Ge–Sb–Te phase-change thin films. Appl. Phys. Lett. **91**, 152103 (2007)
50. I. Stratan, D. Tsiulyanu, I. Eisele, A programmable metallization cell based on Ag-As2S3. J. Optoelectron. Adv. Mater. **8**, 2117–2119 (2006)
51. P. Van Der Sluis, Non-volatile memory cells based on ZnxCd1-xS ferroelectric Schottky diodes. Appl. Phys. Lett. **82**, 4089–4091 (2003)
52. S.P. Thermadam, S. Bhagat, T. Alford, Y. Sakaguchi, M. Kozicki, M. Mitkova, Influence of Cu diffusion conditions on the switching of Cu–SiO 2-based resistive memory devices. Thin Solid Films **518**, 3293–3298 (2010)
53. S. Tappertzhofen, H. Mündelein, I. Valov, R. Waser, Nanoionic transport and electrochemical reactions in resistively switching silicon dioxide. Nanoscale **4**, 3040–3043 (2012)
54. C. Schindler, S.C.P. Thermadam, R. Waser, M.N. Kozicki, Bipolar and unipolar resistive switching in Cu-doped SiO 2. IEEE Trans. Electron Devices **54**, 2762–2768 (2007)
55. W. Chen, R. Fang, M.B. Balaban, W. Yu, Y. Gonzalez-Velo, H.J. Barnaby, et al., A CMOS-compatible electronic synapse device based on Cu/SiO2/W programmable metallization cells. Nanotechnology **27**, 255202 (2016)
56. M. Balakrishnan, S. C. P. Thermadam, M. Mitkova, M. N. Kozicki, A low power non-volatile memory element based on copper in deposited silicon oxide, in *2006 7th Annual Non-Volatile Memory Technology Symposium* (2006), pp. 104–110
57. W. Chen, H. Barnaby, M. Kozicki, Impedance spectroscopy of programmable metallization cells with a thin SiO 2 switching layer. IEEE Electron Device Lett. **37**, 576–579 (2016)
58. S. Tappertzhofen, S. Menzel, I. Valov, R. Waser, Redox processes in silicon dioxide thin films using copper microelectrodes. Appl. Phys. Lett. **99**, 203103 (2011)
59. S. Manhart, Memory switching in SiO films with Ag and Co electrodes. J. Phys. D. Appl. Phys. **6**, 82 (1973)
60. T. Tsuruoka, K. Terabe, T. Hasegawa, M. Aono, Temperature effects on the switching kinetics of a Cu–Ta2O5-based atomic switch. Nanotechnology **22**, 254013 (2011)
61. T. Sakamoto, K. Lister, N. Banno, T. Hasegawa, K. Terabe, M. Aono, Electronic transport in Ta2O5 resistive switch. Appl. Phys. Lett. **91**, 092110 (2007)
62. Y. Tsuji, T. Sakamoto, N. Banno, H. Hada, M. Aono, Off-state and turn-on characteristics of solid electrolyte switch. Appl. Phys. Lett. **96**, 023504 (2010)
63. T. Sakamoto, N. Banno, N. Iguchi, H. Kawaura, H. Sunamura, S. Fujieda, et al., A Ta 2 O 5 solid-electrolyte switch with improved reliability, in *2007 I.E. Symposium on VLSI Technology* (2007), pp. 38–39.
64. N. Banno, T. Sakamoto, S. Fujieda, M. Aono, On-state reliability of solid-electrolyte switch, in *2008 I.E. International Reliability Physics Symposium* (2008), pp. 707–708.
65. C. Gopalan, M. Kozicki, S. Bhagat, S.P. Thermadam, T. Alford, M. Mitkova, Structure of copper-doped tungsten oxide films for solid-state memory. J. Non-Cryst. Solids **353**, 1844–1848 (2007)
66. Y. Li, S. Long, Q. Liu, Q. Wang, M. Zhang, H. Lv, et al., Nonvolatile multilevel memory effect in Cu/WO3/Pt device structures. Phys. Status Solidi (RRL)-Rapid Res. Lett. **4**, 124–126 (2010)
67. M.N. Kozicki, C. Gopalan, M. Balakrishnan, M. Mitkova, A low-power nonvolatile switching element based on copper-tungsten oxide solid electrolyte. IEEE Trans. Nanotechnol. **5**, 535–544 (2006)
68. L. Goux, K. Sankaran, G. Kar, N. Jossart, K. Opsomer, R. Degraeve, et al., Field-driven ultrafast sub-ns programming in WAl 2 O 3 TiCuTe-based 1T1R CBRAM system, in *VLSI Technology (VLSIT), 2012 Symposium on* (2012), pp. 69–70.
69. A. Belmonte, W. Kim, B. Chan, N. Heylen, A. Fantini, M. Houssa, et al., 90 nm WAl 2 O 3 TiWCu 1T1R CBRAM cell showing low-power, fast and disturb-free operation, in *2013 5th IEEE International Memory Workshop* (2013), pp. 26–29.
70. A. Belmonte, W. Kim, B.T. Chan, N. Heylen, A. Fantini, M. Houssa, et al., A thermally stable and high-performance 90-nm-based 1T1R CBRAM cell. IEEE Trans. Electron Devices **60**, 3690–3695 (2013)
71. L. Goux, K. Opsomer, R. Degraeve, R. Müller, C. Detavernier, D. Wouters, et al., Influence of the Cu-Te composition and microstructure on the resistive switching of Cu-Te/Al2O3/Si cells. Appl. Phys. Lett. **99**, 053502 (2011)
72. J. Guy, G. Molas, E. Vianello, F. Longnos, S. Blanc, C. Carabasse, et al., Investigation of the physical mechanisms governing data-retention in down to 10 nm nano-trench Al 2 O 3/CuTeGe conductive bridge RAM (CBRAM), in *2013 I.E. International Electron Devices Meeting* (2013), pp. 30.2. 1–30.2. 4
73. K.-H. Kim, S. Gaba, D. Wheeler, J.M. Cruz-Albrecht, T. Hussain, N. Srinivasa, et al., A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications. Nano Lett. **12**, 389–395 (2011)
74. H.P. Wong, S. Raoux, S. Kim, J. Liang, J.P. Reifenberg, B. Rajendran, et al., Phase change memory. Proc. IEEE **98**, 2201–2227 (2010)
75. K. Aratani, K. Ohba, T. Mizuguchi, S. Yasuda, T. Shiimoto, T. Tsushima, et al., A novel resistance memory with high scalability and nanosecond switching, in *2007 I.E. International Electron Devices Meeting* (2007), pp. 783–786.
76. K. Abe, M. P. Tendulkar, J. R. Jameson, P. B. Griffin, K. Nomura, S. Fujita, et al., Ultra-high bandwidth memory with 3D–stacked emerging memory cells, in *2008 I.E. International Conference on Integrated Circuit Design and Technology and Tutorial* (2008), pp. 203–206.
77. S. Rahaman, S. Maikap, Improved resistive switching memory characteristics using novel bi-layered Ge 0.2 Se 0.8/Ta 2 O 5 solid-electrolytes, in *2010 I.E. International Memory Workshop* (2010), pp. 1–4.
78. J. Yi, S.-W. Kim, Y. Nishi, Y.-T. Hwang, S.-W. Chung, S.-J. Hong, et al., Research on switching property of an oxide/copper sulfide hybrid memory, in *Non-Volatile Memory Technology Symposium, 2008. NVMTS 2008. 9th Annual* (2008), pp. 1–4.
79. R. Soni, M. Meier, A. Rüdiger, B. Holländer, C. Kügeler, R. Waser, Integration of “GexSe 1− x” in crossbar arrays for non-volatile memory applications. Microelectron. Eng. **86**, 1054–1056 (2009)
80. M.N. Kozicki, H.J. Barnaby, Conductive bridging random access memory—materials, devices and applications. Semicond. Sci. Technol. **31**, 113001 (2016)
81. U. Celano, L. Goux, A. Belmonte, K. Opsomer, A. Franquet, A. Schulze, et al., Three-dimensional observation of the conductive filament in nanoscaled resistive memory devices. Nano Lett. **14**, 2401–2406 (2014)
82. Y. Yang, P. Gao, S. Gaba, T. Chang, X. Pan, W. Lu, Observation of conducting filament growth in nanoscale resistive memories. Nat. Commun. **3**, 732 (2012)
83. Q. Liu, J. Sun, H. Lv, S. Long, K. Yin, N. Wan, et al., Real-time observation on dynamic growth/dissolution of conductive filaments in oxide-electrolyte-based ReRAM. Adv. Mater. **24**, 1844–1849 (2012)
84. M. Kudo, M. Arita, Y. Ohno, Y. Takahashi, Filament formation and erasure in molybdenum oxide during resistive switching cycles. Appl. Phys. Lett. **105**, 173504 (2014)

85. W.A. Hubbard, A. Kerelsky, G. Jasmin, E. White, J. Lodico, M. Mecklenburg, et al., Nanofilament formation and regeneration during Cu/Al2O3 resistive memory switching. Nano Lett. **15**, 3983–3987 (2015)
86. S. Tappertzhofen, I. Valov, T. Tsuruoka, T. Hasegawa, R. Waser, M. Aono, Generic relevance of counter charges for cation-based nanoscale resistive switching memories. ACS Nano **7**, 6396–6402 (2013)
87. W. Chen, H. J. Barnaby, M. N. Kozicki, A. Edwards, Y. Gonzalez-Velo, R. Fang, et al., A study of gamma-ray exposure of Cu–SiO programmable metallization cells (2015)
88. J. van den Hurk, A.-C. Dippel, D.-Y. Cho, J. Straquadine, U. Breuer, P. Walter, et al., Physical origins and suppression of Ag dissolution in GeS x-based ECM cells. Phys. Chem. Chem. Phys. **16**, 18217–18225 (2014)
89. C. Schindler, I. Valov, R. Waser, Faradaic currents during electroforming of resistively switching Ag–Ge–Se type electrochemical metallization memory cells. Phys. Chem. Chem. Phys. **11**, 5974–5979 (2009)
90. J.D. McBrayer, R. Swanson, T. Sigmon, Diffusion of metals in silicon dioxide. J. Electrochem. Soc. **133**, 1242–1246 (1986)
91. D.B. Strukov, R.S. Williams, Exponential ionic drift: fast switching and low volatility ofáthin-film memristors. Appl. Phys. A **94**, 515–519 (2009)
92. S. Menzel, U. Böttger, M. Wimmer, M. Salinga, Physics of the switching kinetics in resistive memories. Adv. Funct. Mater. **25**, 6306–6325 (2015)
93. C. Schindler, M. Weides, M. Kozicki, R. Waser, Low current resistive switching in Cu-SiO 2 cells. Appl. Phys. Lett. **92** (2008).
94. A. J. Bard, R. Parsons, J. Jordan, *Standard potentials in aqueous solution* vol. 6: CRC press, 1985.
95. D.-Y. Cho, S. Tappertzhofen, R. Waser, I. Valov, Bond nature of active metal ions in SiO 2-based electrochemical metallization memory cells. Nanoscale **5**, 1781–1784 (2013)
96. A. J. Bard, L. R. Faulkner, J. Leddy, C. G. Zoski, *Electrochemical methods: fundamentals and applications* vol. 2: Wiley New York (1980)
97. S. Tappertzhofen, R. Waser, I. Valov, New insights into redox based resistive switches, in *Non-Volatile Memory Technology Symposium (NVMTS), 2013 13th*, 2013, pp. 1–5
98. T. Tsuruoka, I. Valov, S. Tappertzhofen, J. Van Den Hurk, T. Hasegawa, R. Waser, et al., Redox reactions at Cu, Ag/Ta2O5 interfaces and the effects of Ta2O5 film density on the forming process in atomic switch structures. Adv. Funct. Mater. **25**, 6374–6381 (2015)
99. C. Schindler, G. Staikov, R. Waser, Electrode kinetics of Cu-SiO2-based resistive switching cells: overcoming the voltage-time dilemma of electrochemical metallization memories. Appl. Phys. Lett. **94**, 2109 (2009)
100. T. Tsuruoka, K. Terabe, T. Hasegawa, I. Valov, R. Waser, M. Aono, Effects of moisture on the switching characteristics of oxide-based, gapless-type atomic switches. Adv. Funct. Mater. **22**, 70–77 (2012)
101. N. Knorr, R. Wirtz, S. Rosselli, G. Nelles, Field-absorbed water induced electrochemical processes in organic thin film junctions. J. Phys. Chem. C **114**, 15791–15796 (2010)
102. S. Tappertzhofen, M. Hempel, I. Valov, R. Waser, Proton mobility in SiO 2 thin films and impact of hydrogen and humidity on the resistive switching effect, in *MRS Proceedings* (2011), pp. mrss11-1330-j01-02-k03-02.
103. T. Tsuruoka, I. Valov, C. Mannequin, T. Hasegawa, R. Waser, M. Aono, Humidity effects on the redox reactions and ionic transport in a Cu/Ta2O5/Pt atomic switch structure. Jpn. J. Appl. Phys. **55**, 06GJ09 (2016)
104. S. Tappertzhofen, R. Waser, I. Valov, Impact of the counter-electrode material on redox processes in resistive switching memories. ChemElectroChem **1**, 1287–1292 (2014)
105. I. Valov, E. Linn, S. Tappertzhofen, S. Schmelzer, J. Van den Hurk, F. Lentz, et al., Nanobatteries in redox-based resistive switches require extension of memristor theory. Nat. Commun. **4**, 1771 (2013)
106. X. Guo, C. Schindler, S. Menzel, R. Waser, Understanding the switching-off mechanism in Ag + migration based resistively switching model systems. Appl. Phys. Lett. **91**, 133513 (2007)
107. H. Sun, Q. Liu, C. Li, S. Long, H. Lv, C. Bi, et al., Direct observation of conversion between threshold switching and memory switching induced by conductive filament morphology. Adv. Funct. Mater. **24**, 5679–5686 (2014)
108. W. Yu, Fractal properties and applications of dendritic filaments in programmable metallization cells, Arizona State University (2015)
109. Z. Xu, Y. Bando, W. Wang, X. Bai, D. Golberg, Real-time in situ HRTEM-resolved resistance switching of Ag2S nanoscale ionic conductor. ACS Nano **4**, 2515–2522 (2010)
110. Y. Yang, P. Gao, L. Li, X. Pan, S. Tappertzhofen, S. Choi, et al., Electrochemical dynamics of nanoscale metallic inclusions in dielectrics, Nat. Commun., **5** (2014)
111. J. Mayer, L.A. Giannuzzi, T. Kamino, J. Michael, TEM sample preparation and FIB-induced damage. MRS Bull. **32**, 400–407 (2007)
112. C.-S. Yang, D.-S. Shang, Y.-S. Chai, L.-Q. Yan, B.-G. Shen, Y. Sun, Moisture effects on the electrochemical reaction and resistance switching at Ag/molybdenum oxide interfaces. Phys. Chem. Chem. Phys. **18**, 12466–12475 (2016)
113. F. Messerschmitt, M. Kubicek, J.L. Rupp, How does moisture affect the physical property of Memristance for anionic–electronic resistive switching memories? Adv. Funct. Mater. **25**, 5117–5125 (2015)
114. G. Di Martino, S. Tappertzhofen, S. Hofmann, J. Baumberg, Nanoscale Plasmon-enhanced spectroscopy in memristive switches, *Small,* (2016)
115. J.R. Macdonald, E. Barsoukov, Impedance spectroscopy: theory, experiment, and applications. Second Edition, 1–26 (2005)
116. J. R. Macdonald, W. B. Johnson, Fundamentals of impedance spectroscopy, *Impedance Spectroscopy: Theory, Experiment, and Applications, Second Edition,* pp. 1–26, (2005)
117. Y. Liu, P. Gao, X. Jiang, K. Bi, H. Xu, W. Peng, Percolation network in resistive switching devices with the structure of silver/amorphous silicon/p-type silicon. Appl. Phys. Lett. **104**, 043502 (2014)
118. D. Mahalanabis, Y. Gonzalez-Velo, H.J. Barnaby, M.N. Kozicki, P. Dandamudi, S. Vrudhula, Impedance measurement and characterization of Ag-Ge 30 Se 70-based programmable metallization cells. Electron Devices, IEEE Transactions on **61**, 3723–3730 (2014)
119. D.S. Jeong, H. Schroeder, R. Waser, Impedance spectroscopy of TiO2 thin films showing resistive switching. Appl. Phys. Lett. **89**, 82909–83100 (2006)
120. W.M. Merrill, R.E. Diaz, M.M. LoRe, M.C. Squires, N.G. Alexopoulos, Effective medium theories for artificial materials composed of multiple sizes of spherical inclusions in a host continuum. IEEE Trans. Antennas Propag. **47**, 142–148 (1999)
121. A. Chung, J. Deen, J.-S. Lee, M. Meyyappan, Nanoscale memory devices. Nanotechnology **21**, 412001 (2010)
122. D.J. Wouters, R. Waser, M. Wuttig, Phase-change and redox-based resistive switching memories. Proc. IEEE **103**, 1274 (2015)
123. E. Linn, R. Rosezin, C. Kügeler, R. Waser, Complementary resistive switches for passive nanocrossbar memories. Nat. Mater. **9**, 403–406 (2010)

124. S. Menzel, S. Tappertzhofen, R. Waser, I. Valov, Switching kinetics of electrochemical metallization memory cells. Phys. Chem. Chem. Phys. **15**, 6945–6952 (2013)
125. M.D. Pickett, R.S. Williams, Sub-100 f. and sub-nanosecond thermally driven threshold switching in niobium oxide crosspoint nanodevices. Nanotechnology **23**, 215202 (2012)
126. R. Bez, E. Camerlenghi, A. Modelli, A. Visconti, Introduction to flash memory. Proc. IEEE **91**, 489–502 (2003)
127. Y. Fujisaki, Current status of nonvolatile semiconductor memory technology. Jpn. J. Appl. Phys. **49**, 100001 (2010)
128. E. Linn, R. Rosezin, S. Tappertzhofen, R. Waser, Beyond von Neumann? Logic operations in passive crossbar arrays alongside memory operations. Nanotechnology **23**, 305205 (2012)
129. S. Menzel, U. Böttger, R. Waser, Simulation of multilevel switching in electrochemical metallization memory cells. J. Appl. Phys. **111**, 014501 (2012)
130. S. Tappertzhofen, E. Linn, S. Menzel, A.J. Kenyon, R. Waser, I. Valov, Modeling of quantized conductance effects in electrochemical metallization cells. IEEE Trans. Nanotechnol. **14**, 505–512 (2015)
131. D.E. Nikonov, I.A. Young, Overview of beyond-CMOS devices and a uniform methodology for their benchmarking. Proc. IEEE **101**, 2498–2533 (2013)
132. J. Åkerman, Toward a universal memory. Science **308**, 508–510 (2005)
133. T. Vogelsang, Understanding the energy consumption of dynamic random access memories, in *Proceedings of the 2010 43rd Annual IEEE/ACM International Symposium on Microarchitecture* (2010), pp. 363–374
134. *ITRS. Edition 2013,* (2013)
135. K. Wang, J. Alzate, P.K. Amiri, Low-power non-volatile spintronic memory: STT-RAM and beyond. J. Phys. D. Appl. Phys. **46**, 074003 (2013)
136. B. Rooseleer and W. Dehaene, A 40 nm, 454 MHz 114 fJ/bit area-efficient SRAM memory with integrated charge pump, in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, 2013, pp. 201–204
137. D. Ielmini, Filamentary-switching model in RRAM for time, energy and scaling projections, in *Electron Devices Meeting (IEDM), 2011 I.E. International* (2011), pp. 17.2. 1–17.2. 4
138. A. Belmonte, U. Celano, R. Degraeve, A. Fantini, A. Redolfi, W. Vandervorst, et al., Operating-current dependence of the Cu-mobility requirements in oxide-based conductive-bridge RAM. IEEE Electron Device Lett. **36**, 775–777 (2015)
139. I. Valov, G. Staikov, Nucleation and growth phenomena in nanosized electrochemical systems for resistive switching memories. J. Solid State Electrochem. **17**, 365–371 (2013)
140. M. Morales-Masis, S. Van Der Molen, T. Hasegawa, J. Van Ruitenbeek, Bulk and surface nucleation processes in Ag 2 S conductance switches. Phys. Rev. B **84**, 115310 (2011)
141. Y. Bernard, P. Gonon, V. Jousseaume, Resistance switching of Cu/SiO2 memory cells studied under voltage and current-driven modes. Appl. Phys. Lett. **96**, 3502 (2010)
142. U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, M.N. Kozicki, Study of multilevel programming in programmable metallization cell (PMC) memory. Electron Devices, IEEE Trans. **56**, 1040–1047 (2009)
143. A. Nayak, T. Tsuruoka, K. Terabe, T. Hasegawa, M. Aono, Switching kinetics of a Cu2S-based gap-type atomic switch. Nanotechnology **22**, 235201 (2011)
144. A. Nayak, T. Tamura, T. Tsuruoka, K. Terabe, S. Hosaka, T. Hasegawa, et al., Rate-limiting processes determining the switching time in a Ag2S atomic switch. J. Phys. Chem. Lett. **1**, 604–608 (2010)
145. I. Valov, I. Sapezanskaia, A. Nayak, T. Tsuruoka, T. Bredow, T. Hasegawa, et al., Atomically controlled electrochemical nucleation at superionic solid electrolyte surfaces. Nat. Mater. **11**, 530–535 (2012)
146. S. Tappertzhofen, I. Valov, R. Waser, Quantum conductance and switching kinetics of AgI-based microcrossbar cells. Nanotechnology **23**, 145703 (2012)
147. J. van den Hurk, V. Havel, E. Linn, R. Waser, I. Valov, Ag/GeSx/Pt-based complementary resistive switches for hybrid CMOS/Nanoelectronic logic and memory architectures. Sci. Rep. **3** (2013).
148. T. Tsuruoka, T. Hasegawa, I. Valov, R. Waser, M. Aono, Rate-limiting processes in the fast SET operation of a gapless-type Cu-Ta2O5 atomic switch. AIP Adv. **3**, 032114 (2013)
149. M. Meier, C. Schindler, S. Gilles, R. Rosezin, A. Rudiger, C. Kugeler, et al., A nonvolatile memory with resistively switching methyl-silsesquioxane. IEEE Electron Device Lett. **30**, 8–10 (2009)
150. S. Nandakumar, M. Minvielle, S. Nagar, C. Dubourdieu, B. Rajendran, A 250 mV Cu/SiO2/W memristor with half-integer quantum conductance states. Nano Lett. **16**, 1602–1608 (2016)
151. A. Calderoni, S. Sills, C. Cardon, E. Faraoni, N. Ramaswamy, Engineering ReRAM for high-density applications. Microelectron. Eng. **147**, 145–150 (2015)
152. J. Krans, C. Muller, I. Yanson, T.C. Govaert, R. Hesper, J. Van Ruitenbeek, One-atom point contacts. Phys. Rev. B **48**, 14721 (1993)
153. S.J. Choi, G.S. Park, K.H. Kim, S. Cho, W.Y. Yang, X.S. Li, et al., In situ observation of voltage-induced multilevel resistive switching in solid electrolyte memory. Adv. Mater. **23**, 3272–3277 (2011)
154. A. Belmonte, U. Celano, A. Redolfi, A. Fantini, R. Muller, W. Vandervorst, et al., Analysis of the excellent memory disturb characteristics of a hourglass-shaped filament in Al 2 O 3/Cu-based CBRAM devices. IEEE Trans. Electron Devices **62**, 2007–2013 (2015)
155. S. Gao, C. Chen, Z. Zhai, H. Liu, Y. Lin, S. Li, et al., Resistive switching and conductance quantization in Ag/SiO2/indium tin oxide resistive memories. Appl. Phys. Lett. **105**, 063504 (2014)
156. P. Cappelletti, A. Modelli, Flash memory reliability, in *Flash Memories*, ed: Springer (1999), pp. 399–441.
157. J. Woo, A. Belmonte, A. Redolfi, H. Hwang, M. Jurczak, L. Goux, Role of local chemical potential of Cu on data retention properties of Cu-based conductive-bridge RAM. IEEE Electron Device Lett. **37**, 173–175 (2016)
158. K. Sankaran, L. Goux, S. Clima, M. Mees, J.A. Kittl, M. Jurczak, et al., Modeling of copper diffusion in amorphous aluminum oxide in CBRAM memory stack. ECS Trans. **45**, 317–330 (2012)
159. S. Tappertzhofen, E. Linn, U. Böttger, R. Waser, I. Valov, Nanobattery effect in RRAMs—implications on device stability and endurance. IEEE Electron Device Lett. **35**, 208–210 (2014)
160. G. Molas, E. Vianello, F. Dahmani, M. Barci, P. Blaise, J. Guy, et al., Controlling oxygen vacancies in doped oxide based CBRAM for improved memory performances, in *2014 I.E. International Electron Devices Meeting* (2014), pp. 6.1. 1–6.1. 4
161. M. Barci, J. Guy, G. Molas, E. Vianello, A. Toffoli, J. Cluzel, et al., Impact of SET and RESET conditions on CBRAM high temperature data retention, in *2014 I.E. International Reliability Physics Symposium* (2014), pp. 5E. 3.1-5E. 3.4
162. J. Jameson, P. Blanchard, C. Cheng, J. Dinh, A. Gallo, V. Gopalakrishnan, et al., Conductive-bridge memory (CBRAM) with excellent high-temperature retention, in *2013 I.E. International Electron Devices Meeting* (2013)
163. S. Sills, S. Yasuda, J. Strand, A. Calderoni, K. Aratani, A. Johnson, et al., A copper ReRAM cell for storage class memory applications, in *VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on* (2014), pp. 1–2
164. Y. Li, P. Yuan, L. Fu, R. Li, X. Gao, C. Tao, Coexistence of diode-like volatile and multilevel nonvolatile resistive switching in a ZrO2/TiO2 stack structure. Nanotechnology **26**, 391001 (2015)

165. T. Hino, T. Hasegawa, H. Tanaka, T. Tsuruoka, K. Terabe, T. Ogawa, et al., Volatile and nonvolatile selective switching of a photo-assisted initialized atomic switch. Nanotechnology **24**, 384006 (2013)
166. T. Liu, M. Verma, Y. Kang, M. Orlowski, Volatile resistive switching in Cu/TaOx/δ-Cu/Pt devices. Appl. Phys. Lett. **101**, 073510 (2012)
167. J. Song, J. Woo, A. Prakash, D. Lee, H. Hwang, Threshold selector with high selectivity and steep slope for cross-point memory array (2016)
168. J. Van den Hurk, E. Linn, H. Zhang, R. Waser, I. Valov, Volatile resistance states in electrochemical metallization cells enabling non-destructive readout of complementary resistive switches. Nanotechnology **25**, 425202 (2014)
169. R. Yang, K. Terabe, Y. Yao, T. Tsuruoka, T. Hasegawa, J.K. Gimzewski, et al., Synaptic plasticity and memory functions achieved in a WO3− x-based nanoionics device by using the principle of atomic switch operation. Nanotechnology **24**, 384003 (2013)
170. Z. Wang, S. Joshi, S.E. Savel'ev, H. Jiang, R. Midya, P. Lin, et al., Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. Nat. Mater. **16**, 101–108 (2017)
171. W. Chen, H. Barnaby, M. Kozicki, Volatile and non-volatile switching in Cu-SiO 2 programmable metallization cells. IEEE Electron Device Lett. **37**, 580–583 (2016)
172. Y.M. Lu, M. Noman, W. Chen, P.A. Salvador, J.A. Bain, M. Skowronski, Elimination of high transient currents and electrode damage during electroformation of TiO2-based resistive switching devices. J. Phys. D. Appl. Phys. **45**, 395101 (2012)
173. D. Gilmer, G. Bersuker, H.-Y. Park, C. Park, B. Butcher, W. Wang, et al., Effects of RRAM stack configuration on forming voltage and current overshoot, in *2011 3rd IEEE International Memory Workshop (IMW)* (2011), pp. 1–4
174. H. Wan, P. Zhou, L. Ye, Y. Lin, T. Tang, H. Wu, et al., In situ observation of compliance-current overshoot and its effect on resistive switching. IEEE Electron Device Lett. **31**, 246–248 (2010)
175. K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, et al., Reduction in the reset current in a resistive random access memory consisting of NiOx brought about by reducing a parasitic capacitance. Appl. Phys. Lett. **93**, 3506 (2008)
176. Y. Sato, K. Tsunoda, K. Kinoshita, H. Noshiro, M. Aoki, Y. Sugiyama, Sub-reset current of nickel oxide resistive memory through control of filamentary conductance by current limit of MOSFET. IEEE Trans. Electron Devices **55**, 1185–1191 (2008)
177. D. Kamalanathan, A. Akhavan, M. Kozicki, Low voltage cycling of programmable metallization cell memory devices. Nanotechnology **22**, 254017 (2011)
178. S. Dietrich, M. Angerbauer, M. Ivanov, D. GOG, H. Hoenigschmid, M. Kund, et al., A nonvolatile 2-Mbit CBRAM memory core featuring advanced read and program control. IEEE J. Solid State Circuits **42**, 839–845 (2007)
179. S. Kaeriyama, T. Sakamoto, H. Sunamura, M. Mizuno, H. Kawaura, T. Hasegawa, et al., A nonvolatile programmable solid-electrolyte nanometer switch. IEEE J. Solid State Circuits **40**, 168–176 (2005)
180. L. Goux, K. Opsomer, A. Franquet, G. Kar, N. Jossart, O. Richard, et al., Thermal-stability optimization of Al 2 O 3/Cu–Te based conductive-bridging random access memory systems. Thin Solid Films **533**, 29–33 (2013)
181. P. Schrögmeier, M. Angerbauer, S. Dietrich, M. Ivanov, H. Honigschmid, C.-M. Liaw, et al., Time discrete voltage sensing and iterative programming control for a 4F 2 multilevel CBRAM, in *VLSI Circuits, 2007 I.E. Symposium on* (2007), pp. 186–187
182. R. Symanczyk, R. Dittrich, J. Keller, M. Kund, G. Müller, B. Ruf, et al., Conductive bridging memory development from single cells to 2Mbit memory arrays, in *Non-Volatile Memory Technology Symposium, 2007. NVMTS'07* (2007), pp. 71–75
183. N. Gilbert, Y. Zhang, J. Dinh, B. Calhoun, S. Hollmer, A 0.6 V 8 pJ/write non-volatile CBRAM macro embedded in a body sensor node for ultra low energy applications, in *VLSI Circuits (VLSIC),* 2013 Symposium on. IEEE (2013)
184. R. Fackenthal, M. Kitagawa, W. Otsuka, K. Prall, D. Mills, K. Tsutsui, et al., 19.7 A 16Gb ReRAM with 200 MB/s write and 1GB/s read in 27 nm technology, in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 I.E. International* (2014), pp. 338–339
185. M.-J. Lee, D. Lee, H. Kim, H.-S. Choi, J.-B. Park, H. G. Kim, et al., Highly-scalable threshold switching select device based on chaclogenide glasses for 3D nanoscaled memory arrays, in *Electron Devices Meeting (IEDM), 2012 I.E. International* (2012), pp. 2.6. 1–2.6. 3
186. M. Son, J. Lee, J. Park, J. Shin, G. Choi, S. Jung, et al., Excellent selector characteristics of nanoscale for high-density bipolar ReRAM applications. Electron Device Lett., IEEE **32**, 1579–1581 (2011)
187. S. Kim, X. Liu, J. Park, S. Jung, W. Lee, J. Woo, et al., Ultrathin (< 10 nm) Nb 2 O 5/NbO 2 hybrid memory with both memory and selector characteristics for high density 3D vertically stackable RRAM applications, in *VLSI Technology (VLSIT), 2012 Symposium on* (2012), pp. 155–156
188. K. Gopalakrishnan, R. Shenoy, C. Rettner, K. Virwani, D. Bethune, R. Shelby, et al., Highly-scalable novel access device based on mixed ionic electronic conduction (MIEC) materials for high density phase change memory (PCM) arrays, in *2010 Symposium on VLSI Technology* (2010), pp. 205–206
189. A. Padilla, G. Burr, R. Shenoy, K. Raman, D. Bethune, R. Shelby, et al., The origin of massive nonlinearity in Mixed-Ionic-Electronic-Conduction (MIEC)-based Access Devices, as revealed by numerical device simulation, in *72nd Device Research Conference* (2014), pp. 163–164
190. S.C. Puthentheradam, D.K. Schroder, M.N. Kozicki, Inherent diode isolation in programmable metallization cell resistive memory elements. Appl. Phys. A **102**, 817–826 (2011)
191. D.A. Drachman, Do we have brain to spare? Neurology **64**, 2004–2005 (2005)
192. D. Johnston, S.M.-S. Wu, R. Gray, *Foundations of cellular neurophysiology* (MIT press, Cambridge, 1995)
193. G. Indiveri, E. Chicca, R. Douglas, A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity. IEEE Trans. Neural Netw. **17**, 211–221 (2006)
194. S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, H.-S.P. Wong, An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation. IEEE Trans. Electron Devices **58**, 2729–2737 (2011)
195. M. Prezioso, F. Merrikh-Bayat, B. Hoskins, G. Adam, K.K. Likharev, D.B. Strukov, Training and operation of an integrated neuromorphic network based on metal-oxide memristors. Nature **521**, 61–64 (2015)
196. Y. Li, Y. Zhong, L. Xu, J. Zhang, X. Xu, H. Sun, et al., Ultrafast synaptic events in a chalcogenide memristor, Sci. Rep., **3** (2013)
197. J.R. Schwank, *Basic mechanisms of radiation effects in the natural space radiation environment* (Sandia National Labs, Albuquerque, NM (United States), 1994)
198. D. Nguyen, S. Guertin, G. Swift, A. Johnston, Radiation effects on advanced flash memories. Nucl. Sci., IEEE Trans. **46**, 1744–1750 (1999)
199. Y. Gonzalez-Velo, H. Barnaby, M. Kozicki, P. Dandamudi, A. Chandran, K. Holbert, et al., Total-ionizing-dose effects on the resistance switching characteristics of chalcogenide programmable metallization cells. Nucl. Sci., IEEE Trans. **60**, 4563–4569 (2013)

200. J. Taggart, Y. Gonzalez-Velo, D. Mahalanabis, A. Mahmud, H.J. Barnaby, M.N. Kozicki, et al., Ionizing radiation effects on non-volatile memory properties of programmable metallization cells. Nucl. Sci., IEEE Trans. **61**, 2985–2990 (2014)
201. Y. Gonzalez-Velo, A. Mahmud, W. Chen, J. Taggart, H. Barnaby, M. Kozicki, et al., TID impact on process modified CBRAM cells, in *Radiation and Its Effects on Components and Systems (RADECS), 2015 15th European Conference on* (2015), pp. 1–4
202. P. Dandamudi, M.N. Kozicki, H.J. Barnaby, Y. Gonzalez-Velo, K.E. Holbert, Total ionizing dose tolerance of based programmable metallization cells. Nucl. Sci., IEEE Trans. **61**, 1726–1731 (2014)
203. R. Fang, Y.G. Velo, W. Chen, K.E. Holbert, M.N. Kozicki, H. Barnaby, et al., Total ionizing dose effect of γ-ray radiation on the switching characteristics and filament stability of HfOx resistive random access memory. Appl. Phys. Lett. **104**, 183507 (2014)
204. M.J. Marinella, S.M. Dalton, P.R. Mickel, P.E.D. Dodd, M.R. Shaneyfelt, E. Bielejec, et al., Initial assessment of the effects of radiation on the electrical characteristics of memristive memories. IEEE Trans. Nucl. Sci. **59**, 2987–2994 (2012)
205. Y. Wang, H. Lv, W. Wang, Q. Liu, S. Long, Q. Wang, et al., Highly stable radiation-hardened resistive-switching memory. IEEE Electron Device Lett. **31**, 1470–1472 (2010)
206. L. Zhang, R. Huang, D. Gao, P. Yue, P. Tang, F. Tan, et al., Total ionizing dose (TID) effects on-based resistance change memory. IEEE Trans. Electron Devices **58**, 2800–2804 (2011)
207. A. H. Edwards, K. A. Campbell, Density functional study of Ag in Ge 2 Se 3, in *Non-Volatile Memory Technology Symposium (NVMTS), 2009 10th Annual* (2009), pp. 1–7
208. S. Ferch, E. Linn, R. Waser, S. Menzel, Simulation and comparison of two sequential logic-in-memory approaches using a dynamic electrochemical metallization cell model. Microelectron. J. **45**, 1416–1428 (2014)
209. A. Siemon, S. Menzel, R. Waser, E. Linn, A complementary resistive switch-based crossbar array adder. IEEE J. Emerging Sel. Top Circuits Syst. **5**, 64–74 (2015)