Journal of Computational Electronics (2024) 23:899–909
https://doi.org/10.1007/s10825-024-02176-3

Floating/grounded charged controlled memristor emulator using DVCCTA

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Received: 17 May 2023 / Accepted: 24 April 2024 / Published online: 16 May 2024

Abstract
In this work, a charge-based memristor emulator is designed using a single active current mode component Differential Voltage Current Conveyor Transconductance Amplifier with one capacitor and two resistors as passive components. Importantly, the proposed circuit topology can be changed to either grounded or floating configuration using a single switch. Moreover, the proposed memristor design can be operated either in incremental or decremental configuration by using another switch. Therefore, using only two switches, the same circuitry can be utilized to design the floating/grounded incremental/decremental memristor. The pinched hysteresis loop area can be controlled by applying different biasing voltages. Further, the mathematical analysis is performed to drive the theoretical TiO_2 based results for the proposed memristor emulator. In addition, simulations confirming the theoretical analysis are conducted in PSPICE using the 180 nm TSMC technology with a supply voltage of ± 0.9 V by varying frequencies and capacitances to obtain a pinched hysteresis loop. The presented circuit performs effectively for frequencies upto 500 MHz while operating with grounded type memristor and 300 MHz with floating type design. To check the ability to remember the history of the proposed memristor, the non-volatility test is performed for both the incremental and decremental configurations. Moreover, the suggested memristor design is applied in an adaptive learning circuit to prove its feasibility in neuromorphic applications.

Keywords Current mode · Decremental configuration · Floating · Grounded · Incremental configuration · Memristor emulator · Pinched hysteresis loop

1 Introduction

Until 1971, only three fundamental components were known i.e., resistor (defining relation between voltage and current), inductor (current and magnetic flux), and capacitor (charge and voltage). In [1], the author proposed a fourth fundamental nonlinear element by forming a missing relationship between charge and flux, which is known as a memristor. The memristor exhibits a hysteresis curve pinched at the origin within the voltage and current plane that changes with the operating frequency [2]. The pinched hysteresis curve represents the memory in the memristor, hence it is observed as an inherent non-volatile characteristic. Apart from the non-volatility property of the memristor, other features like lower energy consumption [3, 4], higher operating speed [5], better scaling for high integration density [6] etc. have created widespread interest among researchers. Importantly, the memristor can be most beneficial to overcome the major limitation of Von Neumann's architecture which is a separate memory requirement from the logic design. Note that a non-volatile memristor not only provides storage capability but also it can implement various analog and digital logic when connected using specific architecture [7]. Hence, this important characteristic of the memristor has led to the development of hybrid architecture comprising memory and logic functionalities to enhance memory storage capabilities [8], enabling more efficient memory computation. Remarkably, the first prototype of a solid state memristor was developed by a team of researchers at HP Laboratories in the year 2008 [9]. Here, a thin film of titanium dioxide is situated between

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two platinum contacts to produce the memristor. Additionally, various other materials such as (metal insulator metal) MIM structure [10], oxides such as WO_x, FeO_x, SiO_x etc. [11–13], chalcogenides [14] and ferroelectric materials [15] are also used to construct memristor. However, commercialization of memristor is still not popular due to the limitations in performance of the device, difficulty in nanoscale fabrication, and most importantly, its high manufacturing cost.

Therefore, to overcome this limitation, the behavior of the memristors can be studied by designing a memristor emulator circuit with readily available components. Importantly, this memristor emulator has ability to mimic the required characteristics such as non-volatility and current-voltage relationship as shown in TiO_2 model proposed by HP labs [3]. Specifically, various designs of memrisor emulators based on HP's TiO_2 linear ion model are discussed in the literature using various analog components. Particularly, design of the emulator is demonstrated using Operational Amplifier (OPAMP) [16, 17] and current mode building blocks such as Operational Transconductance Amplifier (OTA) [18, 19], Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) [20], Current Conveyor Transconductance Amplifier (CCTA) [21], Current Backward Transconductance Amplifier (CBTA) [22], and Voltage Difference Transconductance Amplifier (VDTA) [23, 24]. Further, these memristor emulator will assist the research community to explore the potential use of memristors in various applications e.g., as synapse in artificial neural networks (ANN) [25], logical operations [26, 27], resistive RAM [28], memristor based SRAM [29], chaotic oscillator [30, 31], chaotic neural networks (CNN) [32], image compression [33].

Apart from this, a memristor operation can be divided based on either flux controlled (Memductance) and charge controlled (Memristance) [1]. Additionally, the emulator circuits can be categorized into grounded configuration and floating configuration based on the application. In the literature, the charge based grounded configuration is discussed in [20, 22, 34–36], and [37] is a flux controlled memristor emulator. Also, flux based floating configuration is discussed in the papers [19, 26, 33, 38] and charge based floating configuration memristor is discussed in [39]. However. there is still need for a generic emulator capable of functioning in both floating and grounded configuration. This limitation can be overcome in [21, 32, 40–42] where authors discussed both floating/grounded configuration. However, the implemented circuits in [18, 40, 42] require separate circuitry for grounded/floating configuration. Therefore, design of a versatlie memristor emulator circuit is required capable of working on both grounded and floating configuration using unified circuit approach. This will increase the memristor application for future technolology. Moreover it is desirable for the memristor emulator to achieve the highest values possible of speed or frequency of operation. However, circuits proposed in [17, 22] encounter limitation in operating frequency. For [19] operating speed is limited to 1 MHz. Here, based on our current knowledge, the highest operating speed achieved by any memristor emulator is discussed by Vista et. al. in [41] is 50 MHz. However, feasibility of the circuit is not tested. In addition, the area of the designed memristor emulator proposed in [17, 35, 36] is quite large for physical implementation. Also, the memristor design discussed in [17, 35, 38] and [41] require high power consumption thereby imposing constraints on overall system capabilities. Therefore, designing the memristor emulator to operate at high frequencies while minimizing power consumption and reducing size is essential.

Therefore, motivated by the above, there is need to design generic menrsitor which can be operated in floating/grounded configuration in single circuitry with higher operating frequency, smaller area and lower power consumption. This paper presents the design of a charge-based memristor emulator utilizing the TiO_2 model [9]. The emulator employs a single active component, the DVCCTA, along with two resistors and one capacitor. Unlike [19], the presented emulator circuit uses a single circuitry for floating and grounded configuration with incremental/decremental cases. It can be adjusted electronically by changing the bias voltage. The rest of the paper is organized as follows: Sect. 2 describes the detailed mathematical description to develop a theoretical model of the memristor emulation circuit under consideration. Moreover, at increased frequencies, parasitic resistances and capacitances becomes crucial. Hence, the effect of nonidealities at the port of DVCCTA, parasitic resistances, and capacitances are also studied in this section. Further, the effect of variation on frequencies, capacitor values, amplitude, and biasing voltages on implemented memristor emulator circuit is studied in Sect. 3. In addition, to confirm the retention property, a non-volatiltiy test for incremental and decremental configuration has been included in the same section. A comparative analysis between the designed circuit and previous literature work is done in Sect. 4. The proposed circuit workability is tested in the adaptive learning circuit in Sect. 5. The Sect. 6 discusses summary and conclusion of the presented circuit.

2 Mathematical description and implementation of proposed emulator model

The emulator circuit presented in this design is composed of a single Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA) as an active component with one capacitor and two resistors as passive components.

2.1 Port relationship of DVCCTA

The port relationship of DVCCTA shown in Fig. 1 is given by $I_{y1}=0$, $I_{y2}=0$, $V_x=V_{y1}-V_{y2}$, $I_z\pm=\pm I_x$, and $I_o\pm=\pm g_m V_{z1}$. The MOSFET based implementation of DVCCTA is illustrated in Fig. 2 is taken from [44]. The value of transconductance gain is shown as

$$g_m = k\left(\frac{V_c - V_{ss}}{2} - V_T\right) \tag{1}$$

where V_c is the externally applied voltage, V_{ss} is the supply voltage, V_T is the threshold voltage and k is given by $\frac{\mu_n C_{ox}}{\sqrt{2}}\sqrt{\left(\frac{W}{L}\right)_{M_{25}}\left(\frac{W}{L}\right)_{M_{28}}}$. μ_n given here is the mobility of electrons, C_{ox} is the oxide capacitance, $\left(\frac{W}{L}\right)_{M_{25}}$ and $\left(\frac{W}{L}\right)_{M_{28}}$ are the aspect ratios of MOSFET. The values of MOSFETs are shown in Table 1.

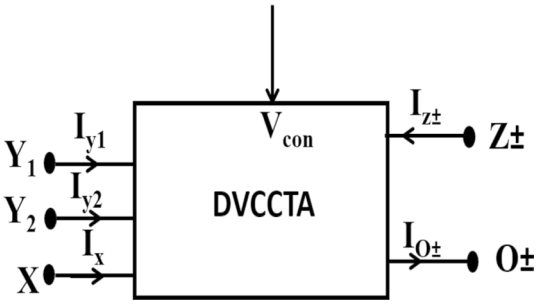

Fig. 1 DVCCTA symbol

Table 1 Aspect ratios for MOSFET

MOSFET	W (μm)	L (μm)
M_1-M_4	8.5	0.36
M_{19}, M_{11}, M_{13}, M_{15}, M_{17}, M_{19}, M_{21}, M_{23}, M_{24}	4.32	0.18
M_6, M_8, M_{10}, M_{12}, M_{14}, M_{16}, M_{18}, M_{20}, M_{22}, M_{25}	21.6	0.18
M_{31}, M_{33}, M_{35}, M_{37}	4.31	0.36
M_{29}, M_{32}, M_{34}, M_{36}	7.2	0.36
M_{28}, M_{30}	21.6	0.36
M_{26}, M_{27}	21.6	0.36

2.2 Theoretical analysis of presnted memristor emulator (MRE)

The proposed memristor emulator design presented in Fig. 3 is built upon linear ion drift model [9]. Here characteristics equation is taken and compared with the results mentioned by the authors in this paper. It can be made to operate in incremental type or decremental type floating/grounded configuration by using two simple switches S_1 and S_2 as shown in Table 2. The W/L ratio is selected through g_m/I_d methodology to ensure that all the transistors work in the saturation region. The generalised equation mentioned in [9] is shown below:-

$$V(\mathrm{t}) = M(q(t))\, i(t) \tag{2}$$

Here

$$M(q(t)) = R_{\mathrm{set}}x(t) + R_{\mathrm{reset}}(1 - x(t)) \tag{3}$$

Here R_{set} is the low resistance value and R_{reset} is the high resistance value. $x(t)$ depends on width $w(t)$ of the

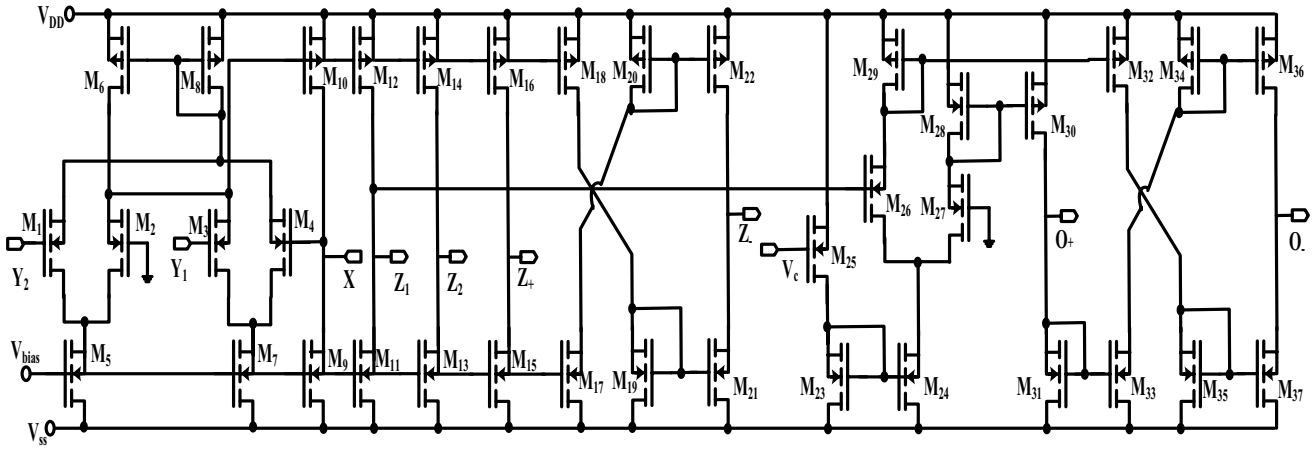

Fig. 2 MOSFET implementation of DVCCTA

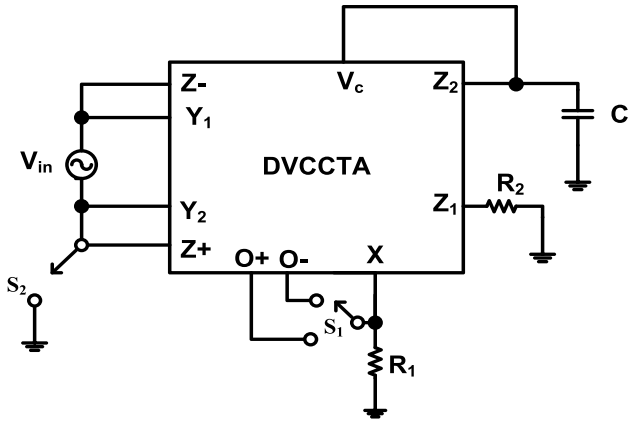

Fig. 3 Proposed floating/grounded memristor emulator circuit

Table 2 S_1 and S_2 linkage for floating (F)/grounded (G) incremental (Inc)/decremental (Dec) configuration

Switch S1	Switch S2	F/G	Inc/Dec	Symbol
$S_1 \rightarrow$ port O-	$S_2 \rightarrow$ open	F	Inc	
$S_1 \rightarrow$ port O+	$S_2 \rightarrow$ open	F	Dec	
$S_2 \rightarrow$ port O-	$S_2 \rightarrow$ closed	G	Inc	
$S_2 \rightarrow$ port O+	$S_2 \rightarrow$ closed	G	Dec	

inner oxide layer which moves w.r.t applied voltage $V(t)$. The $w(t)$ depends on $q(t)$ (charge). Overall memristance equation is given by

$$M(q(t)) = \underbrace{R_{\text{reset}}}_{\text{Constant}} - \underbrace{R_{\text{reset}}\text{kq}(t)}_{\text{Time variant}} \tag{4}$$

where k depends on mobility of charge carriers, thickness of the device and R_{set} values.

Applied voltage in Fig. 3 is represented as

$$V_{y1} - V_{y2} = V_x = V_{\text{in}}(t) \tag{5}$$

Here the differential voltage applied at the Y_1 and Y_2 is utilized to make the emulator circuit work in a floating configuration. For grounded configuration, Y_2 terminal is connected to ground. Input current ($I_{\text{in}}(t)$) flows from Z–terminal (direction of current is reversed) is copied to Z_1 port, X port and Z_2 port.

Voltage at Z_1 port is $I_{\text{in}}(t)R_2$. Therefore, current at O ± terminal is given by

$$I_{o\pm} = \pm g_m I_{\text{in}}(t) R_2 \tag{6}$$

Charge at Z_2 terminal is obtained as,

$$V_c = \int \frac{I_{\text{in}}(t)}{C}\text{dt} = \frac{q(t)}{C} \tag{7}$$

Substituting the value of V_c. The Eq. (6) is modified as:-

$$I_{o\pm} = \pm k\left(\frac{q(t)}{2C} - \frac{V_{\text{ss}}}{2} - V_T\right) I_{\text{in}}(t)R_2 \tag{8}$$

On doing circuit analysis for port X, the equation is represented as:-

$$I_{\text{in}}(t) + \frac{V_{\text{in}}(t)}{R_1} + I_{o\pm} = 0 \tag{9}$$

Generalized Memristance equation for decremental/incremental configuration is obtained by replacing $I_{o\pm}$ by Eq. (3) and rearranging the above equation,

$$\frac{V_{\text{in}}(t)}{I_{\text{in}}(t)} = \underbrace{\frac{\mp \text{kq}(t)}{2C} R_1R_2}_{\text{Constant term}} \underbrace{- R_1 \pm \left(\frac{V_{\text{ss}}}{2} + V_T\right) kR_1R_2}_{\text{Time variant term}} \tag{10}$$

The above mentioned $M(q(t))$ is in the form of linear ion drift Based model mentioned in Eq. (4). Incremental memristance is given by

$$\frac{V_{\text{in}}(t)}{I_{\text{in}}(t)} = \frac{\text{kq}(t)}{2C} R_1R_2 - \left(\left(\frac{V_{\text{ss}}}{2} + V_T\right) kR_1R_2 + R_1\right) \tag{11}$$

Decremental Memristance is given by

$$\frac{V_{\text{in}}(t)}{I_{\text{in}}(t)} = -\frac{\text{kq}(t)}{2C} R_1R_2 + \left(\left(\frac{V_{\text{ss}}}{2} + V_T\right) kR_1R_2 - R_1\right) \tag{12}$$

For analysing the behaviour of memristor emulator in frequency domain, input voltage is excited by applying sinusoidal signal with amplitude A_m. Memristance equation can be modified as

$$M(q(t)) = \frac{\pm\, k\, R_2 A_m}{2\omega\, R_1\, C\left(-1 \pm \left(\frac{V_{\text{ss}}}{2} + V_T\right) kR_2\right)^2} \propto \frac{1}{f\tau} \tag{13}$$

where τ is the time constant of the proposed emulator circuit represented as

$$\tau = \frac{\pm\, kR_2 A_m}{4\pi \text{fR}_1 C\left(-1 \pm \left(\frac{V_{\text{ss}}}{2} + V_T\right) kR_2\right)^2} \tag{14}$$

To validate the three fingerprint characteristics explained in [2], time constant criteria has to be satisfied.

(i) If frequency decreases, i.e., $\tau < 1/\text{f}$, then hysteresis characteristics property is lost as mentioned in [24].
(ii) If the frequency of the excitation voltage is increased, then the pinched hysteresis curve area decreases as

the τ value decreases. This is the second fingerprint mentioned in [2].

(iii) If frequency tends to be infinite, then the time variant portion disappears and the memristor behaves like a normal linear resistor. This is the third fingerprint mentioned in [2].

2.3 Nonideal analysis of proposed memristor emulator

Considering nonidealities at the port $V_x = \eta_1 V_{y1} - \eta_2 V_{y2}$, $I_{z1} = \rho_1 I_x$,$I_{z2} = \rho_2 I_x$,$I_{z-} = \rho_- I_x$, $I_{o\pm} = \lambda_\pm g_m V_{z1}$ and effect of parasitics at various terminals. The proposed memristor emulator with nonidealities is shown in Fig. 4. At higher frequencies, non idealities and parasitic resistance and capacitance comes into effect. R_x is the series parasitic resistance at X terminal, R_{y1}, R_{y2}, R_{z1}, R_{z2}, R_{z-}, R_{z+}, R_{o-} and R_{o+} are the parallel parasitic resistance at Y_1, Y_2, Z_1, Z_2, Z_-, Z_+, O_- and O_+ terminals respectively. C_{y1}, C_{y2}, C_{z1}, C_{z2}, C_{z-}, C_{z+}, C_{o-} and C_{o+} are the parasitic capacitances at Y_1, Y_2, Z_1, Z_2, Z_-, Z_+, O_- and O_+

terminals respectively. Considering $\eta_1 = \eta_2 = \eta$, Eq. (4) is represented as

$$V_x = \eta(V_{y1} - V_{y2}) = \eta V_{\text{in}}(t) \tag{15}$$

Transconductance gain at O± terminal is considered as

$$I_{o\pm} = \pm\lambda_\pm g_m I_{\text{in}}(t) R_{\text{eq1}} \tag{16}$$

where $R_{\text{eq1}} = R_{z1} || R_2 || \frac{1}{C_{z1} s}$.

The voltage at Z_2 is obtained as

$$V_c = \frac{q(t)}{C_1 + C_{z1}} = \frac{q(t)}{C_{\text{eq1}}} \tag{17}$$

Using Eq. (6), Substituting this value in Eq. (16)

$$I_{o\pm} = \pm\lambda_\pm \text{k}\left(\frac{q(t)}{2C_{\text{eq1}}} - \frac{V_{\text{ss}}}{2} - V_T\right) I_{\text{in}}(t) R_2 \tag{18}$$

Considering $p_1 = p_2 = p_+ = p_- = p$.

Port analysis at X terminal yields,

$$I_{o\pm} + \frac{I_{\text{in}}(t)}{\rho} + \frac{V_x}{R_{\text{eq2}}} = 0 \tag{19}$$

where $R_{\text{eq2}} = (R_x + R_1) || R_{o\pm} || \frac{1}{C_{o\pm} s}$.

The generalized Memristance equation is modified as

$$M(q(t)) = \frac{\mp k\lambda_\pm q(t) R_{\text{eq2}}}{2C_{\text{eq1}}} - \frac{R_{\text{eq2}}}{\eta\rho} \pm \frac{\lambda_\pm \text{k} R_{\text{eq1}} R_{\text{eq2}}}{\eta}\left(\frac{V_{\text{ss}}}{2} + V_T\right) \tag{20}$$

3 3. Simulation results and discussion

The implementation of the proposed emulator circuit using TSMC 180nm Level 7 MOSFET parameters in PSPICE environment is shown in Fig. 3. The aspect ratios of MOSFET used for active element DVCCTA is shown in Table 1. The DC power supply and bias Voltage(V_{bias}) is taken as ±0.9V, and -0.3V, respectively. However, the aspect ratios mentioned in Table 1 are chosen in a way so that all the transistors work in the saturation region. Furthermore, the resistance values are taken as R_1=12 kΩ and R_2=16 kΩ. The input current and voltage waveform to the applied to the memristor emulator is illustrated in Fig. 5 having a time period of 20 nsec for 5 cycles. Similar to the curve mentioned in [9], Fig. 5 illustrates the zero crossing of appied voltage and current. Likewise Pinched hysteresis loop [2] which is an important characteristic of any memristor circuit

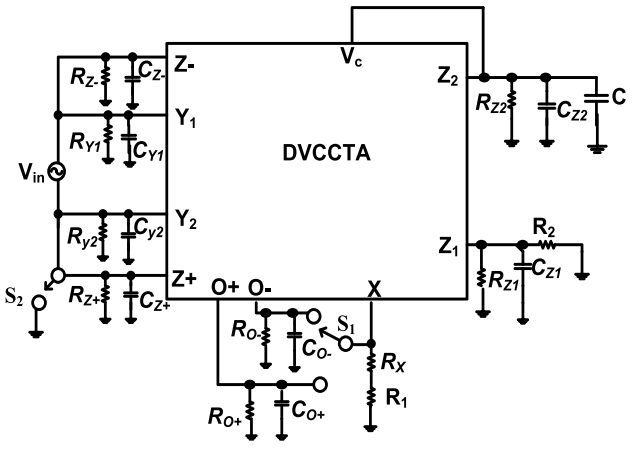

Fig. 4 Proposed floating/grounded memristor emulator circuit considering non ideality and parasitics

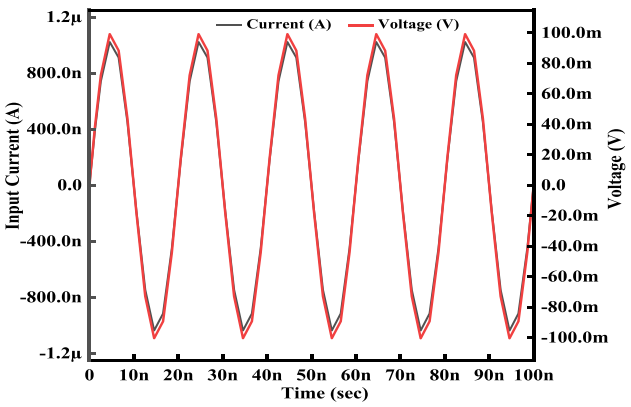

Fig. 5 Input current and Input voltage waveform observed for proposed Memristor emulator

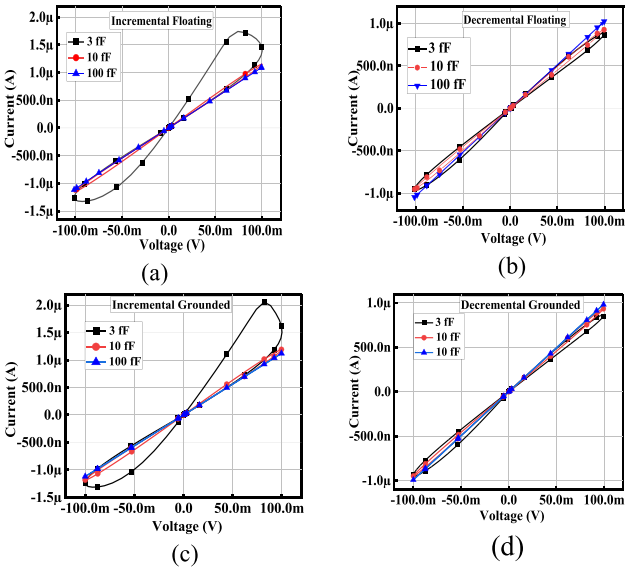

Fig. 6 Comparison of Pinched Hysteresis curve of proposed memristor emulator at 150 MHz for different capacitor values operating in **a** Floating type incremental **b** Floating type decremental **c** Grounded type incremental **d** Grounded type decremental

is depicted in Fig. 6 for varying capacitors, wherein Floating type incremental/ decremental configuration is shown in Fig. 6 a and b, and Grounded incremental/decremental in Fig. 6 c and d, respectively. From Fig. 3, it can be observed that switch S_2 regulates whether the emulator circuit will be grounded/floating type while S_1 for Incremental/decremental configuration. The direction of switches S_1 and S_2 is listed in Table 2. Figure 6 exhibits that the hysteresis lobe area decreases as the capacitor (C) value is increased which satisfies Eq. (14) mentioned in Sect. 2. Concordly, the value of the time constant (τ) decreases as the C is increased leading to a decrease in lobe area. In addition, Figs. 7 and 8 indicate the variation of the pinched hysteresis loop with frequencies (f) for incremental configuration operating in floating/grounded mode. It can be perceived that the area of the curve is maximum for lower f but for higher f, the curve area reduces and eventually became a straight line on further increase. As the f is increased such that $\tau < 1/f$, the pinched hysteresis curve property is lost and the memristor behaves like a normal resistor. It verifies the second and third criteria mentioned in [2] for any circuit to act like a memristor. It happens due to the reduction of τ mentioned in Eq. (14). The Pinched hysteresis loop for incremental and decremental configuration in Floating/Grounded case is illustrated in Fig. 9. It can be seen that the incremental mode has an enhanced loop area in comparison to the decremental mode. For due to τ being directly proportional to A_m mentioned in Eq. (14), the Pinched hysteresis loop is expanded with an increase in Amplitude A_m as shown in

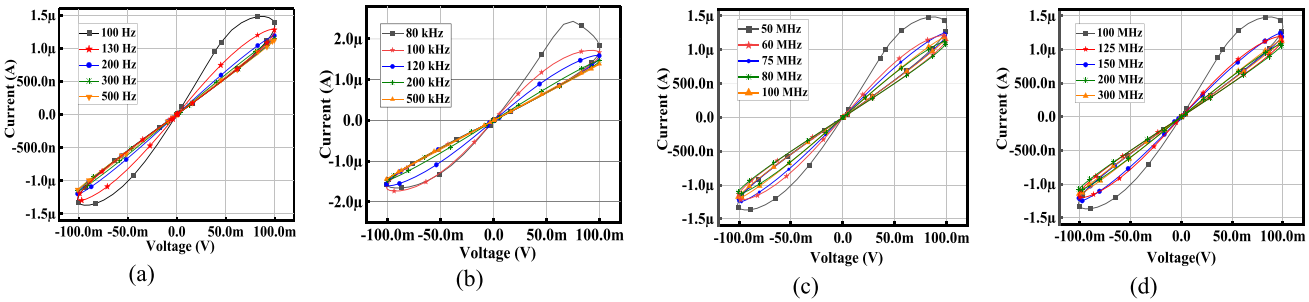

Fig. 7 Pinched Hysteresis Loop for varying Frequencies in Floating Incremental configuration **a** 100 -500 Hz at C = 5 nF **b** 80–500 kHz at C = 10 pF **c** 50–100 MHz at C = 10 fF **d** 100–300 MHz at C = 5 fF

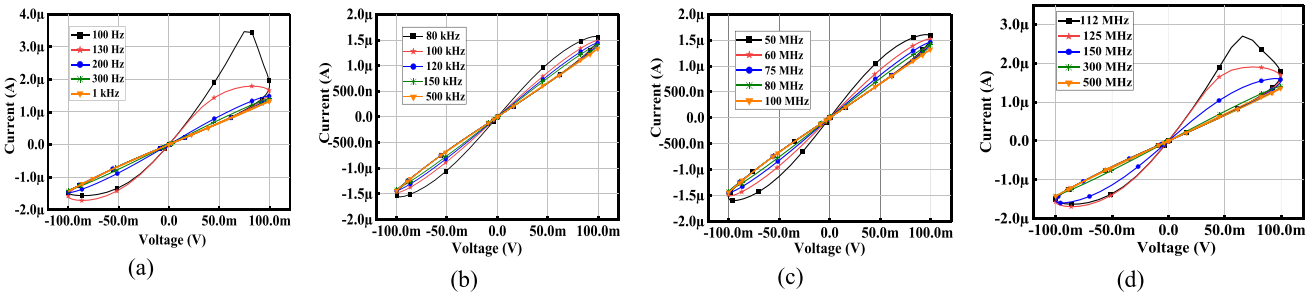

Fig. 8 Pinched hysteresis loop for varying frequencies in grounded incremental configuration **a** 100-1 kHz at C = 10 nF **b** 80-500 kHz C = 10 pF **c** 50–100 MHz at C = 15fF **d** 112–500 MHz at C = 8fF

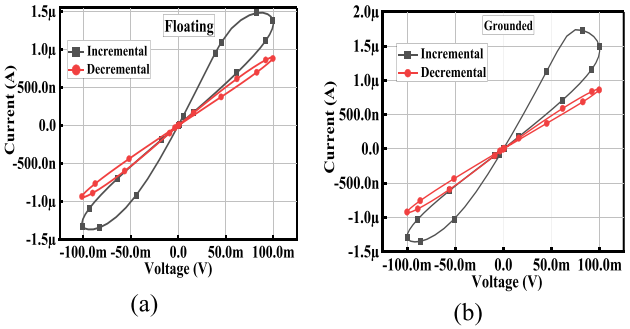

Fig. 9 Comparison of pinched hysteresis loop for incremental/ decremental configuration for **a** Floating type **b** Grounded type

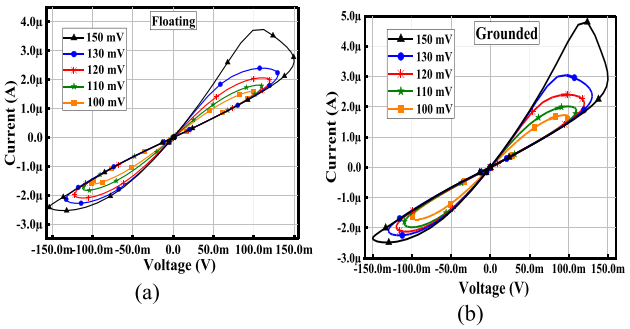

Fig. 10 Comparison of Pinched hysteresis loop for different applied amplitude Voltage A_m for **a** Floating Type **b** Grounded type

Fig. 10. The electronic tunability is checked by applying different V_{bias} to the memristor emulator circuit for floating/ grounded in Figs. 11 a and b, respectively. It can be seen that the curve area decreases as V_{bias} is increased. Another important 12(b) working in incremental and decremental configuration by applying 11 consecutive input characteristic of the memristor is the retention property, where the data are retained even in the absence of any input signal. This property is checked for both floating/grounded type in Fig. 12a and input voltage pulses with the time period of 167 nsec having 6% duty cycle. It can be observed from both the figures that memristance M(q(t)) remains unchanged in the absence of an applied voltage pulse. The memristance value is increased when the next pulse is applied in Fig. 12a and decreased for the decremental configuration in Fig. 12b. This proves that the presented memristor emulator shows non-volatility property.

4 Comparative study of proposed design with existing literature

The conclusions from Table 3 depict the comparison of the proposed design with existing literature as follows:

- [17, 22, 34–36, 38, 43] require more components to design memristor emulator circuits. However, [24] requires only one VDTA, and [39] requires one DXCCTA but it can be operated only in the floating configuration. The presented design requires single active component and few passive components to work as memristor emulator in both grounded and floating configuration.
- [20, 22, 34–36, 43] can be operated only in the grounded configuration while [17, 24, 38, 39] operate only in the floating configuration. Moreover, [18, 21, 40–42] can be operated in both the configuration. However, in [18, 21], and [40], separate circuits are needed for grounded and floating configuration due to which monolithic ICs operating in grounded/floating configuration cannot be manufactured. Simple switching allows the circuit to work in both floating and grounded configuration.
- Maximum frequency of operation for [17, 22, 35, 36, 38] is in the kHz range, and [18, 20, 21, 34, 40, 42] operate within 10 MHz range, with others operating upto 60 MHz range. The presented design operates upto

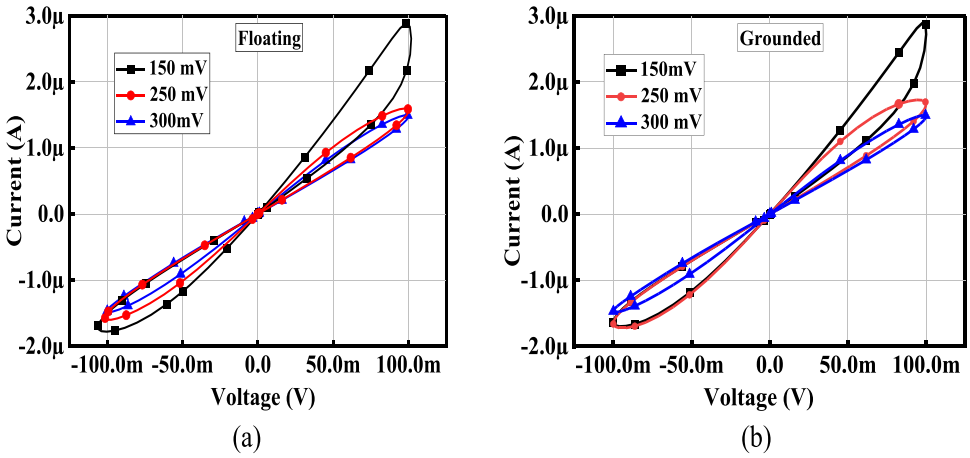

Fig. 11 Pinched hysteresis loop for different biasing voltages (V_{bias}) applied to **a** Floating type **b** Grounded type

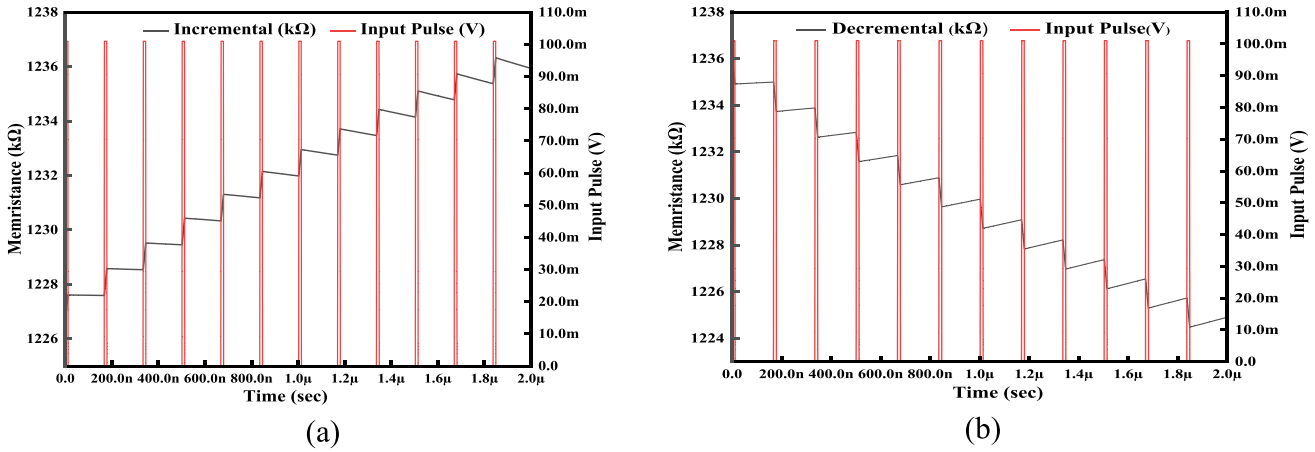

Fig. 12 Non volatility test done for floating/grounded configuration **a** Incremental topology **b** Decremental Topology

300 MHz range for the floating type and 500 MHz range for the grounded type.

- Compared to [17, 34–36, 43] power consumption of proposed memristor is less. In contrast, while the power consumption of the proposed design exceeds that of references [24, 39], and [41], it operates at a higher frequency, indicating a trade-off between power consumption and operating frequency in these cases. Also, for [24] only floating topology is proposed whereas proposed circuit can operate in both floating and grounded configuration.
- The proposed design uses less number of MOSFETs compared to references outlined in [17, 22] and [39].
- While comparing with [21] and [24], number of MOSFETs used in the proposed circuit is greater. However, both the literature requires separate circuit designs for the implementation of grounded and floating configuration thereby lacking generalized circuit design.

From all the factors, it can be observed that simple generic floating/grounded memristor working in incremental and decremental configuration is constructed in this paper with higher operating frequency.

5 Application in adaptive learning

Memristor's ability to mimic synaptic behavior has led to its application in neuromorphic circuits [24] and [45]. The memristor's resistance adjusts in accordance to the received electrical signals. This permits them to simulate the properties of synapses in biological neural networks. To better understand the primitive learning process and behavior of the brain, researchers are trying to imitate the learning process of simple unicellular organisms like amoeba. It can sense the change in environment i.e., humidity or temperature and slow down its speed. Next time when unfavorable condition occurs, amoeba slows down spontaneously. This learning behavior of amoeba can be used to train the neuromorphic circuit. The electronic RLC circuit depicting the amoeba's skill in recognizing patterns and anticipating future events is shown in Fig. 13a. The oscillation produced with resonant frequency f which is determined by the equation below

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{21}$$

Additionally, the memristor (M(q(t)) component encapsulates the memory mechanisms responsible for memory storage within the amoeba. The variation of temperature due to which amoeba moves is represented in the form of external Voltage i.e., input voltage spikes as given in Fig. 13b. The response i.e., velocity or motion of amoeba with respect to variation in temperature can be observed in Fig. 13c. The amoeba slows down in response to drop in temperature. To test the workability of the memristor, both incremental type and decremental type have been used and its response is presented in Fig. 13c with values chosen as $R = 800\Omega$, $L = 800$uH and $C = 130$ pF. It can be seen that amoeba slows down or oscillations are observed when the fourth spike in the input voltage is present. It can be observed that incremental configuration memristor emulator output response shows greater response value compared to decremental configuration. Therefore, functionality of the suggested circuit is verified by the neuromorphic circuit.

6 Conclusion

The charged-based memristor emulator is proposed in this paper, wherein a single current mode active element DVCCTA, two resistors and one capacitor are used. In addition, two switches are used to alter the mode of operation

Table 3 Comparison of proposed memristor emulator with existing literature

SN	Reference, Year	No. of active components	No of MOS FET	No. of passive components	Power supply	Power consumption	Tech	Inc/Dec	Maximum frequency	Grounded/floating
1	[17], 2014	4 AD844AN, 1 Opamp, 1 Analog Multiplier	NA	8 Resistors, 1 Capacitor	±15 V	1.8 W	BJT	Inc	Few Hz	Floating
2	[18], 2018	2 OTA,	34	1 Capacitor	±1.2 V	–	180 nm CMOS	Both	8 MHz/ 400 kHz	Both
3	[20], 2017	1 DVCCTA	29	3 Resistors, 1 Capacitor	±1.25 V	3.59 mW	250 nm CMOS	Both	1 MHz	Grounded
4	[21], 2017	1 CCTA	30	3 Resistors, 1 Capacitor	±1.5 V	–	250 nm CMOS	Both	10 MHz	Both
5	[22], 2017	1 CBTA, 1 Analog Multiplier,	> 50	2 Resistors, 1 Capacitor	±0.9 V	–	180 nm CMOS	Both	100 kHz	Grounded
6	[24], 2020	1 VDTA	16	1 Resistor, 1 Capacitor	±0.9 V	8 µW	180 nm CMOS	Both	50 MHz	Floating
7	[34], 2014	1 DDCC, 1 Analog Multiplier	> 50	2 Resistors, 1 Capacitor	±1.5 V	74.5 mW	350 nm CMOS	Both	1 MHz	Grounded
8	[35], 2015	2 AD844AN, 1 OTA	NA	3 Resistors, 2 Capacitors	±12 V	1.07 W	BJT	Both	Few KHz	Grounded
9	[36], 2015	2 AD844AN, 1 Analog Multiplier	NA	2 Resistor, 1 Capacitor	±10 V	0.509W	BJT	Both	160 kHz	Grounded
10	[38], 2016	4 AD844AN, 3 OTA	NA	6 Resistors, 1 Capacitor	±15 V	–	BJT	Inc	Few KHz	Floating
11	[39], 2022	1 DXCCTA	33	4 Resistors, 1 Capacitor	±1.2 V	4.7 mW	90 nm CMOS	Both	60 MHz	Floating
12	[40], 2020	1 CDTA, 1 OTA	30	1 Capacitor	±0.9 V	–	180 nm CMOS	Both	2 MHz	Both
13	[41], 2022	2 VDCC	46	2 MOSFET	±0.9 V	0.869 mW	180 nm CMOS	Both	50 MHz	Both
14	[42], 2023	1 VDBA, 1 OTA,	25	1 Capacitor	±0.9 V	-	180 nm CMOS	Both	8 MHz	Both
15	[43], 2020	1 CCII, 1 OTA	22	1 Resistor, 1 Capacitor	±1.2 V	9.567 mW	180 nm CMOS	Both	26.3 MHz	Grounded
16	This Work	1 DVCCTA	37	2 Resistors, 1 Capacitor	±0.9 V	4.84 mW	180 nm CMOS	Both	300 MHz-Floating, 500 MHz- Grounded	Both

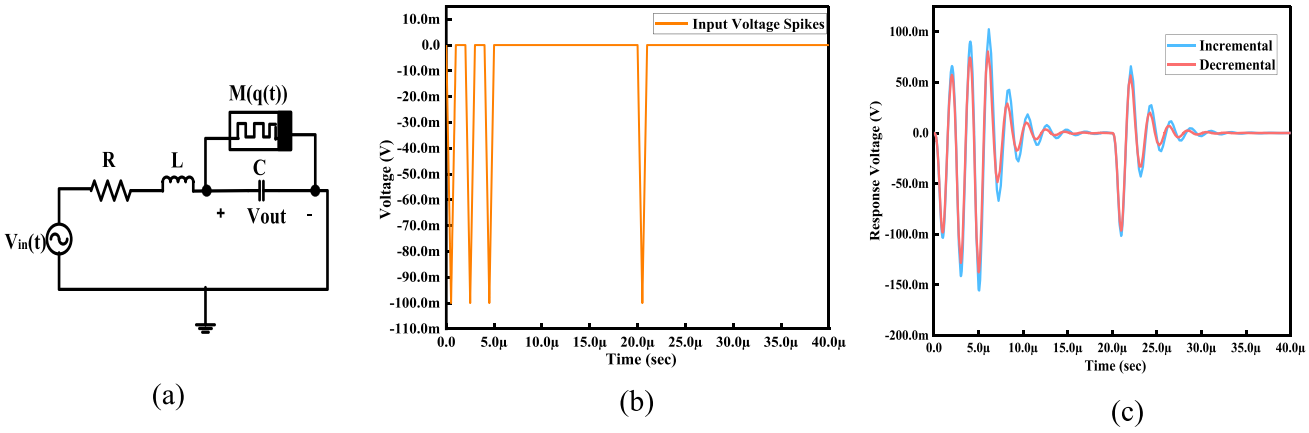

Fig. 13 **a** Circuit representing amoeba learning behavior. **b** Input temperature variation. **c** Output response of amoeba in incremental and decremental configuration

while one switch is used to change type to either floating or grounded. Another switch is used to change the configuration to incremental or decremental. Theoretical analysis performed in this paper and the procured simulation results agree with the derived time constant τ described in Sect. 2. Further, the behavior of parasitic resistance and capacitance on τ is also performed. The circuit presented here is electronically tunable *w.r.t.* bias voltage (V_{bias}). The effect of variation in input amplitude (A_m) for floating/grounded type is also studied. The memory retention property is tested by applying input pulse for incremental and decremental configuration. Finally, to check the feasibility of the presented design, was evaluated by incorporating it in neuromorphic circuit.

Acknowledgements The authors would like to acknowledge Swati Verma for her valuable insights and suggestions.

Funding This research was conducted without receiving any funding from public, commercial, or not-for-profit sectors.

Data availability All relevant data supporting the findings of this study are included within the article and its supplementary information files. However, raw data are available from the authors upon reasonable request and with the permission of the data providers.

Declarations

Conflict of interest The authors would like to assert that there are no conflicts of interest regarding this research study.

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