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Combinational logic circuits based on a power- and area-efficient memristor with low variability

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Abstract

The saturation of complementary metal–oxide–semiconductor (CMOS) technology in terms of area and power efficiency has given rise to advanced research on nanodevices. Memristors and their switching properties facilitate the implementation of various combinational logics and neural networks by potential replacement of the existing CMOS technology for edge computing devices. This work presents the design, implementation, and performance evaluation of memristor-based combinational logic circuits including adders, subtractors, and decoders via MATLAB Simulink and Cadence Virtuoso. In this work, we propose an optimized design of memristor-based combinational logic circuits and conduct a comparative study with the conventional method. The proposed memristor model is thoroughly validated experimentally for a high-density Y_2O_3-based memristive crossbar array and shows ultralow values in device-to-device and cycle-to-cycle variability. The power calculated from these circuits is reduced by more than 90% as compared to conventional CMOS technology implemented in Cadence Virtuoso. Moreover, the number of components utilized in the memristor-based logic circuits is significantly reduced in comparison to existing CMOS technology, which makes it more area-efficient and opens new avenues for the design and implementation of complex logic circuitry in few-micrometer scale.

Keywords Memristor · Transistor · CMOS · Combinational logic gates · Power-efficient · Digital electronics

1 Introduction

Many contemporary computer workloads, including artificial intelligence (AI) and scientific computing techniques, require the parallel processing of a large amount of data. Since the memory and computation units are separate, a significant amount of operational time and energy is needed for data transfer in the von Neumann architecture [1]. This serves as a basis for the majority of computer systems and is fairly inefficient for data-intensive computing [2]. Large-scale parallel designs, such as graphic processing units (GPUs), or specialized systems such as tensor processing units (TPU) have been implemented in an attempt to address this memory constraint in computing systems [3]. Currently, metal–oxide–semiconductor field-effect transistor (MOSFET) and complementary metal–oxide–semiconductor (CMOS) technology are the two main pillars providing advanced support in digital electronics and are the foundation of the mainstream computational paradigm [4].

Combinational logic circuits are widely utilized in several applications including calculators, digital measuring instruments, computers, digital processing, control automation,

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industrial processing, and digital communications [5]. However, current CMOS technology is limited according to Moore's law, and hence, new technology with low power and small area is being sought. A memristor is a two-terminal device which is a well-known technology, and its many advantages include electrical programmability [6], its nanoscale size [7], precise tunability [8], and ability to function as a resistive element on a variety of scales [9]. It is fully capable of performing both logic and memory operations in an efficient way [10], displaying low energy and power consumption and multibyte storage capability [11]. Additionally, memristors use pulse-based operation and adjustable resistance which are preferred for regulating the synaptic weights in neuromorphic computing processes. Memristor-aided logic (MAGIC) and material implication (IMPLY) memristor logic are the two aspects of pure memristor-based logic circuits [12]. However, due to structural complications, MAGIC cannot perform cascade connections between multiple logic gates. In IMPLY, operational time increases, as it requires multiple operation steps in the circuit [13]. Recently, to improve the logical state and reduce the power consumption, buffers are used which increase the required chip area [14]. By utilizing memristors in a circuit, one can easily address the limitations of current technology in terms of speed, energy, power and area to design efficient combinational logic gates. Several studies [13, 15, 16] have reported the implementation of "AND" and "OR" logic gates by utilizing memristor circuits or a combination of CMOS-memristor logics. In this paper, several combinational logic gates are implemented using a memristor model as proposed in Kumar et al. [17], which is inspired by the experimental results of Y_2O_3-based memristors and memristive crossbar arrays (MCAs) that display ultralow device-to-device (D2D) and cycle-to-cycle (C2C) variability [18]. The proposed analytical model effectively shows the digital transition between the high-resistance state (HRS) and low-resistance state (LRS) and vice versa.

This paper is organized as follows: Section 2 introduces the methodology, which includes the analytical memristor model with digital behavior in its current–voltage response, and also outlines the design procedure for various combinational logic gates. Section 3 presents the implemented combinational logic circuits and their results with logic truth tables. Section 4 describes the performance evaluation of the implemented logic circuits by considering various performance parameters such as number of components, area and utilized power. Section 5 summarizes the conclusion and future scope of the research work.

2 Analytical model

Nowadays, memristors are used in many applications such as memory [19], synapses [20], neuromorphic computing [21], deep neural networks [22], and logic gates [23]. Owing to their broad use in logic gates, the logic states "0" and "1" are represented by the switching states, i.e., HRS and LRS, of the memristor, respectively. In this work, an analytical model of a memristor is utilized in MATLAB Simulink and Cadence Virtuoso to verify its current–voltage (I–V) characteristics. The model is then integrated with other circuit components to perform logic operations with various combinational logic gates including half adder, full adder, half subtractor, full subtractor, and two-input and three-input decoders. A detailed comparison of these logic gates with existing CMOS technology is also discussed.

2.1 Memristor model

The proposed nonlinear model [17] is applicable to both unipolar and bipolar memristive systems. Here, Eq. (1) shows the relationship between current and voltage (I–V) of the memristor.

$$I(t) = \begin{Bmatrix} b_1 w^{a_1}\left(e^{\alpha_1 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), & V_i(t) \geq 0 \\ b_2 w^{a_2}\left(e^{\alpha_2 V_i(t)} - 1\right) + \chi\left(e^{\gamma V_i(t)} - 1\right), & V_i(t) < 0 \end{Bmatrix} \tag{1}$$

The parameters a_1 and a_2 show the effects of the state variable on the device current for positive and negative applied voltages, respectively. The fitting parameters b_1 and b_2 define the slope of conductance in I–V characteristics, α_1 and α_2 denote the hysteresis loop area controlling parameters, and the state variable is represented by w. The net electronic barrier of the memristive device is denoted by the parameters χ and γ, and the applied input voltage is $V_i(t)$.

$$f(w) = \log \begin{Bmatrix} (1+w)^P, & 0 \leq w \leq 0.1 \\ (1.1)^P, & 0.1 < w \leq 0.9 \\ (2-w)^P, & 0.9 < w \leq 1 \end{Bmatrix} \tag{2}$$

Here, Eq. (2) defines the piecewise window function ($f(w)$) which ensures that w ϵ [0,1]. Equation (3) illustrates the state variable derivative in the time domain, with A and m denoting the effect of the input voltage on the state variable.

$$\frac{\mathrm{d}w}{\mathrm{d}t} = A \times V_i^m(t) \times f(w) \tag{3}$$

However, in the past several years, different memristor models have been reported [7, 24, 25] which have shown compatibility on different programming platforms. Here,

Table 1 Comparison between our proposed model with others reported models

Model	Device type	State variable	Control mechanism	Simulation compatible
Linear ion drift [7]	Bipolar	$0 \le w \le D$ doped region physical width	Current	SPICE
Nonlinear ion drift [24]	Bipolar	$0 \le w \le 1$ doped region normalized width	Voltage	No
Yakopcic [25]	Bipolar	$0 \le w \le 1$ not explained physically	Voltage	SPICE/Verilog/MAPP
Our model [17]	Unipolar/bipolar	$0 \le w \le 1$ validated with experimental data [17]	Voltage	MATLAB/Cadence Virtuoso

Table 1 effectively shows the comparison and fundamental difference between our proposed model and other reported models [7, 24, 25]. It should be noted that the piecewise window function utilized offers better controllability over the nonlinear analytical model in terms of bipolar resistive switching, effectively applicable for a lower input voltage window, utilizes minimum parameters as a degree of freedom, and offers better tunability in device conductance which further enhances the ability of the proposed analytical model to perform both analog and digital logic operations. Furthermore, its experimental validation proves its real-time application with lower variability as added superior advantages in its novelty, as compared to the reported data in the literature [17].

2.2 Design procedure

To design and implement the various combinational circuits, the aforementioned nonlinear analytical model is used to create a memristor element on MATLAB Simulink and Cadence Virtuoso. The sinusoidal input voltage waveform is utilized to obtain the pinched hysteresis resistive switching response with perfect zero crossing at the origin. Here, it should be noted that some valid modifications have been incorporated into the parameter values to obtain the perfect digital behavior as compared to analog response, as reported previously [17] and outlined in Table 2.

Further, to investigate the memristive behavior with digital pulse, a rectangular voltage input pulse with an amplitude of +2 and 0 V is applied. Here, the amplitude of +2 V is referred to as logic "1" and 0 V is referred to as logic "0". Figure 1 shows the simulated output waveform for the digital logic design, and the pinched hysteresis loop (Fig. 1d) in the I–V characteristics clearly shows the abrupt transition from HRS to LRS and vice versa, which confirms the digital behavior of the memristor and makes it more suitable for digital logic design. Here, it should be noted that in the bipolar memristive behavior, the SET ("ON") state appears at the positive voltage side while the RESET ("OFF") state appears at the negative voltage side. The resistance values of HRS and LRS are 0.526 MΩ and 0.0527 MΩ, respectively. To design and simulate the inverter and other combinational circuits, 180-nm CMOS technology is utilized along with a memristor. Dong et al. [26] reported that using the memristor-CMOS hybrid logic circuit efficiently reduced the circuit delay.

3 Circuit implementation, results and discussion

As discussed earlier, the MATLAB Simulink tool is utilized to design and implement all the combinational logic circuits, where the memristor works as a switching device and "ON" and "OFF" according to the input voltage amplitude. The output current of the memristor is denoted by I_{out}. Here, Eq. (4) shows the calculation approach adopted for logic "1" and "0".

$$\left.\begin{array}{l}\text{For Logic "1"} : V_{out} = R_{on} \times I_{out} \\ \text{For Logic "0"} : V_{out} = R_{off} \times I_{out}\end{array}\right\} \quad (4)$$

Equations (5a) and (5b) show the Boolean expressions, while Table 3 depicts the combined truth table for a half adder and half subtractor, respectively. Figure 2 shows the

Table 2 Comparison of values of parameters for analytical modeling and its physical interpretation

Parameters	Modified values	Values in [17]	Physical significance
b_1	1.59×10^{-7}	6.7×10^{-7}	Experimental fitting parameter
a_1	1.5	1.5	Degrees of influence of the state variable
α_1	1.6	0.8	Hysteresis loop area controlling parameters under positive bias
χ	1×10^{-11}	1×10^{-11}	Magnitude of ideal diode behavior
Υ	1	1	Diode parameters like thermal voltage and ideality factor
A	5×10^{-2}	3×10^{-4}	Control the effect of the window function
m	5	5	Control the effect of input on the state variable
p	5	1.5	Bounding parameter for window function between 0 and 1

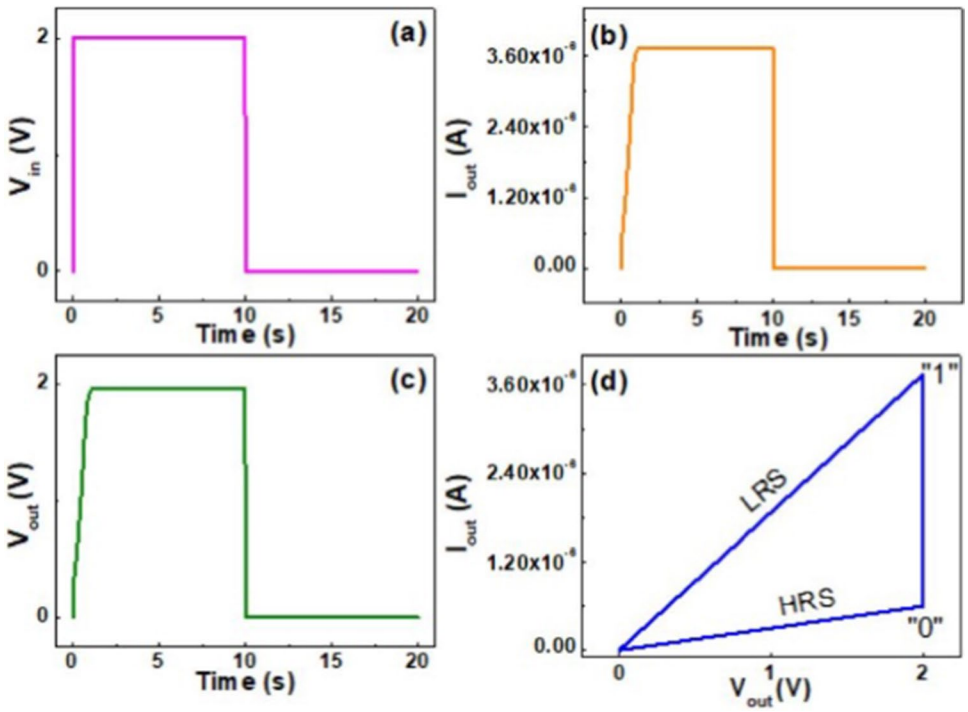

Fig. 1 **a** Input voltage, **b** output current, **c** output voltage, **d** resistive switching response of memristor (positive half cycle)

Table 3 Truth table for half adder and half subtractor

Input 1	Input 2	Sum	Carry	Difference	Borrow
0	0	0	0	0	0
0	1	1	0	1	1
1	0	1	0	1	0
1	1	0	1	0	0

designed circuit layouts in MATLAB Simulink for the half adder (Fig. 2a) and half subtractor (Fig. 2b). Here, to perform the logic operations, two different input voltages, +2 and 0 V, are applied with different duty cycles of 0.5 and 0.25 to create the input logic ({0,0}, {0,1}, {1,0}, {1,1}).

The output logic combinations are presented in Table 3. Table 4 shows the design process flow during logic computation in the case of half adder. Figure 3 shows both input voltage pulses (Fig. 3a), sum and carry outputs (Fig. 3b) and difference and borrow (Fig. 3c) for a half adder and half subtractor, respectively.

$$\left.\begin{aligned}\text{Sum} &= X \oplus Y \\ \text{Carry} &= X.Y\end{aligned}\right\} \tag{5a}$$

$$\left.\begin{aligned}\text{Difference} &= X \oplus Y \\ \text{Borrow} &= \overline{X}.Y\end{aligned}\right\} \tag{5b}$$

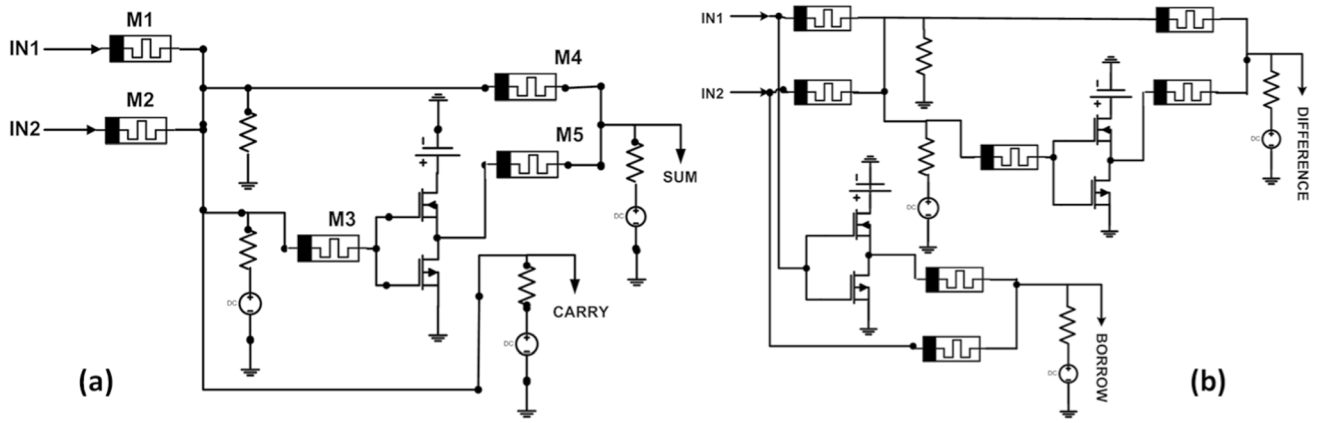

Fig. 2 Memristor-based designs for **a** half adder and **b** half subtractor

Table 4 Computation design of half adder using memristors

IN1/ IN2/Components	0,0	1,1	1,0	0,1
M1/ M2	HRS/HRS	LRS/LRS	LRS/HRS	HRS/LRS
M4	HRS	LRS	LRS	LRS
M3	HRS	LRS	HRS	HRS
CMOS logic output	1	0	1	1
M4	LRS	HRS	LRS	LRS
Sum logic output	0	0	1	1
Carry logic output	0	1	0	0

To design and implement a full adder circuit, two half adders and one additional "OR" gate is utilized, where the "OR" gate is used for carry output, as depicted in Fig. 4a. Similarly, for the full subtractor, two half subtractors and one additional "OR" gate are used, as shown in Fig. 4b. Here, three different duty cycles of 0.5, 0.25, and 0.125 are imposed on the designed circuit to obtain the logic inputs ({000}, {001}, {010}, {011}, {100}, {101}, {110}, {111}). The output logic combinations are presented in Table 5. Figure 5 shows the three input voltage pulses (Fig. 5a), sum and carry outputs (Fig. 5b), and difference and borrow (Fig. 5c) for full adder and full subtractor, respectively.

$$\left.\begin{aligned} \text{Sum} &= X \oplus Y \oplus Z \\ \text{Carry} &= X.Y + (X \oplus Y).Z \end{aligned}\right\} \tag{6a}$$

$$\left.\begin{aligned} \text{Difference} &= X \oplus Y \oplus Z \\ \text{Borrow} &= \overline{X}.Y + \overline{X \oplus Y}.Z \end{aligned}\right\} \tag{6b}$$

For the 2:4 decoder circuit implementation, a similar input voltage scheme is applied as utilized in the half adder and half subtractor. Here, two 1-bit inputs are applied to the four memristor-based "AND" gates to perform the decoder operation according to Eqs. (7a–7d). Figure 6 shows the circuit layout implemented for the 2:4 decoder, while Fig. 7 shows the results for the 2:4 decoder. Table 6 shows the truth table for the 2:4 decoder circuit. Further, to extend the functionality, a 3:8 decoder is also implemented, as shown in Fig. 8, and the results are displayed in Fig. 9 while Table 7 shows the truth table of 3:8 decoder.

$$\text{Output 1} = A.B \tag{7a}$$

$$\text{Output 2} = A.\overline{B} \tag{7b}$$

$$\text{Output 3} = \overline{A}.B \tag{7c}$$

$$\text{Output 4} = \overline{A.B} \tag{7d}$$

4 Performance evaluation

In this section, a performance evaluation for the implemented combinational circuits is presented. The performance evaluation is based on the various critical circuit parameters such as power utilized, circuit area, and the total number of components used in the respective circuit design. By considering the aforementioned parameters, here we discuss each one in detail.

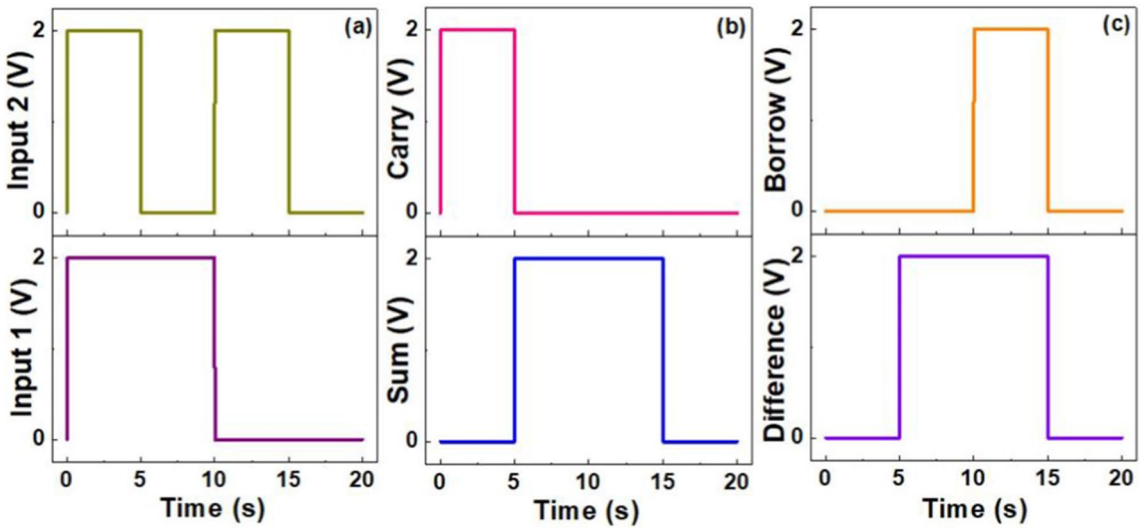

Fig. 3 **a** 2 Input waveforms, **b** output waveform of a half adder circuit, and **c** output waveform of a half subtractor circuit using memristors

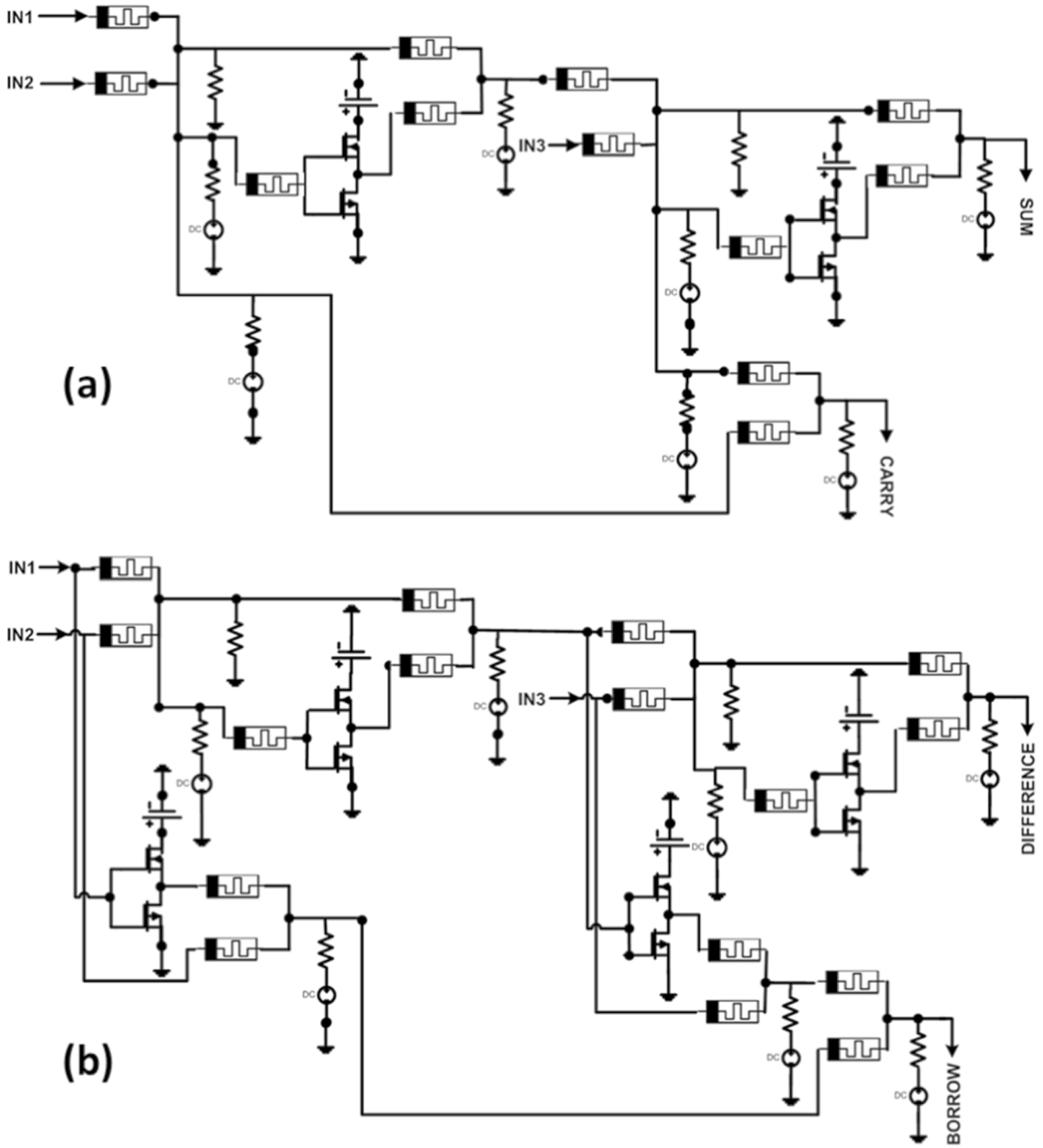

Fig. 4 Memristor-based combinational circuit designs for **a** full adder and **b** full subtractor

Table 5 Truth table for full adder and full subtractor

Input 1	Input 2	Input 3	Sum	Carry	Difference	Borrow
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1

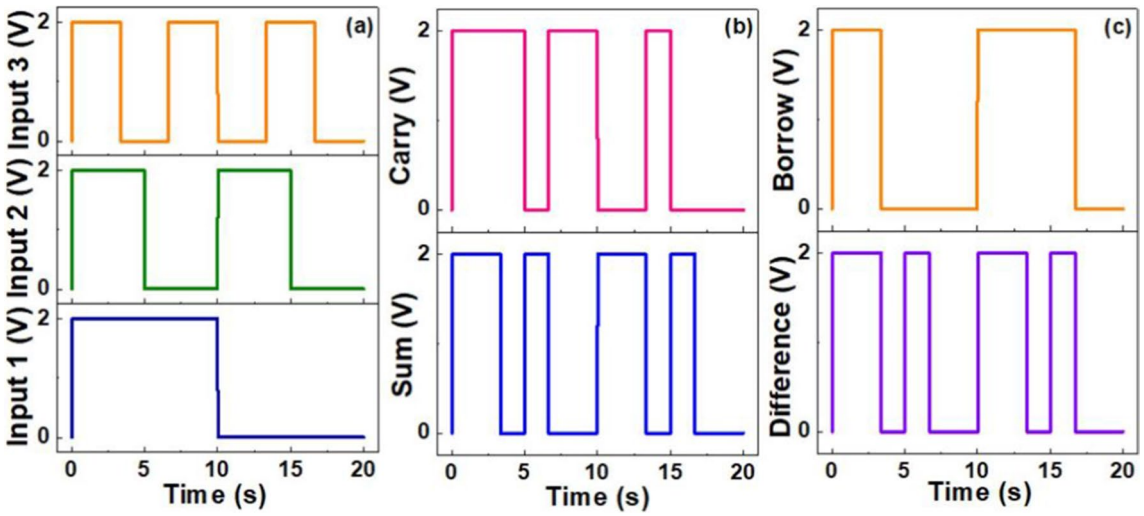

Fig. 5 **a** Three-input waveforms, **b** output waveform of full adder circuit, and **c** output waveform of full subtractor circuit using memristors

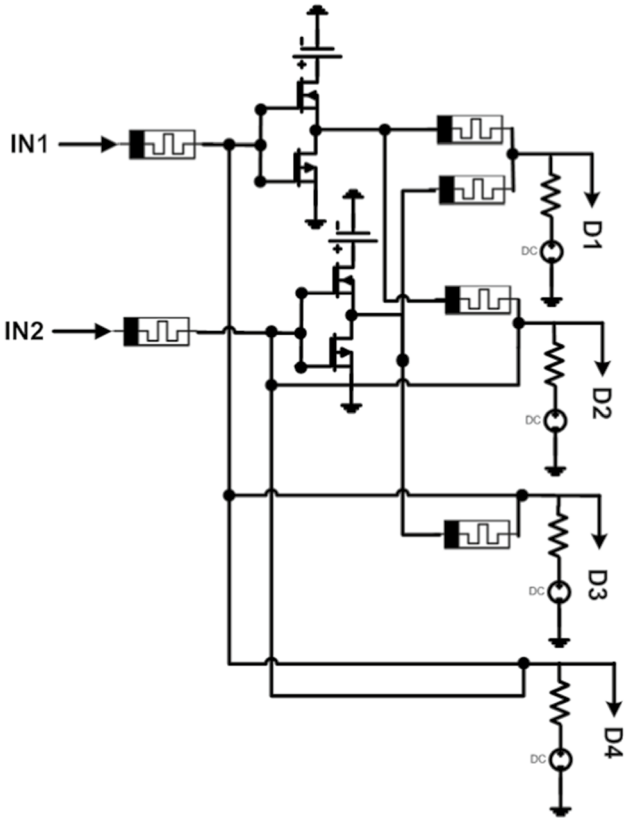

Fig. 6 Implemented circuit for 2:4 decoder using memristors

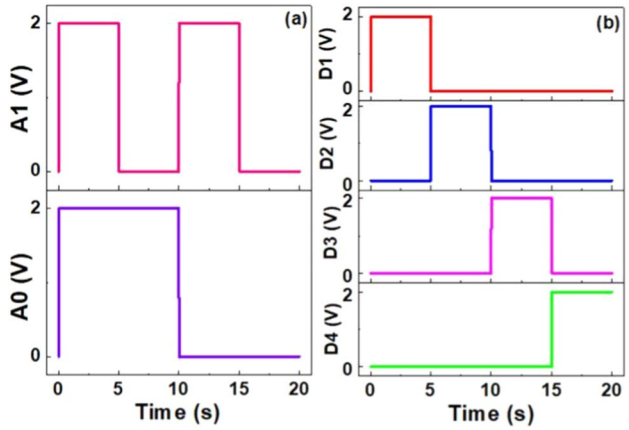

Fig. 7 **a** Two-input waveforms and **b** output waveform of a 2:4 decoder circuit using memristors

Table 6 Truth table for 2:4 decoder

Inputs		Outputs			
*A*0	*A*1	*D*1	*D*2	*D*3	*D*4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

4.1 Component comparison

Here, Table 8 shows a comparison between the number of memristors and CMOS inverters used in memristor-based combinational logic gates with conventional CMOS technology. It is observed that the memristor-based combinational logic circuits require a significantly smaller number of components than that required for only transistor-based conventional circuits.

As observed from the comparison in Table 8 the memristor-based logic shows a significant improvement in the utilized components to implement the combinational circuits. Importantly, the utilized circuit power and area are

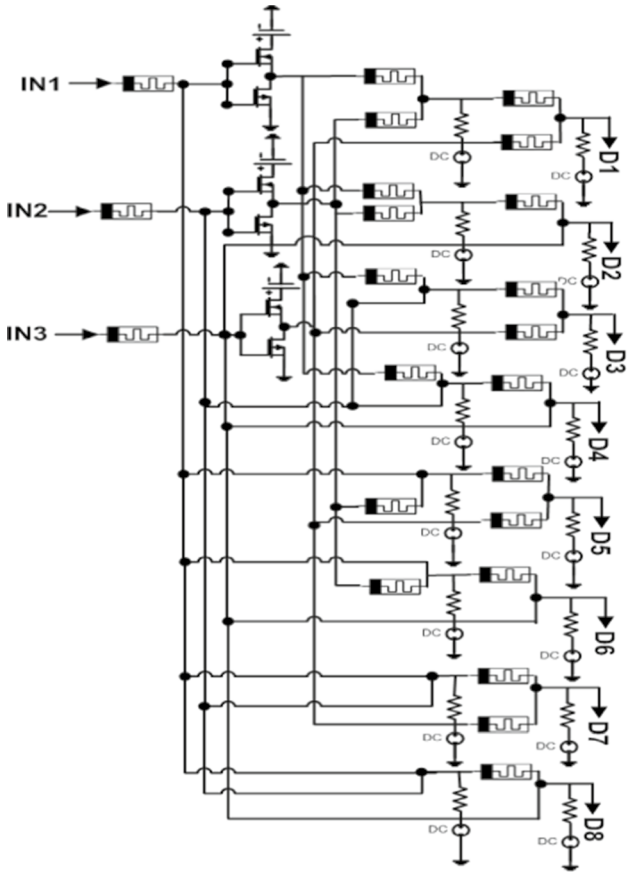

Fig. 8 Implemented circuit for 3:8 decoder using memristors

directly related to the number of utilized components in the logic circuits.

4.2 Area calculation

The area of the memristor-based combinational logic circuits has been calculated using layout calculation rules, as reported by Kang et al. [27]. Here, the area of the memristor is considered as 9 nm^2 [28], while the area of MOSFET is calculated as 1.06 μm^2. The total area of the memristor is much smaller than the total area covered by the MOSFET, and the memristor can be implemented on a polysilicon layer of the MOSFET. Therefore, 1000 memristors can be fabricated on the same chip-level area as occupied by a single CMOS [16, 29]. Figure 10 shows a comparison of the area of the memristor-based circuits and CMOS-based circuits, in which memristor-based circuits occupy significantly less area due to their nanometer scale as compared to CMOS.

4.3 Power comparison

The power consumption of the circuits is another important parameter when designing the circuit. For the memristor-based combinational circuits, power is calculated by integrating the product of the output voltage and the summation of the input currents of the circuit. Figure 11 shows the worst-case power comparison between memristor-based combinational logic and CMOS-based combinational logic circuits. Here, it should be noted that the CMOS-based combinational logic circuits are implemented in Cadence Virtuoso by adopting 180-nm CMOS technology. As observed from the calculation, the

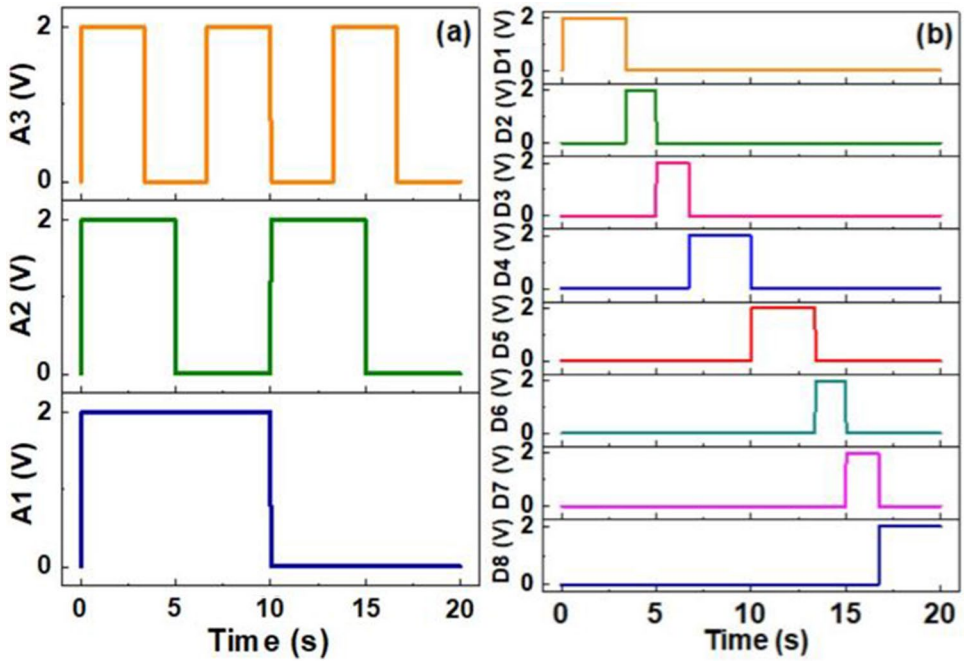

Fig. 9 **a** Three-input waveforms, **b** output waveform of 3:8 decoder circuit using memristor

Table 7 Truth table for 3:8 decoder

Inputs			Outputs							
*A*1	*A*2	*A*3	*D*1	*D*2	*D*3	*D*4	*D*5	*D*6	*D*7	*D*8
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table 8 Component comparison with area

Implemented logic circuits	Memristor-based logic gates		Only transistor-based logic gates		Improvement (%)
	No. of memristors	No. of CMOS inverters	No. of MOSFET	No. of CMOS inverters	
Half adder (AD)	5	1	10	2	50
Full adder (FA)	12	2	22	3	44
Half subtractor (HS)	7	2	10	3	30.7
Full subtractor (FS)	16	4	22	4	23.07
2:4 decoder (D)	6	2	32	2	82.35
3:8 decoder (D)	22	3	64	3	74.62

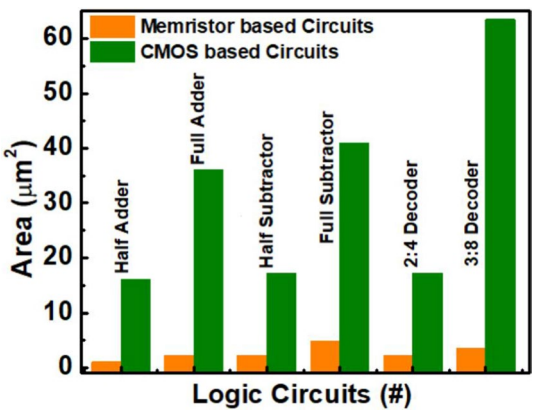

Fig. 10 Area comparison of memristor-based and CMOS-based logic circuits

memristor-based logic circuits consume much less power during operation than CMOS-based logic, which further strengthens the argument for using the memristor technology for various logic applications.

5 Conclusion and future outlook

In this work, we have utilized our proposed nonlinear memristor analytical model to design and implement various combinational logic circuits via MATLAB Simulink and Cadence Virtuoso. The model is validated based on experimental demonstration using low-variance in-house-fabricated memristors and MCA. The resistive switching response obtained shows clear digital behavior, which makes it a suitable candidate for digital logic design. Moreover, the memristor-based combinational logic circuits show significantly better performance in terms of the number of components, total circuit chip area, and power utilized as compared to those for the existing CMOS-based combinational logic circuits wherein 180-nm CMOS technology has been used. Therefore, the designed circuits are highly reliable for use in future complex circuits and integrated circuits. This work can be further extended by designing complex digital circuits such as flip-flops, and counters. Furthermore, the proposed methodology and circuit design approach can be useful for implementing power- and area-efficient complex circuitry for amplifiers, oscillators, and neuromorphic networks.

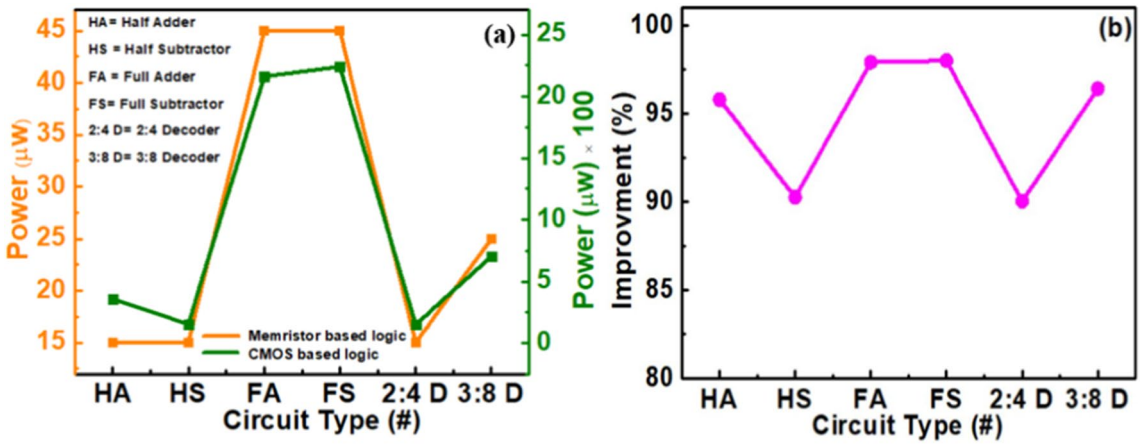

Fig. 11 Power consumption in **a** memristor-based and CMOS-based combinational logic circuits. **b** Improvement in power consumption in memristor-based combinational logic circuits as compared to those in only CMOS-based logic circuits

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Data availability The paper has no associated data.

Declarations

Conflict of interest The authors declare no conflict of interest.

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