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Phenomenological modeling of memristor fabricated by screen printing based on the structure of Ag/polymer/Cu

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Abstract

The attributes of memristors such as their non-volatile nature, simple structure, no leakage current, and fast switching speed present enormous opportunities for various analog and digital applications. It is imperative to develop an accurate physical model of the memristor in order to design digital applications. Hitherto published memristor modeling approaches do not match the practical memristor dynamics. In this work, a new model is developed by considering Schottky contact at the metal–insulator–metal (MIM) interfaces, and a novel memristor is fabricated to validate the proposed model. A bead polymer based on methyl methacrylate and *n*-butyl methacrylate (MMBM) is first used to explore the resistive switching properties of the device. A cost-effective screen printing technique is demonstrated to deposit the resistive switching layer for the fabrication of the memristor. The resistive switching behavior is observed in the sandwiched layer with a silver (Ag) top electrode and copper (Cu) bottom electrode. The surface morphology and electrical characteristics of the fabricated device are investigated by scanning electron microscopy and two-point probe resistivity measurement. The results confirm the formation of the Schottky barriers at the MIM interfaces of the fabricated device. The proposed model is compared with the device described in this paper having an error of 0.7609 (in terms of the relative root-mean-square error). Moreover, a NOR logic gate is simulated for the circuit simulation of the proposed model. This will pave the way for new digital design applications based on the memristor.

Keywords Schottky · Resistive switching · Screen printing · Polymer

1 Introduction

The semiconductor industry is growing by leaps and bounds due to progress in both micro and nanodevices over the years [1]. The electronics market has inevitably developed after the revolutionary invention of the transistor at Bell laboratories by American Telephone and Telegraph (AT&T) in 1947 [2]. Transistors have transformed the semiconductor industry with the continued enhancement of electrical switching and amplification properties, replacing the bulky and unreliable vacuum tubes in computers and circuit applications [3]. In this era, digital circuits are based on complementary-metal-oxide-semiconductor (CMOS) technology. Currently, the size of the transistor has reached 7 nm, i.e., only a few atoms [4]. Nowadays, CMOS technology is approaching its physical limits [5]. Furthermore, the complex structure of CMOS technology increases the cost per bit for digital design applications, and the downscaling of the transistor channel length gave rise to leakage current [6, 7].

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The memristor (memory resistor) can be used as the building block for logic gates and memory [8, 9]. It does not have problems like leakage current and size [10]. Its structure is very simple as compared to the complex structure of CMOS technology. In 1971, the theoretical concept of the memristor was introduced by Professor Leon Chua [11], but the physical realization of the memristor remained unresolved for nearly 40 more years [12]. Hewlett-Packard (HP) serendipitously observed the pinch hysteresis loop (PHL) in the crossbar nanoscale memory array, which led to unprecedented uproar in industry and research after the groundbreaking discovery of the physical realization of the memristor. Due to its unique electrical current–voltage (I–V) characteristics and novel simple structure, it has been widely used in different applications [8, 9, 13]. Resistive random access memory (ReRAM), flash memory, chaos circuits, biomimetic circuits, electrochemical metallization memory, magneto-resistive memory, cellular neural networks, recurrent neural networks, ultra-wideband receivers, adaptive filters, oscillators, programmable threshold comparators, Schmitt triggers, amplifiers, and logic gates have all been developed based on memristors [14–22]. Different mathematical models of memristors have been reported in the literature; however, these models are not sufficiently accurate in terms of their physical dynamics [23–28]. The existence of metal and insulator at both interfaces is not considered in the memristor models. Therefore, the reported models are not suitable because they lack the tunneling mechanism at both interfaces and therefore cannot accurately predict experimental behavior. The existing mathematical models of memristors deviate from physical mechanisms in real-time devices. Thus, any developer who wants to design a phenomenological model for the memristor must consider the metal–insulator barrier.

The PHL of the memristor has already been observed in experiments using different materials. Binary oxides, perovskite oxides, complex molecular materials, mixtures containing inorganic nanoparticles, and organic–inorganic interfaces have been proposed as the most suitable candidate for the switching layer of the memristor [29–36]. The fabrication of the sandwiched layer is considered the core of the memristor, and various techniques can be used to deposit this active layer. The sol–gel method, atomic layer deposition (ALD), anodization, and sputtering are the main methods for fabricating the switching layer. Most fabrication techniques have their inherent strengths and weaknesses. Limitations observed in previously reported fabrication techniques include infeasibility of mass production, high cost, radiation effects, time-consuming fabrication process, and expensive switching layer material. In this work, a novel memristor fabrication technique is presented to address these limitations in existing device fabrication methods. The screen printing technique is used to deposit the resistive switching layer, while bead polymer based on methyl methacrylate and *n*-butyl methacrylate (MMBM) is used as the active layer. To the best of our knowledge, there are no previous reports on the use of the screen printing technique and the above-mentioned switching material to observe the PHL of current and voltage in the memristive device. The screen printing technique is simple, durable, and environmentally friendly. The main objectives of this research work are as follows:

1. Development of a phenomenological model of a memristor with consideration of MIM interfaces.
2. Fabrication of a novel memristor using the screen printing technique to validate the phenomenological model of the memristor.

The remainder of the paper is organized as follows. Section 2 reviews the literature in detail. A novel physical model of the memristor is explained in Sect. 3. Section 4 describes the experimental work for the in-house fabrication of the novel memristor and its results. A summary is provided in Sect. 5.

2 Literature review

2.1 Modeling of the memristor

In order to apply memristive devices for essential applications, the development of an accurate memristor model is imperative. The model should preferably be simple, intuitive, and closed-form. The different models of memristors proposed in the literature are discussed as follows:

2.1.1 Linear drift model

HP coined the concept of memristor modeling in 2008 based on a variable resistor [12]. They established a link of the physical device with the mathematical model of the memristor, which is known as the linear drift model (LDM) [12]. For comparison with the LDM, a titanium dioxide (TiO_2) memristor was fabricated. In the TiO_2-based memristor, the TiO_2 bilayer acts as the switching layer deposited between the platinum (Pt) electrodes. The TiO_2 bilayer further comprises two layers: an oxygen-deficient TiO_{2-x} referred to as the doped layer, and a perfect TiO_2 layer referred to as the undoped layer. The resistance of TiO_{2-x} is considered the *ON*-state resistance of the device, whereas the resistance of TiO_2 is considered the *OFF*-state resistance of the device. HP described the switching mechanism of these devices as resistive switching. Mathematically, the current control memristor for circuit analysis is defined in Eq. (1).

$$V = R(x)I, \tag{1}$$

where x is a state variable and R is general resistance that is dependent on x. In the LDM, R_{on} (doped region) and R_{off} (undoped region) are connected in series. The total resistance R_T of the memristor is calculated by Eq. (2).

$$R_T = R_{\text{on}}(x) + R_{\text{off}}(1 - x), \tag{2}$$

When the external voltage is applied, the oxygen vacancies drift with average dopant mobility μ_v. The boundary drifts between the doped and the undoped regions with an average velocity as defined in Eq. (3).

$$\frac{\mathrm{d}x}{\mathrm{d}t} = \frac{\mu_v V(t)}{D}, \tag{3}$$

where μ_v is the average mobility and D is the total length of the memristor device. By applying positive voltage, oxygen vacancies drift from the TiO_{2-x} to the TiO_2 region. Hence, the width of TiO_{2-x} is increased and the memristance is decreased, due to which the current is increased, switching the device from the *OFF* state to the *ON* state. The device memristance is defined in Eq. (4).

$$M(q) = R_{\text{off}}(1 - \mu_v \frac{R_{\text{on}}}{D^2} q(t)). \tag{4}$$

The device's conducting width and memristance exceed its physical dimensions in this model [12]. Therefore, an accurate mathematical model is critically needed to address these challenges. Different window functions are reported in the literature to address these challenges.

2.2 Window function

The LDM simulations revealed erroneous results, showing conducting width and memristance exceeding the device's physical dimensions [12]. Thus, a precise model is needed which can address these issues. Various window functions are suggested in the existing literature to solve the nonlinearity issue and boundary limits. The drift velocity ($\frac{\mathrm{d}x}{\mathrm{d}t}$) of nonlinear dopant can be controlled by introducing window function $f(x)$ in Eq. (5).

$$\frac{\mathrm{d}x}{\mathrm{d}t} = \frac{\mu_v V(t)}{D^2} f(x). \tag{5}$$

2.2.1 Prodromakis window function

Prodromakis et al. [37] presented a new window function with two parameters as defined in Eq. (6).

$$f(x) = j[1 - \{(x - 0.5)^2 + 0.75\}]^{2p}, \tag{6}$$

where the parameter j is used for scalability and the parameter p is used for controllability. The terminal state problem is resolved using this window function. This window function provides the linkage between linear and nonlinear models, but it is very complex. Its complexity increases as the value of p increases, which will limit its applications in digital computing.

2.2.2 Biolek's window function

An alternative window function presented by Biolek is defined by Eq. (7).

$$f(x) = 1 - (x - sgn(-I))^{2p}. \tag{7}$$

The terminal problem is addressed by introducing the new function $sgn(I)$ by the Biolek window function [38]. However, the complexity of this window function is increased due to the new $sgn(I)$ function.

2.2.3 Joglekar's window function

The Joglekar window function [39] is defined in Eq. (8).

$$f(x) = 1 - (2x - 1)^{2p}, \tag{8}$$

where p is a positive exponent parameter. The drift velocity over the whole length of the device is regulated using the control parameter (p). When the value of p is smaller, the rate of change in x is also low. As p approaches infinity, it reduces to LDM. The parabola curve of the window function changes to a rectangular curve with an increase in the value of p. However, it also suffers from the computational complexity problem.

2.2.4 Strukov's window function

Strukov et al. introduced a novel window function for LDM [12], which resolves the problem of the boundary effect. It depicts the nonlinear drift close to the boundaries. Strukov's window function is given in Eq. (9).

$$f(x) = x - x^2. \tag{9}$$

Simple mathematical expressions make this window function computationally efficient as compared to other reported window functions.

2.2.5 Nonlinear ion drift model

Practical memristive devices show highly nonlinear behavior due to their nanoscale structure. The window function models significantly deviate from the behavior of the fabricated devices. For that, more appropriate models are proposed in the literature. In the nonlinear ion drift model proposed in

[40], Eq. (10) determines the current–voltage relationship based on the experimental results.

$$i(t) = \omega(t)^n(\beta \sinh(\alpha.v(t))) + (\chi[\exp(\gamma.v(t)) - 1]), \tag{10}$$

where α, β, γ, and χ are the experimental fitting constants. The exponent n shows the influence of the state variable $\omega(t)$ on the current. In this model, asymmetric PHL is assumed. When the memristor is in the *ON* state, the $\omega(t)$ approaches 1, as the current is dominated by the first expression in Eq. (10), which describes a tunneling mechanism. When the memristor switches to the *OFF* state, the $\omega(t)$ approaches zero, as the current is dominated by the second expression in Eq. (10), which indicates the junction barrier formation. This model assumes that there is a nonlinear dependence between the voltage and state variable $\omega(t)$. Equation (11) determines the speed of $\omega(t)$.

$$\mathrm{d}w/\mathrm{d}t = \alpha.f(\omega).v(t)^m, \tag{11}$$

where $f(\omega)$ is a window function, and m and α are constants.

2.2.6 Simmons tunnel barrier memristor model

Linear and nonlinear ion drift models are proposed for the physical memristor model based on two resistors connected in series. However, the Simmons tunnel barrier [41] represents a more accurate physical model of the memristor. Simmons introduced the concept of an electric tunnel between the insulator and electrode in 1963. The rectangular barrier is formed when both electrodes are of the same type. A trapezoid barrier is developed with different types of electrodes. In this model, an electron tunnel barrier is connected in series with a resistor. Equation (12) presents the analytical expression of the derivative of the state variable x. It is determined by iteratively applying a regression technique.

$$\frac{\mathrm{d}x(t)}{\mathrm{d}t} = \begin{cases} c_{\mathrm{off}} \sinh\left(\frac{i}{i_{\mathrm{off}}}\right) \exp\left[-\exp\left(\frac{x - a_{\mathrm{off}}}{w_c} - \frac{i}{b}\right) - \frac{x}{w_c}\right], & i > 0 \\ c_{\mathrm{on}} \sinh\left(\frac{i}{i_{\mathrm{on}}}\right) \exp\left[-\exp\left(\frac{x - a_{\mathrm{on}}}{w_c} - \frac{i}{b}\right) - \frac{x}{w_c}\right], & i < 0 \end{cases} \tag{12}$$

where c_{off}, c_{on}, i_{on}, i_{off}, w_c, and b are the fitting parameters, and a_{on} and a_{off} are the upper and lower limits of x, respectively. The change in the magnitude of x is controlled by the parameters c_{off} and c_{on}. The magnitude of c_{on} is greater than c_{off}. Once a particular threshold is achieved, the change in x is ignored.

2.2.7 Threshold adaptive memristor (TEAM) model

The TEAM model [42] was inspired by the Simmons tunnel barrier model. It uses the same physical model as presented by the Simmons tunnel barrier model but with simple mathematical expressions. The TEAM model depends upon the current threshold as given in Eq. (13). The derivative of the state variable x is dependent on both the current and x itself. The derivative of x for the TEAM model is defined in Eq. (13).

$$\frac{\mathrm{d}x(t)}{\mathrm{d}t} = \begin{cases} k_{\mathrm{off}}(\frac{i(t)}{i_{\mathrm{off}}} - 1)^{\alpha_{\mathrm{off}}} f_{\mathrm{off}}(x), & i > 0 \\ 0, & i_{\mathrm{off}} < i > i_{\mathrm{on}} \\ k_{\mathrm{off}}(\frac{i(t)}{i_{\mathrm{off}}} - 1)^{\alpha_{\mathrm{off}}} f_{\mathrm{off}}(x), & i < 0 \end{cases}, \tag{13}$$

where k_{off}, k_{on}, α_{on}, and α_{off} are the constants. The value of k_{off} is considered positive, whereas k_{on} is considered negative. The i_{off} and i_{on} are the current threshold values. The functions $f_{\mathrm{off}}(x)$ and $f_{\mathrm{on}}(x)$ behave as a window function, and x is a state variable that represents the effective electric tunnel width. The TEAM model has high complexity. In contrast to the other models, it freely allows any I–V relationship to be selected. Also, due to the high nonlinear dependence, the device can be modeled using the threshold currents. However, it depends on the current threshold, where the state of the memristor changes after a certain current threshold. Certain assumptions are considered in this model to enhance simplicity and computational efficiency. The value of the state variable x does not change after a certain current threshold. In the TEAM model, the memristor current is polynomial-dependent on the internal state drift derivative instead of exponential. The lower value of constants will enhance the complexity of the model.

These models have varying degrees of accuracy, with different phenomenological principles and features. The majority of models only consider particular aspects of memristive behavior, and hence these are incomplete models. HP presented a valuable concept of the memristor model based on the variable resistor, but it lacks the tunneling mechanism. Simmons's model described the concept of the electric tunnel between the insulator and the electrode. This model is close to the physical memristor; however, it skips the other barrier.

3 Phenomenological memristor model

In this section, a physical model is developed for the symmetric bipolar two-terminal memristor device. This model produces rich PHL behavior that is controlled by the nonlinearity of memristance. In this phenomenological model, the I–V relationship is based on the physical working mechanism of a memristor, whereas the internal state variable derivative can be independently chosen from any state variable derivative relationship. The state variable x=w/D is the normalized value, where w is the doped region as shown in Fig. 1. The total thickness of the device

in this model is considered as D. Whenever the voltage is applied across the terminals of the device, it forms a conductive filament across the entire device length, which is called R_{on}, and the rupture of the conductive filament is known as R_{off}. The proposed model correlates the physical working mechanism and the mathematics of a practical system using LDM with MIM interfaces as shown in Fig. 1. Two Schottky diodes are used to consider the MIM barriers. When the voltage is applied, the charges are trapped in the MIM interfaces. Kirchhoff's voltage law calculates the applied voltage across the memristor. V_1 and V_2 voltages are dropped due to the MIM interfaces, and its mathematical expression is given in Eq. 14.

$$V_t = V_1 + (R_{on}(x) + R_{off}(1-x))i(t) + V_2, \tag{14}$$

where V_t is the total applied voltage across the terminal of the device. The x is used to keep the device within its physical limits and to switch the states. The velocity of x is expressed in Eq. (15).

$$\frac{dx}{dt} = kW(x)I, \tag{15}$$

where k is a constant value and I is the current passing through the device. $W(x)$ is a window function. Strukov's window function [12] is used in this proposed model as expressed in Eq. (16).

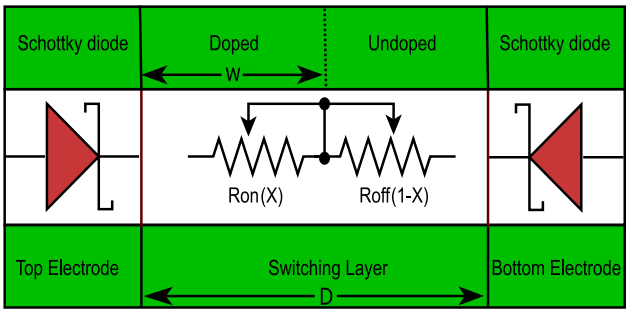

Fig. 1 Schematic illustration of MIM interfaces with a variable resistor in the proposed model

$$W(x) = x - x^2 \tag{16}$$

The ratio of voltage and current is called the memristance of the device. When negative voltage is applied, the memristance increases, and the device switches to the *OFF* state from the *ON* state. This process is known as the setting of the device, whereas the converse is referred to as resetting of the device. The model parameters are subdivided into three distinct categories, namely, input parameters, device parameters, and hyperparameters. For the simulation of phenomenological modeling, the values of the input parameters are the same as the input values provided to the experimental device. The values of device parameters are experimentally extracted from an in-house-fabricated device. Furthermore, the hyperparameters are tunable and are calibrated to acquire the optimal I–V curve value. HSPICE software is used to simulate the proposed model with the parameters given in Table 1.

3.1 Simulation of memristor model

The PHL behavior in the I–V plane of the proposed model is simulated using the abovementioned parameters in the HSPICE environment. A single memristor simulated response is evaluated by providing the sinusoidal waveform with amplitude of 1 V and frequency of 1 Hz as input. The well-known Lissajous figure of the memristor is observed in Fig. 2a. The bow-like curve indicates bipolar behavior because its switching state depends upon the amplitude of the threshold and the polarity of the applied voltage. The PHL characteristic of the simulated result indicates that the model has symmetric behavior in the I–V plane. The PHL of the model consists of two states (i.e., low-resistance state [LRS] and high resistance state [HRS]). The threshold voltages for switching the device between HRS and LRS are labeled V_{set} and V_{reset}, where V_{set} represents the voltage required to set the device into the LRS, while V_{reset} represents the voltage required to reset the device into the HRS. In this case, V_{set} is observed at 1 V, and V_{reset} is observed at $-1\ V$. The area within the PHL represents the amount of charge that is stored in the device and can be used to characterize its resistive behavior, which is called the memristance

Table 1 Simulation parameters of the proposed model

Parameter type	Parameter description	Symbol	Unit	Value
Input parameters	Input voltage	V	V	1
	Frequency	f	Hz	1
Device parameters	Width of the thin film	D	$\mu\ m$	16
	Average mobility	μ_v	$Femtom^2/(V.s)$	10
	Resistance at temperature	R_{ini}	Ω	2
Hyper parameters	Resistance in ON state	R_{on}	Ω	150
	Resistance in OFF state	R_{off}	Ω	5000

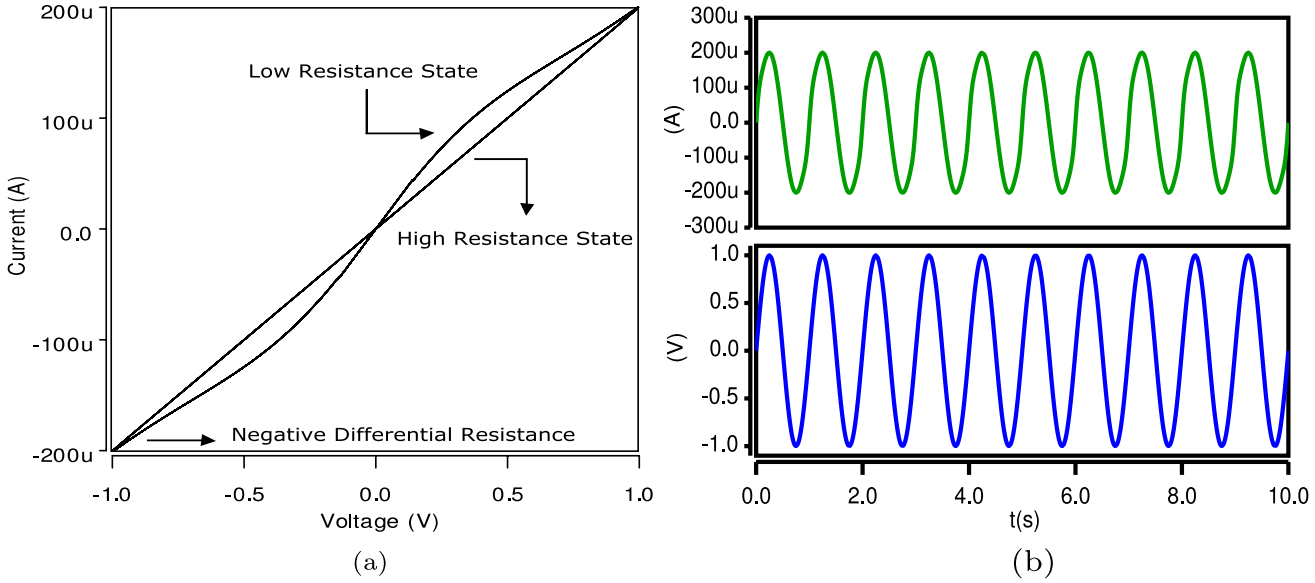

Fig. 2 **a** I–V characteristics of the proposed mathematical model of the memristor. **b** The proposed model presents the time-dependent relationship between the applied voltage and current

of the device. The loop determines the memory property of the memristor. This is a fundamental characteristic that distinguishes it from other basic electrical devices: resistor, capacitor, and inductor. The memristor exhibits the generation of the current that traces the loop on the hysteresis curve when an input voltage is applied. The size of the loop's area correlates directly with the amount of charge that the device can store or preserve. This stored charge significantly impacts the memristor's ability to maintain its resistance state, ultimately influencing its memory property. The larger loop area indicates greater capacity for charge storage and a more pronounced memory effect exhibited by the memristor. The transition of the device from the HRS to the LRS, or vice versa, is attributed to the occurrence of the negative differential resistance (NDR) phenomenon. This abrupt change in resistance characterizes the NDR effect. The NDR phenomenon is responsible for the switching behavior of the memristor. The NDR occurs at the switching voltage as shown in Fig. 2a. In the memristor, even the small voltage produced nonlinear behavior. The nonlinearity in the device occurs due to the nanoscale structure of the memristor, which allows even a small voltage bias to produce nonlinearity. This nonlinearity is attributed to either tunneling at the metal–semiconductor interface or electron hopping within the device. The nonlinear property of the proposed model is also observed in the simulated result as shown in Fig. 2. The value of the current varies between -200 and 200 μA. Furthermore, one of the key parameters for measuring the quality of the I–V response is dependent on the quick transition of the device state. The transition time was measured as the length of time taken by the memristor to switch between the LRS and HRS, and vice versa. Figure 2b indicates that the model switches its state quickly. The second most important parameter is power consumption, which is dependent on the value of the current. The lower value of current relative to the reported memristor models while keeping the voltage at the same level makes the proposed model more power-efficient. The average power consumption of the memristor model is calculated at 1 mW in its stable state. The HSPICE tool is the most commonly accepted and widely used tool, with no convergence issues. Along with its toolbox, it offers various applications and workflow. These advantages make the HSPICE a valuable tool for circuit design.

3.2 NOR logic gate

Memristors have important and intriguing applications in the design of logic gates for the processing of digital design applications. Logic operations with the help of a memristor will open a new path for novel functionality for computing applications. A NOR logic gate was simulated using the memristor ratio logic (MRL) family to validate the proposed memristor model [43]. Unlike other logic families, this logic family is compatible with CMOS technology. Two memristors are connected in series with the CMOS inverter to build the NOR gate logic. The simulation result for the NOR gate is given in Fig. 3. A value of 5 V is provided as the high input, whereas $0V$ is considered as the low voltage. Figure 3 presents a schematic of a NOR logic gate constructed by connecting two memristors in series with opposite polarity, forming an OR gate. The output is obtained from the common node of the memristors'

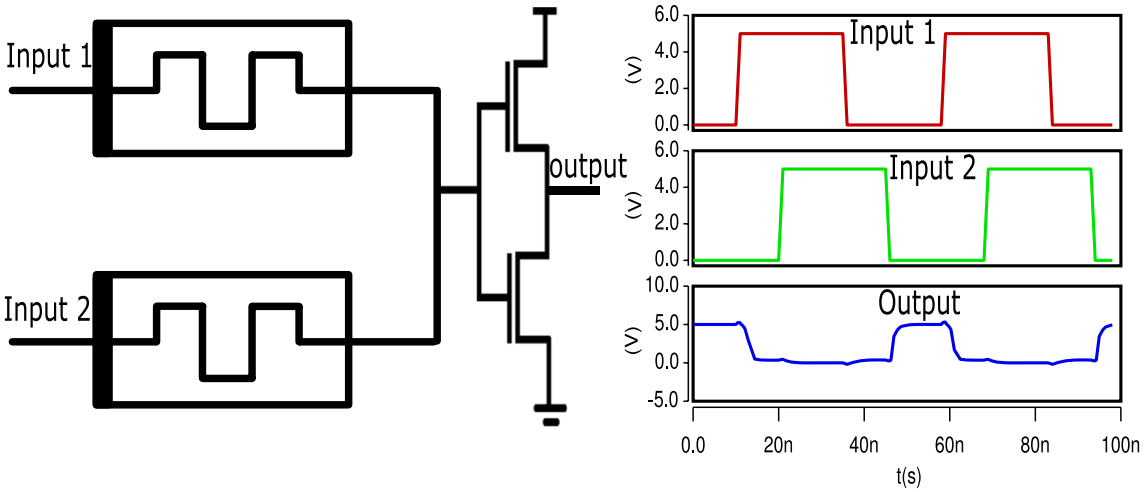

Fig. 3 Simulation result for NOR logic gate using the proposed memristor model

terminals, while the input signals are fed to the other terminals. The memristance of the memristor depends on the direction of the current flow. Its value increases when the current flows from the negative to the positive terminal of the memristor and decreases when the current flows from the positive to the negative terminal of the device. If both inputs have the same logical value, no current flows, and the same logic is observed at the output terminal. The flow of current from a higher potential to a lower potential is observed in an OR gate when one input is logical 0 and the other input is logical 1. As a result, the output of the OR gate becomes logical 0. To complete the NOR gate circuit, a CMOS inverter is connected at the end output terminal of the OR gate. In Fig. 3, 5 V and 0 V are considered as logical 1 and logical 0 inputs, respectively. The output of the NOR gate is logical 0 if any of the inputs is at logical 1, as demonstrated in Fig. 3.

4 Novel memristor fabrication

The chemicals used for the deposition of the insulating layer using the screen printing method for the fabrication of the novel memristor are given below:

1. Bead polymer based on methyl methacrylate and *n*-butyl methacrylate
2. Xylene (dimethylbenzene)

The properties of the switching layer material are given in Table 2.

Table 2 Technical properties of the insulating layer

Property	Value	Unit
Glass transition temperature (Tg)	43	°C
Viscosity number	50–60	cm^3/g
Molecular weight (MW)	150,000	g/mol
Dynamic viscosity	450	mPas
Density	1.08	g/cm^3
Purity	>99.5	%
Bulk density	650	g/L

4.1 Experimental procedure

An equimolar concentration of bead polymer based on methyl methacrylate and *n*-butyl methacrylate and dimethyl benzene solution is prepared. The solution is stirred for 10 min to obtain maximum precipitate. Cu is used as the substrate to deposit the insulating layer of acrylic polymer. Before the deposition process, the substrate is washed with deionized water in a water bath. Then it is rinsed with acetone and ethanol. Ultraviolet (UV) treatment is also provided for 10 min. It is used as the bottom electrode for the in-house-fabricated device. The abovementioned solution is used to deposit the insulating layer. A semiautomatic screen printing machine is used to deposit the active layer of the electric switch. The screen used for the insulating layer deposition has 200 threads per square inch. After the deposition of the switching layer using the screen printing technique, the sample is cured at 105 $^{\circ}C$ for 90 min. Highly conductive Ag is deposited on the sample by drop-casting in a circular shape. Ag is used to make the top electrode to complete the simple structure of the resistive switching device. Finally, the samples are treated with heat at 105 $^{\circ}C$ for 90 min. The

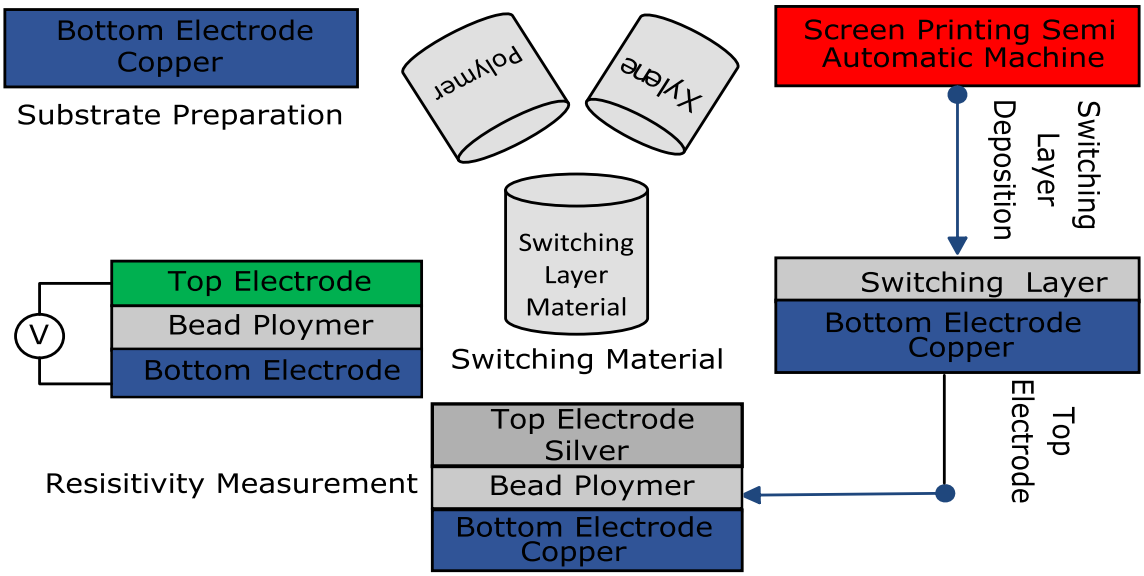

Fig. 4 Experimental setup of the fabricated device

experimental setup of the proposed device is given in Fig. 4. The experiment is performed at standard room temperature and pressure.

4.2 Characterization of memristor fabrication

4.2.1 Structural analysis of switching layer of fabricated device

The surface morphology of the samples is observed with the help of scanning electron microscopy (SEM) images (TESCAN Vega LMU). The thin film of the resistive switching layer is characterized at different zoom levels, as illustrated in Fig. 5a. It is evident that the switching layer is very smooth and has a uniform surface of the thin film used to fabricate the device. The top view of highly magnified images shows that the polymeric layer is successfully deposited densely on the flexible copper substrate as depicted in Fig. 5. To avoid the charging effect, samples are sputtered with gold. Figure 5b is taken from the energy-dispersive x-ray (EDX) analysis. It is used to provide elemental identification and quantitative compositional information. EDX analysis indicates that there are no significant impurities in

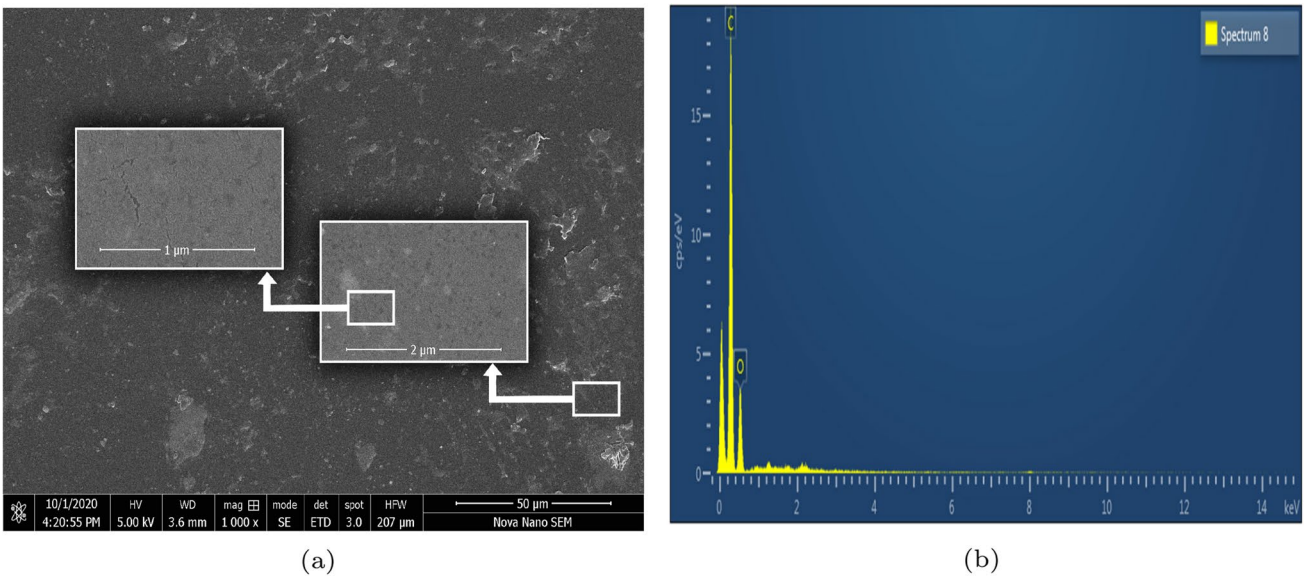

Fig. 5 Surface morphology of a switching layer of the fabricated device. **a** Surface morphology of a switching layer of the fabricated device at 1 μm, 2 μm, and 50 μm. **b** Energy-dispersive x-ray analysis of the bead polymer for the switching layer

the polymer thin film layer. From Fig. 5 it can be concluded that the screen printing technique has good potential for the deposition of thin film layers.

4.2.2 I–V characterization of novel memristor

Electrical measurement is performed by the Metrohm Autolab (PGSTAT 12) utilizing the general purpose electrochemical system (GPES) manager software. The top Ag electrode is connected with the driving force, and the bottom Cu electrode is constantly grounded in all I–V measurements to analyze the electrical characteristics of the in-house-fabricated device. Double voltage sweeps are applied to analyze the switching properties of the MIM structure. The current compliance (CC) is fixed at 10 mA. Figure 6a displays the I–V characteristics of the in-house-fabricated device, which have symmetric properties passing through the origin with two distinct slopes. The steep slope indicates the LRS, which is called R_{on}. The shallow slope determines the HRS, which is known as R_{off}. The magnitude of measured current varies between -0.08 *A* and 0.08 A. The fabricated device switches its state at 0.75 V, indicating bipolar switching behavior. The device shows resistive switching behavior when the external force is applied at its electrode. The transition of the device from the LRS to HRS is referred to as the setting of the device, while the reverse transition from HRS to LRS is referred to as the resetting of the device. The steep slope observed in the LRS of the memristor depends on several factors. It may be due to the existence of a higher concentration of conductive filaments within the switching material during the LRS. These highly conductive pathways facilitate the flow of charges, and result in lower resistance of the device. On the other hand, the shallow slope observed in the HRS may be due to a destruction of conductive filaments within the switching layer material. This configuration restricts the flow of charges, leading to higher resistance, and a shallower slope is observed. Different CC is provided to the device to check its behavior for a dynamic range of analysis. The CC is provided to save the device from permanent damage. In Fig. 6, before positive and negative threshold voltage approaches, the device shows constant current due to CC of 100 mA. When the voltage is swept between 1 V and -1 *V* with CC of 100 mA, the fabricated device shows the rich PHL. The behavior of the MIM structure looks similar to the previous one; however, the threshold voltage seems to be observed a bit earlier. Due to CC, the magnitude of the current is decreased. The CC is settled to 1 mA to observe the I–V characteristics, where it is observed that the PHL disappears as shown in Fig. 6b. The PHL of the fabricated device disappears due to a very small value of CC.

The CC limits the current to a specific value, aiming to protect the device from a permeant hard breakdown. Therefore, when the CC decreases, the maximum current flowing through the device decreases, and vice versa. However, for the observation of the PHL, it is necessary for the CC value to be greater than the value of the current in the LRS. Otherwise, the CC restricts the current to a value smaller than that of the LRS. As a consequence, the PHL diminishes, and the electrical switching state cannot be observed. When the double voltage sweep is provided, the resultant PHL looks similar to Fig. 6b. When the fabricated device kisses the voltage greater than 0, the current becomes constant at

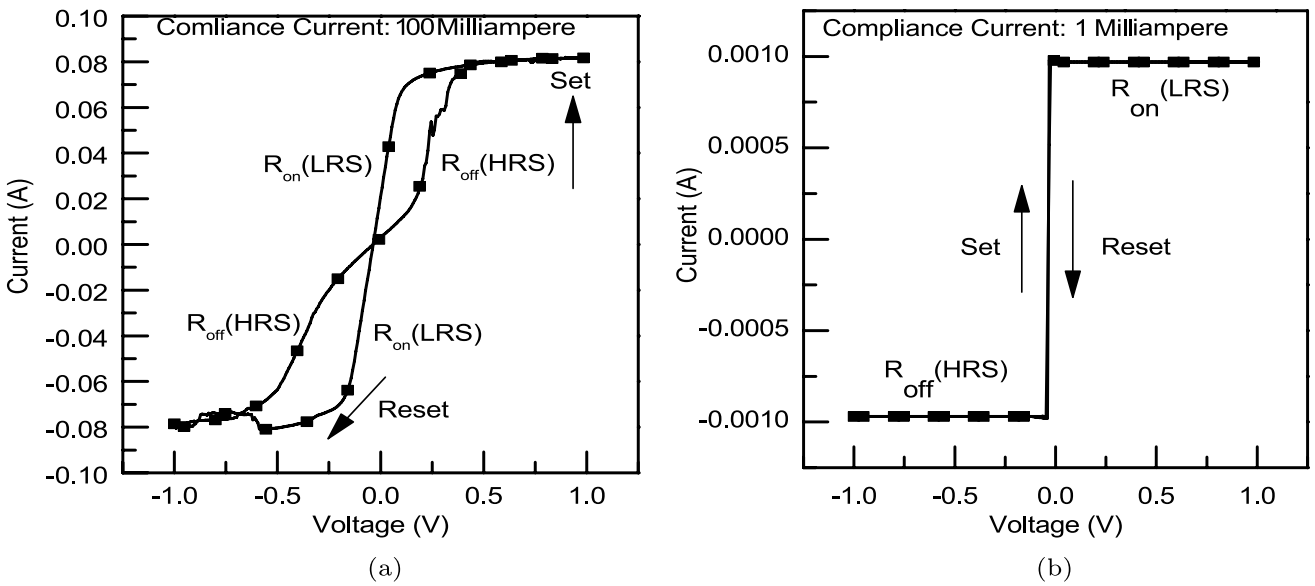

Fig. 6 I–V characterization of the in-house-fabricated bipolar memristor. **a** I–V characterization of the fabricated device at 100 *mA*. **b** I–V characterization of the fabricated device at 1 *mA*

any applied voltage. It can be observed from Fig. 6a and b that the PHL shrinks and disappears when the value of CC decreases. The accuracy of the proposed model in the noise condition is calculated using the relative root mean square (RMS) error formula. The relative RMS is determined by Eq. (17).

$$e_{i,v} = \sqrt{\frac{1}{N}\left(\frac{\sum_{i=1}^{N}\left(V_{pro,i} - V_{ref,i}\right)^2}{\bar{V}_{\text{ref}}^2} + \frac{\sum_{i=1}^{N}\left(I_{pro,i} - I_{ref,i}\right)^2}{\bar{I}_{\text{ref}}^2}\right)}, \tag{17}$$

where V_{pro}, i and I_{pro}, i are respectively the corresponding $i-th$ sample of the voltage and current of the proposed model, and N is the number of samples, where the value of N is 250. V_{ref}, i and I_{ref}, i are respectively the corresponding $i-th$ samples of the voltage and current of the in-house-fabricated device. The RMS error is used to evaluate the accuracy of a model's output. It determines how well the model represents the experimental device. A lower RMS error indicates a better fit between the model and the practical device. Using MATLAB 2019, the RMS error of the proposed model with the data points of the in-house-fabricated device is 0.7609. The error between the I–V characteristic of the in-house-fabricated device and the proposed model is due to experimental setup noise and material impurities.

4.3 Schottky conduction

The complex I–V graph is further investigated to reveal the hidden mystery behind the Schottky conduction. As shown in Fig. 7, the LRS and HRS are governed by Schottky conduction because the I–V relationship has a linear fitting curve. The J–V relationship is described by Eq. (18).

$$J = A * T^2\{\exp[\frac{-q(\varphi_B - \beta(E)^{\frac{1}{2}})}{kT}], \tag{18}$$

where q is the electronic charge, J is current density, $A*$ is the Richardson constant, φ_B is barrier height, T is absolute temperature, K is the Boltzmann constant, E is the electric field, and β is the Schottky coefficient. Figure 7 shows the curve between the $ln(J)$ and the $E^{\frac{1}{2}}$. Figure 7a and b depict the Schottky behavior in LRS and HRS during the negative polarity. Figure 7c and d illustrate the Schottky barriers in LRS and HRS during positive polarity. Both sides of voltage polarity exhibit Schottky behavior. The results of the analytical study validate the information for the junction barrier in the device.

4.4 Comparison

Table 3 depicts the superior performance of the proposed model in comparative analysis with other models. Some interesting facts about the memristor models can be observed. The analysis is conducted taking into account five parameters including boundary effect, nonlinear drift, complexity, junction barrier, and accuracy. The boundary effect dilemma and nonlinear drift phenomenon are resolved by all the models except LDM. The complexity challenges remain unsolved by all the competitors except LDM and the proposed model. Some models totally ignore the junction barrier parameter and others only partially address it, but the proposed model considers both junction barriers. A comparison of the accuracy of the different models in terms of the metal–insulator interfaces is also considered. The LDM [12] and nonlinear ion drift model [40] do not consider the junction barrier formed due to the metal–insulator interface. The Simmons tunnel barrier [41] considers the tunnel at one interface and ignores the barrier at the other end. Similarly, the TEAM model [42] is inspired by the same physical mechanism proposed by the Simmons model. The proposed model has solved the boundary effect, nonlinear drift, and junction barrier. The code is run 10 times to calculate the unbiased simulation runtime. The average computational runtime is compared for the different models and presented in Table 3. The proposed model shows an improvement in simulation runtime of up to 2.76% and exhibits enhanced accuracy as illustrated by the RMS error value, achieving a noteworthy improvement of 4.71% over the previous model. Moreover, the proposed model exhibits high accuracy with lower complexity than the competitors. The proposed model satisfies all requirements of the memristor model given in Table 3.

Different materials and techniques have been reported in the literature for the fabrication of the memristor. However, none of the techniques is cost-effective, fast, and simple. Screen printing is one of the best techniques for the rapid and mass production of devices. The Ag/MMBM/Cu-based structure is analytically demonstrated for the first time for the fingerprint of resistive switching behavior. The cost-effective novel structure and technique have opened the path for memristor fabrication. The comparison of different structures and fabrication techniques is tabularized in Table 4. Although much work has been carried out on modeling, fabrication, and memristor-based applications, there is still ample room for improving the accuracy, stability, and complexity of the memristor model in a more simple, intuitive, and closed form. Moreover, other physical structures must be implemented in order to create sufficient space to improve the robustness, stability, and cyclic endurance of the fabricated device.

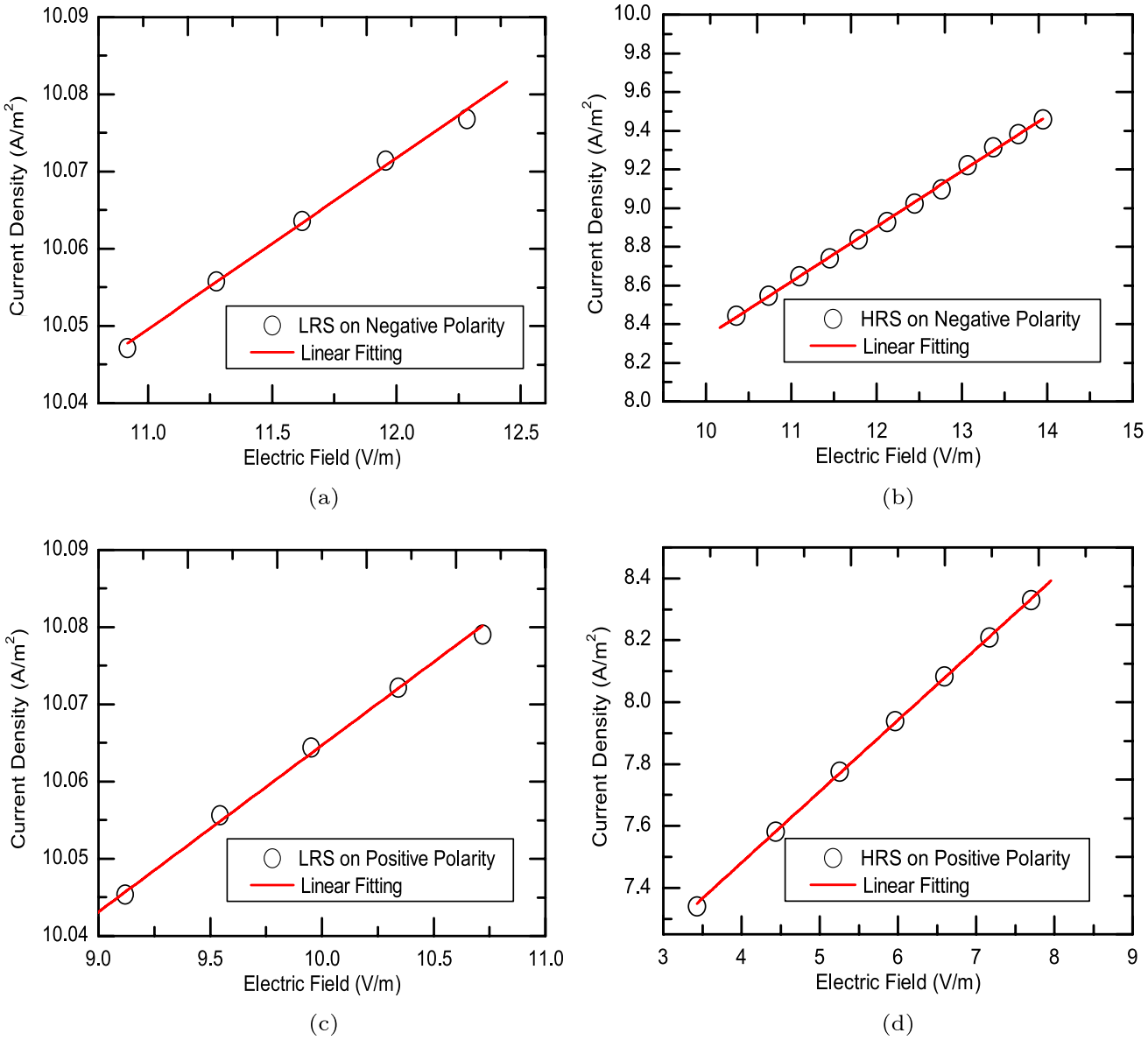

Fig. 7 I–V graph in double logarithmic scales. **a** $ln(J)$ against $E^{\frac{1}{2}}$ shows the Schottky contact in LRS during negative polarity. **b** $ln(J)$ against $E^{\frac{1}{2}}$ shows the Schottky contact in LRS during positive polarity. **c** $ln(J)$ against $E^{\frac{1}{2}}$ shows the Schottky contact in LRS during positive polarity. **d** $ln(J)$ against $E^{\frac{1}{2}}$ shows the Schottky contact in HRS during negative polarity

Table 3 Comparison of different memristor models with the proposed model

Memristor model → Parameters ↓	LDM [12]	Nonlinear [40]	Simmons [41]	TEAM [42]	Proposed
Resolves boundary effect	No	Yes	Yes	Yes	Yes
Imposes nonlinear drift	No	Yes	Yes	Yes	Yes
Simulation runtime (S)	1.45	1.56	1.74	1.69	1.41
Complexity	Low	Average	Very high	High	Low
RMS error	0.8376	0.8125	0.7956	0.7985	0.7609
Junction barrier	No	No	Limited	Limited	Yes
Accuracy	Very low	Low	Moderate	Moderate	High

Table 4 Comparison of different layer deposition techniques for fabrication of memristor device

Sr. No.	Materials	TE/BE	$V_{set}\backslash V_{reset}$	Memory window	Fabrication process	Capital cost	Production time
1	ZnO [44]	Ag/Cu	1.2 V/−1.25 V	High	Electrohydrodynamic printing	Average	High
2	TiO_2 [45]	Pt/Pt	1 V/−1 V	High	ALD	High	High
3	NiO [45]	Pt/Pt	10 V/−10 V	Average	Pulsed laser deposition	High	High
4	HfO_2 [46]	TiN/TiN	1.5 V/−1.4 V	Low	ALD	High	High
5	ZrO_2 [32]	ITO/Ag	1 V/−1 V	Low	Electrohydrodynamic printing	Average	High
6	Al_2O_3 [47]	Ti/Pt	1.4 V/−1.7 V	Average	RF-magnetron sputtering	High	High
7	MnO [48]	Ti/Pt	0.7 V/−1.1 V	High	RF-reactive sputtering	High	High
8	ZnO_{1-x}/ZnO [49]	Pt/Pt	1.5 V/−0.6 V	Low	Sol–gel	Average	High
9	Cu doped SiO2 [50]	Cu/W	0.9 V/−0.75 V	Low	E-beam evaporation	High	High
10	Polymer	Ag/Cu	1V/−1V	Low	Screen printing	Very low	Very low

5 Conclusion

This paper describes the modeling and experimental demonstration of a memristor device. Digital design applications based on memristors require the most accurate physical model of the device for the analysis and study of the circuit simulation. The proposed model shows the effect of the most noticeable physical phenomenon of Schottky barriers in polymeric memristive devices. The simulated results have previously been observed experimentally with the use of expensive materials and sophisticated techniques. In this work, a cost-effective and rapid screen printing fabrication technique is first demonstrated for the fabrication of memristor devices, and the rich pinch hysteresis electrical measurement is observed in the Ag/MMBM/Cu-based novel structure. Based on the experimental results, the polymeric memristor shows Schottky behavior at both interfaces. Compared with existing models, the primary significance of the proposed model is its consideration of the meta-to-semiconductor interface impact. The proposed model and fabricated device show a close relationship between simulated and experimental results. The accurate modeling approach and simple fabrication technique of the memristor will open new horizons in digital design computing applications.

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Declarations

Competing interests The authors have not disclosed any competing interests.

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