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Polycrystalline silicon nanowire FET performance depending on density of states

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Abstract
Herein, we investigate the performance of thin film transistors based on polycrystalline silicon nanowires using the complementary metal–oxide–semiconductor spacer technique. A drain current model was developed based on the Poisson equation whose charge density includes the acceptor traps. The density of states (DOS) distribution was characterized by two exponentials modeling the tail and the deep states within the gap. A comprehensive analysis was conducted on the impact of the DOS parameters on the transfer characteristics. The results show that the deep states affect the current behavior in the subthreshold region, while the tail states affect the current above the threshold. For comparison, the model was fitted with the experimental data. The deep state density was high, which provides qualitative insight into the structure of polycrystalline silicon nanowires (poly-SiNWs). The results are in good agreement with the study of the conduction mechanism and the measurement of DOS for these nanowires.

Keywords Polysilicon nanowires · Modeling · Density of states

1 Introduction

Polycrystalline silicon nanowires (poly-SiNWs) have attracted considerable attention in recent decades as an active element for the new generation of electronic devices, such as thin film transistors (TFT) [1–3] and biochemical sensors [4, 5], owing to their sensitivity to chemical and biological species. The electrical properties of poly-SiNWs and their realization technique have rendered these nanowires potentially promising candidates for overcoming several obstacles, such as the short-channel effects encountered in fin field-effect transistors (FinFETs) [6]. Different techniques have been implemented to realize poly-SiNWs [7, 8], and the top-down approach affords an important advantage due to its compatibility with the concept of miniaturization. Planar technology is commonly used in the very large-scale industrial applications to produce reliable and low-cost devices. More precisely, for low-temperature technologies, polycrystalline silicon is a widely used material.

Although the operation of devices based on poly-SiNWs has been demonstrated [1, 9, 10] and their performance has been encouraging, they are still being researched to better understand and identify the properties of poly-SiNWs for integration in commercial devices. Furthermore, the electrical properties of poly-SiNWs are closely linked to their production processes, their diameter [11], and their architecture. More precisely, their crystalline quality plays a decisive role in the device performance. Thus, poly-SiNWs with good crystalline quality will afford high-performance devices such as transistors with a high I_{ON}/I_{OFF} ratio, reduced threshold voltage, and small subthreshold swing slope [12]. In contrast, a low or even highly disordered crystalline quality is advantageous for sensors owing to the interaction of the electrical defects on the surface with the surrounding chemical species [13].

The performance/crystalline quality duality of poly-SiNWs needs to be analyzed to understand and predict their behaviors. Since physical characterizations are a powerful tool for understanding the device properties, analytical and numerical studies have been performed to build models to explicitly determine the electrical properties. Several approaches have been employed to model the electrical performance of poly-SiNW-based devices with different architectures, including back gate, dual gate [14], and gate all around [15,

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16], by analyzing the impact of the number and position of grain boundaries present in the nanowire structure. For poly-SiNWs with a high density of defects, adopting a model that is described by only grain boundaries is not convenient. Indeed, studies on the conduction mechanism [17] for poly-SiNWs with diameters less than 50 nm have shown that carrier transport occurs via variable-range hopping (VRH). This verifies the disordered nature for poly-SiNWs and rules out the model based on grains separated by grain boundaries.

In this study, we investigate the performance of TFTs based on poly-SiNWs with 30 nm diameters that were realized using the complementary metal–oxide–semiconductor (CMOS) spacer technique [7]. First, a model of the drain current was developed based on the Poisson's equation. The charge of acceptor traps to the density of states (DOS) was represented by two exponentials describing the deep and band tail states. Thereafter, the impact of the DOS parameters is detailed and discussed to elucidate the performance of poly-SiNWs. Finally, the model was fitted with the experimental transfer characteristic data, justified in agreement with our study on the conduction mechanism and DOS measurements for TFTs based on poly-SiNWs in order to provide the DOS within the gap.

2 Device modeling

2.1 Surface potential model

Our previous study [17] on the electrical properties of poly-SiNWs obtained using the spacer method revealed that the conduction mechanism operates via VRH when the nanowire diameter is around 50 nm. This is explained by the high density of electric traps that are afforded by the disordered structure of the lower part of the un-doped poly-Si layer, from which these nanowires are obtained. Therefore, we can consider the DOS model [18] to express the distribution of these defects within the gap. The density of two exponential acceptor and donor tail states and two exponential deep acceptor and donor states can be expressed as follows:

$$g_{\mathrm{TA}}(E) = N_{\mathrm{TA}} \exp\left(\frac{E-E_C}{w_{\mathrm{TA}}}\right) \tag{1}$$

$$g_{\mathrm{DA}}(E) = N_{\mathrm{DA}} \exp\left(\frac{E-E_C}{w_{\mathrm{DA}}}\right) \tag{2}$$

$$g_{TD}(E) = N_{TD} \exp\left(\frac{E_V-E}{w_{TD}}\right) \tag{3}$$

$$g_{\mathrm{DD}}(E) = N_{\mathrm{DD}} \exp\left(\frac{E_V-E}{w_{\mathrm{DD}}}\right) \tag{4}$$

Here, g_{TA}(E) and g_{TD}(E) are two exponential densities that correspond to the densities of the acceptor and donor states, respectively, in the tape tails. Additionally, g_{DA}(E) and g_{DD}(E) are two exponential densities corresponding to the densities of the deep acceptor and donor states, respectively. E is the trap energy, E_C is the conduction band energy, and $\mathrm{E_V}$ is the valence band energy. For tail distributions, DOS is described by the conduction and valence band edge intercept densities (N_{TA} and $\mathrm{N_{TD}}$, respectively) and the characteristic decay energies (W_{TA} and W_{TD}, respectively). For deep distributions, DOS is described by the conduction and valence band edge intercept densities (N_{DA} and N_{DD}, respectively) and the characteristic decay energies (W_{DA} and W_{DD}, respectively).

Figure 1 shows the cross-section of the metal–insulator–semiconductor structure and the corresponding energy diagram. For simplicity, we only consider the free electrons and the charge of the acceptor traps. The one-dimensional Poisson equation is

$$\frac{\partial^2\psi}{\partial x^2} = \frac{q}{\epsilon_{si}}\left(n + n_T\right) \tag{5}$$

Here, n is the concentration of free electrons and $\mathrm{n_T}$ is the density of ionized acceptor traps:

$$n = N_0 \exp\left(\frac{q\psi}{\mathrm{kT}}\right) \tag{6}$$

$$n_T = n_{\mathrm{tail}} + n_{\mathrm{deep}} = \int_{E_V}^{E_C} g_{\mathrm{TA}}(E).f_A(E).\mathrm{d}E + \int_{E_V}^{E_C} g_{\mathrm{DA}}(E).f_A(E).\mathrm{d}E \tag{7}$$

where $N_0 = N_C \exp\left(-\frac{E_{F0}}{\mathrm{kT}}\right)$ is the electron concentration under equilibrium conditions, and N_C is the effective DOS in the conduction band. f_A(E) is the probability function of occupation of an acceptor trap by an electron:

$$f_A(E) = \frac{1}{1+\exp\left(\frac{E-E_{F0}}{\mathrm{kT}}\right)} = \begin{cases} 1; E < E_{F0} \\ \exp\left(\frac{E_{F0}-E}{\mathrm{kT}}\right); E > E_{F0} \end{cases} \tag{8}$$

Here, $\mathrm{E_{F0}}$ denotes the Fermi level under equilibrium conditions. Based on the band gap diagram, the number of ionized acceptor traps at steady state is

$$n_{\mathrm{tail}}(\psi) = \int_{E_V}^{E_{F0}+q\psi} g_{TA}(E).\mathrm{d}E + \int_{E_{F0}+q\psi}^{E_C} g_{\mathrm{TA}}(E).\exp\left(\frac{E_{F0}-E}{\mathrm{kT}}\right)\mathrm{d}E \tag{9}$$

$$n_{\mathrm{tail}}(\psi) = \alpha_T\left[A_T \exp\left(\frac{q\psi}{\mathrm{kT}}\right) - B_T \exp\left(\frac{q\psi}{W_{\mathrm{TA}}}\right)\right] - C_T \tag{10}$$

$$n_{\mathrm{deep}}(\psi) = \int_{E_V}^{E_{F0}+q\psi} g_{DA}(E).\mathrm{d}E + \int_{E_{F0}+q\psi}^{E_C} g_{\mathrm{DA}}(E).\exp\left(\frac{E_{F0}-E}{\mathrm{kT}}\right)\mathrm{d}E \tag{11}$$

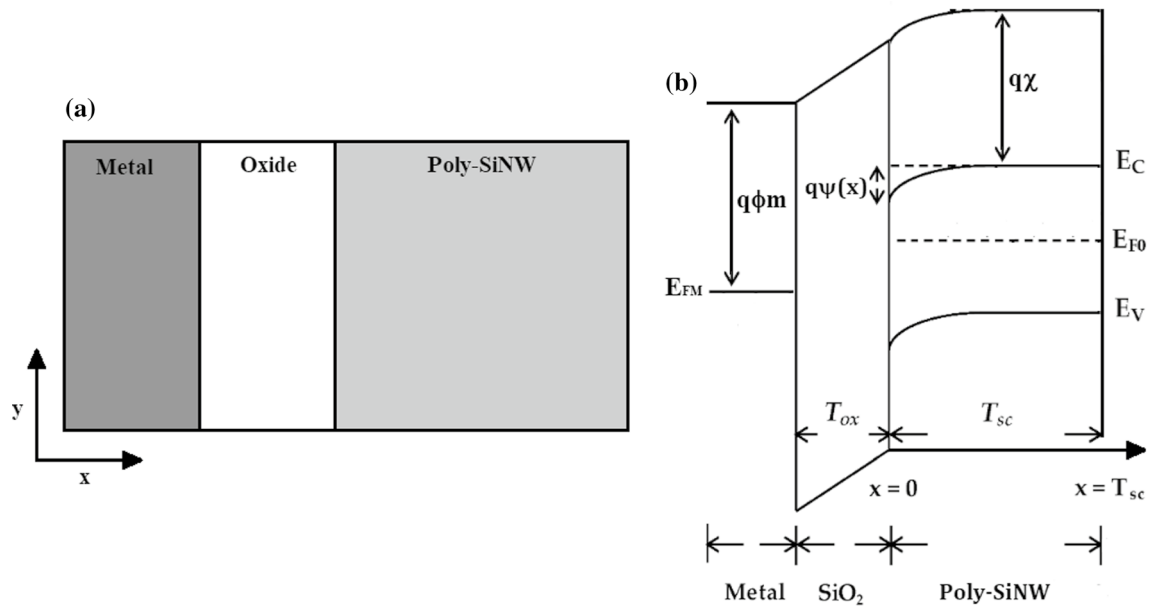

Fig. 1 **a** Schematic of the considered metal–insulator–semiconductor structure. **b** Energy band diagram

$$n_{\text{deep}}(\psi) = \alpha_D\left[A_D \exp\left(\frac{q\psi}{\text{kT}}\right) - B_D \exp\left(\frac{q\psi}{W_{\text{TA}}}\right)\right] - C_D \quad (12)$$

Here,

$$\alpha_T = \frac{W_{\text{TA}}N_{\text{TA}}}{\text{kT} - W_{\text{TA}}}; \alpha_D = \frac{W_{\text{DA}}N_{\text{DA}}}{\text{kT} - W_{\text{DA}}}; A_T = A_D = \text{kT}\exp\left(\frac{E_{F0} - E_C}{\text{kT}}\right); B_T = W_{\text{TA}}\exp\left(\frac{E_{F0} - E_C}{W_{\text{TA}}}\right)$$
$$; B_D = W_{\text{DA}}\exp\left(\frac{E_{F0} - E_C}{W_{\text{DA}}}\right); C_T = W_{\text{TA}}N_{\text{TA}}\exp\left(-\frac{E_C}{\text{kT}}\right); C_D = W_{\text{DA}}N_{\text{DA}}\exp\left(-\frac{E_C}{\text{kT}}\right)$$

Using the property $\partial(\partial\psi/\partial x)^2 = 2\left(\partial^2\psi/\partial x^2\right)\partial\psi$, the electric field ξ along x is expressed according to (5) as

$$\partial\left(\xi^2\right) = \frac{2q}{\varepsilon_{si}}\left(n + n_T\right)\partial\psi \quad (13)$$

Substituting (6), (10), and (12) in (13) and integrating from $\psi_{Tsc}(x = T_{sc})$ to $\psi_s(x = 0)$, the expression of the electric field at the SiO_2/poly-SiNW interface ($x = 0$) is

$$\xi_s = \sqrt{\frac{2kT}{\varepsilon_{\text{si}}}\left|\left(N_1 + N_2 + N_3 + N_4\right)\right|} \quad (14)$$

Here,

$$N_1 = \left(N_0 + \alpha_T A_T + \alpha_D A_D\right)\left(\exp\left(\frac{q\psi_s}{\text{kT}}\right) - \exp\left(\frac{q\psi_{\text{Tsc}}}{\text{kT}}\right)\right)$$

$$N_2 = -\frac{W_{\text{TA}}}{kT}\alpha_T B_T\left(\exp\left(\frac{q\psi_s}{W_{\text{TA}}}\right) - \exp\left(\frac{q\psi_{\text{Tsc}}}{W_{\text{TA}}}\right)\right)$$

$$N_3 = -\frac{W_{DA}}{\text{kT}}\alpha_D B_D\left(\exp\left(\frac{q\psi_s}{W_{\text{DA}}}\right) - \exp\left(\frac{q\psi_{\text{Tsc}}}{W_{\text{DA}}}\right)\right)$$

$$N_4 = -\left(C_T + C_D\right)\left(\frac{q\psi_s}{\text{kT}} - \frac{q\psi_{\text{Tsc}}}{\text{kT}}\right)$$

For a range of parameters W_{TA}, W_{DA}, N_{TA}, and N_{DA}, which we will discuss later, only the terms N_2 and N_3 subsist in the expression of ξ_s. Neglecting the potential ψ_{Tsc}, the final expression of ξ_s becomes

$$\xi_s \approx \sqrt{\frac{2\text{kT}}{\varepsilon_{si}}\left(N_{02}\exp\left(\frac{q\psi_s}{W_{\text{TA}}}\right) + N_{03}\exp\left(\frac{q\psi_s}{W_{\text{DA}}}\right)\right)} \quad (15)$$

Here,

$$N_{02} = -\frac{W_{\text{TA}}}{\text{kT}}\alpha_T B_T; N_{03} = -\frac{W_{DA}}{\text{kT}}\alpha_D B_D$$

Considering the V_{ox} potential in the insulator and using Gauss's law at the SiO_2/poly-SiNW interface, the gate voltage is

$$V_{\text{GS}} = V_{\text{ox}} + \psi_s + V_{\text{FB}} = \psi_s + V_{\text{FB}} + t_{\text{ox}}\frac{\varepsilon_{\text{si}}}{\varepsilon_{\text{ox}}}\xi_s \quad (16)$$

where V_{FB} is the flat band voltage defined by $V_{FB} = q\chi - q\varphi_m$. Thus, ψ_s becomes

$$\psi_s = V_{GS} - V_{FB} - \frac{\sqrt{2kT\varepsilon_{si}}}{C_{ox}}\sqrt{N_{02}\exp\left(\frac{q\psi_s}{W_{TA}}\right) + N_{03}\exp\left(\frac{q\psi_s}{W_{DA}}\right)} \quad (17)$$

Here, C_{ox} is the oxide capacity per unit area. An analytical expression of ψ_s cannot be clearly obtained from (17). However, depending on the choice of the parameters N_2 and N_3, one of the two parameters dominates the expression of ξs. Then, ψ_s becomes

$$\psi_s = V_{GS} - V_{FB} - \frac{\sqrt{\varepsilon_{si}2kT}}{C_{ox}}\sqrt{N_{02,3}}\exp\left(\frac{q\psi_s}{2W_{T,DA}}\right) \quad (18)$$

Here,

$$N_{02,3}\exp\left(\frac{q\psi_s}{W_{T,DA}}\right) = N_{02}\exp\left(\frac{q\psi_s}{W_{TA}}\right) or N_{03}\exp\left(\frac{q\psi_s}{W_{DA}}\right) \quad (19)$$

From (18), the numerical solution ψ_s for a given V_{GS} value shows that the potential $\psi_s << V_{GS}$ when $V_{GS} > V_{FB}$, yielding the following final expression of ψs

$$q\psi_s = 2W_{T,DA}.\ln\left(\frac{V_{GS}-V_{FB}}{\frac{\sqrt{\varepsilon_{si}2kT}}{C_{ox}}\sqrt{N_{02,3}}}\right) \quad (20)$$

2.2 Drain current model

The free electron concentration, according to the charge sheet model, over the entire depth of the nanowire is as follows:

$$n_{free} = \int_0^{T_{sc}} n(x).dx = \int_0^{T_{sc}} \frac{n(x)}{d\psi}d\psi dx = \int_{\psi_s}^{0} \frac{n(x)}{\xi(x)}d\psi \quad (21)$$

$$n_{free} = \frac{N_0}{\sqrt{\frac{2kT}{\varepsilon_{si}}N_{02,3}}}\frac{2W_{T,DA}.kT}{2W_{T,DA}-kT}\left(\frac{V_{GS}-V_{FB}}{\frac{\sqrt{\varepsilon_{si}2kT}}{C_{ox}}\sqrt{N_{02,3}}}\right)^{\frac{2W_{T,DA}}{kT}-1} \quad (22)$$

According to the MOSFET drain current [22], its expression is

$$I_{DS} = \frac{W}{L}q\mu_0 n_{free}\int_{V_S}^{V_D} d\psi(z) \quad (23)$$

where W and L are the width and length of the channel, respectively, μ_0 is the mobility of electrons, and $\psi(z)$ is the potential along the channel. The drain current is

$$I_{DS} = \frac{W}{Z}\frac{q\mu_0 N_0}{\sqrt{\frac{2kT}{\varepsilon_{si}}N_{02,3}}}\frac{2W_{T,DA}.kT}{2W_{T,DA}-kT}\left(\frac{V_{GS}-V_{FB}}{\frac{\sqrt{\varepsilon_{si}2kT}}{C_{ox}}\sqrt{N_{02,3}}}\right)^{\frac{2W_{T,DA}}{kT}-1}V_{DS} \quad (24)$$

The subthreshold slope is

$$SS = \frac{\ln(10)}{\frac{\partial \ln(I_{DS})}{\partial V_{GS}}} = \ln(10).\frac{V_{GS}-V_{FB}}{\frac{2W_{T,DA}}{kT}-1} \quad (25)$$

3 Results and discussion

To validate our model, a technology computer-aided design (TCAD) simulation was performed using Silvaco commercial software [19]. Figure 2 displays a three-dimensional (3D) view of the simulated device, and Table 1 summarizes the DOS parameters and the chosen dimensions, similar to the experimental device reported in Ref. [20]. Herein, we focus on the effect of DOS parameters (N_{TA}, W_{TA}, N_{DA}, W_{DA}) on the transfer characteristics. Thus, only one parameter is varied while the others are kept fixed. For reference, $I_{DS}(V_{GS})$ curves include transfer characteristics fitted with experimental data from Ref. [20].

Figure 3 displays the transfer characteristics of the model in comparison to the simulation with N_{TA} ranging from 10^{20} to 10^{22} cm^{-3} eV^{-1}. The model and simulation results agree well, demonstrating the validity of our model. When N_{TA} increases, the current above the threshold decreases and the threshold voltage and the subthreshold slope are very weakly affected. Based on (24), only the parameters of the band tail states affect the current, justifying the weak variation of the subthreshold slope according to (25). In contrast, the decrease in the drain current above the threshold is explained by the increase in N_{02} with N_{TA}. The N_{TA} effect studied in

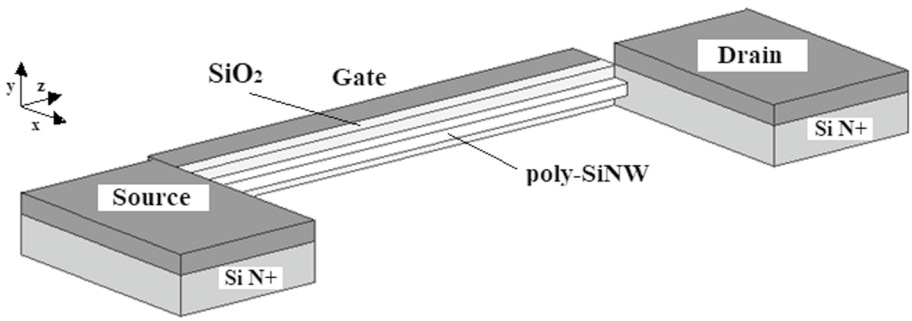

Fig. 2 3D TCAD architecture for the simulated device (not to scale)

Table 1 Device dimensions and DOS parameters

Parameter	Value
Oxide thickness: t_{ox}	30 nm
Nanowire depth (x):T_{sc}	30 nm
Nanowire height (y): W	30 nm
Nanowire length: Z	5 µm
ε_{si}	1.033 pF cm^{-1}
C_{ox}	11.04 µF cm^{-2}
N_{TA}	10^{20}–10^{22} cm^{-3} eV^{-1}
N_{DA}	10^{18}–10^{21} cm^{-3} eV^{-1}
W_{TA}	0.04–0.08 eV
W_{DA}	0.1–1.1 eV
N_{TD}	10^{21} cm^{-3} eV^{-1}
N_{DD}	10^{18} cm^{-3} eV^{-1}
W_{TD}	0.04 eV
W_{DD}	0.1 eV
N_c	8.6×10^{9} cm^{-3}
E_G	1.12 eV
E_{F0}	0.56 eV
μ_0	1400 V.cm^2 s^{-1}
V_{FB}	70 mV

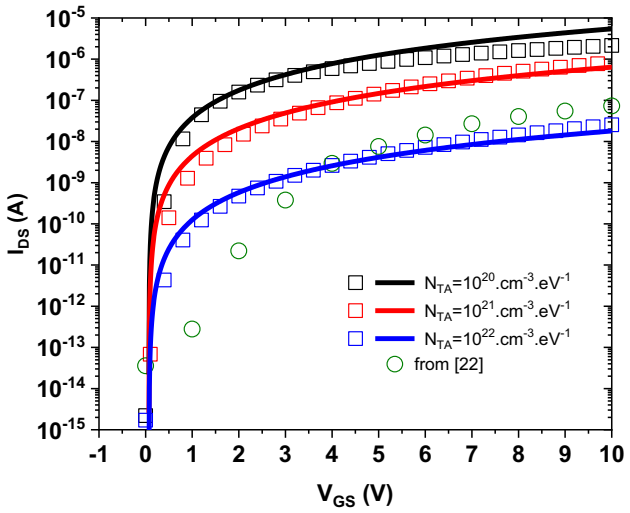

Fig. 3 I_{DS} (V_{GS}) at $V_{DS}=0.5$ V for various N_{TA} ($W_{TA}=0.04$ eV, $N_{DA}=10^{18}$ cm^{-3} eV^{-1}, $W_{DA}=0.1$ eV). Symbol: simulated; line: modeled

this context agrees with the simulations of Gao et al. [21], highlighting the band tail effect on the drain current when the gate voltage exceeds the threshold voltage. Additionally, from (18), $\partial\psi_s/\partial V_{GS}$ exhibits a slope independent of N_{TA}, leading to a less pronounced increase in the surface potential when the device operates above the threshold. However, the experimental characteristics exhibit a high threshold voltage and sub-threshold slope. Clearly, the consideration of N_{TA} alone does not afford a DOS representation that brings the model closer to the experimental characteristics.

Figure 4 shows the transfer characteristics for W_{TA} varying from 0.04 to 0.08 eV while the other parameters are kept fixed. Obviously, the increase in W_{TA} degrades the device performance as the threshold voltage and subthreshold slope increase and the current above the threshold decreases. Below the threshold, W_{TA} significantly affects the subthreshold slope, which increases according to (25), and the drain current decreases with N_{02} above the threshold. Given the W_{TA} range considered, only the band tail states describe the total density of the acceptor traps. Compared to N_{TA}, the effect of W_{TA} is clearly seen on the transfer characteristics as the dominant factor of the slopes below and above the threshold.

Figure 5 shows the transfer characteristics for W_{DA} varying from 0.3 to 1.1 eV, while the other parameters are kept fixed. In this case, the expression for the current depends on N_2 and N_3, and an explicit expression for the drain current cannot be formulated with these two quantities together. Indeed, as mentioned earlier, one of the two parameters subsists in the expression of the current. This fact is illustrated in Fig. 6, which displays the variation in N_2 and N_3 as a function of ψ, where the intersection potential ψ_i corresponds to $N_2(\psi_i)=N_3(\psi_i)$ and is expressed by:

$$q\psi_i = \frac{W_{DA}W_{TA}}{W_{DA}-W_{TA}} \ln\left(\frac{W_{DA}\alpha_D B_D}{W_{TA}\alpha_T B_T}\right) \tag{26}$$

Thus, based on the value of ψ_i, we define two currents I_{deep} and I_{tail}: Above ψ_i (region above the threshold), the drain current is described by I_{tail}, which depends on N_2; N_2

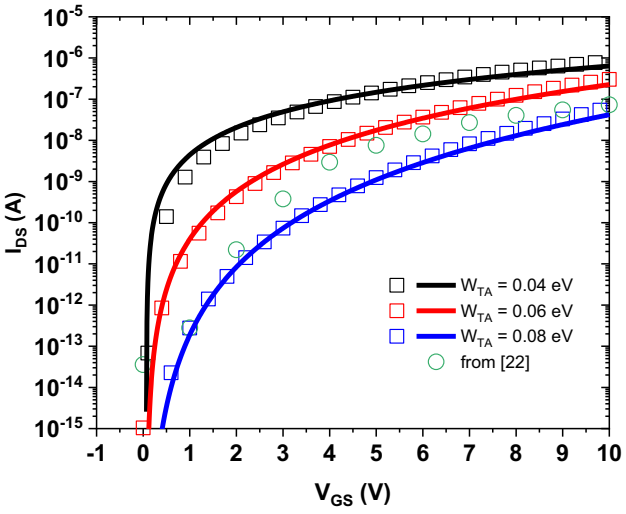

Fig. 4 I_{DS} (V_{GS}) at $V_{DS}=0.5$ V for various W_{TA} ($N_{TA}=10^{21}$ cm^{-3} eV^{-1}, $N_{DA}=10^{18}$ cm^{-3} eV^{-1}, $W_{DA}=0.1$ eV). Symbol: simulated; line: modeled

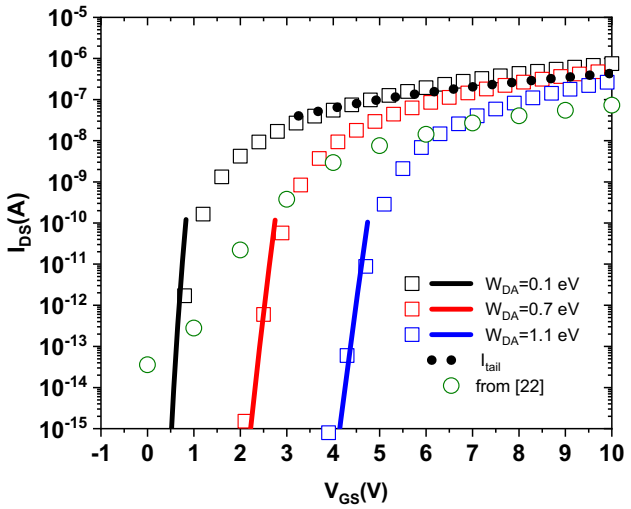

Fig. 5 $I_{DS}(V_{GS})$ at $V_{DS}=0.5$ V for various W_{DA} ($W_{TA}=0.04$ eV, $N_{TA}=10^{21}$ cm^{-3} eV^{-1}, $N_{DA}=10^{18}$ cm^{-3} eV^{-1}). Symbol: simulated; line: modeled

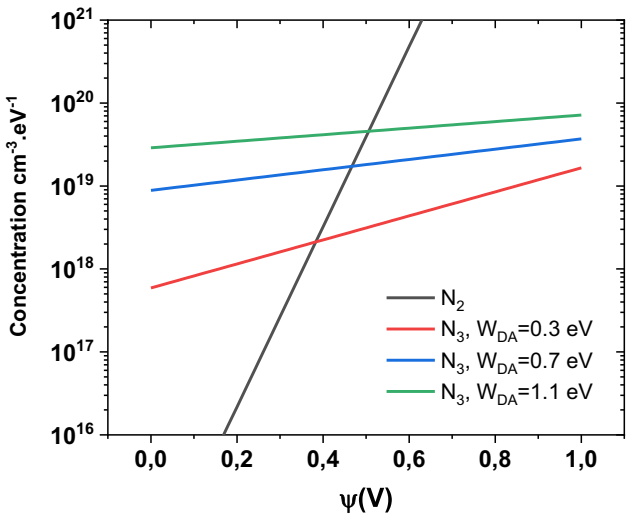

Fig. 6 N_2 and N_3 versus ψ for various W_{DA} ($W_{TA}=0.04$ eV, $N_{TA}=10^{21}$ cm^{-3} eV^{-1}, $N_{DA}=10^{18}$ cm^{-3} eV^{-1})

is kept fixed in this case. Below ψi (below the threshold), the drain current is described by I_{deep}, which depends on N_3. Figure 7 exhibits the I_{deep} current as a function of V_{GS} for a limit value of 10^{-10} A. From the expression of I_{deep}, the transfer characteristics can be differentiated into two regions with a new threshold voltage and a new subthreshold slope depending on W_{DA}. However, in the region below the threshold and for $W_{DA} \geq 0.7$ eV, I_{deep} is drastically weak to the point of being practically immeasurable. Thus, the current is only present above the threshold of I_{deep}, which appears in the subthreshold region of the device and whose slope varies very weakly with W_{DA}. This explains

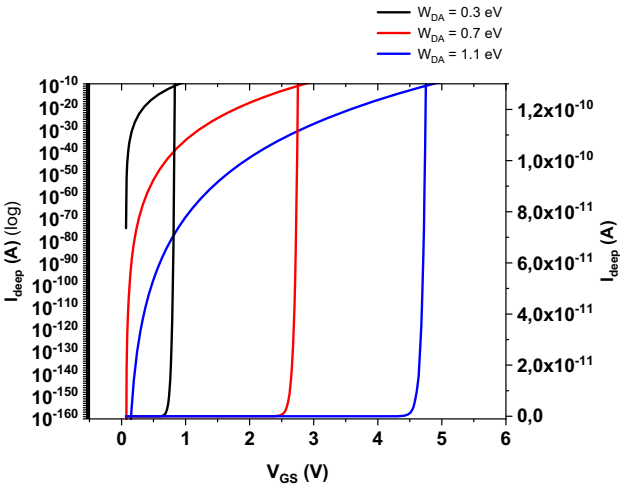

Fig. 7 I_{deep} (V_{GS}) at $V_{DS}=0.5$ V for various W_{DA} values

the small variation in the slope under the device threshold with increasing W_{DA}. The expression of the potential according to (18) shows that its value is negative even when $V_{GS} > V_{FB}$. For the region of the channel near the SiO_2/poly-SiNW interface, the band diagram will exhibit high curvature of the conduction band that is manifested by a strong decrease in the concentration of free electrons. In other words, the region near the SiO_2/poly-SiNW interface is deserted for a positive V_{GS}. On the other hand, a negative surface potential will shift the probability of the occupation function f_A(E) back toward energies below E_{F0}, which will drastically reduce the probability that an acceptor trap will be ionized. Hence, the device performance degrades in the region below the threshold.

Figure 8 shows the transfer characteristics for N_{DA} ranging from 10^{19} to 10^{21} cm^{-3} eV^{-1}. Below an N_{DA} value between 10^{20} and 10^{21} cm^{-3} eV^{-1}, the drain current is described by I_{tail} and I_{deep}, whose subthreshold slope does not vary with N_{DA} (the part of the very weak currents is not shown in the figure). Above a certain value of N_{DA}, only the deep states influence the drain current, whose decrease above the threshold is due to the increase of N_{03} with N_{DA}. Figure 9 displays a fit of the model with the experimental data. Compared to the DOS distribution of polycrystalline silicon referenced in the literature [18], the DOS studied herein displays a high density of deep states. As is known, deep states are afforded by the dangling bonds present in disordered silicon, such as microcrystalline or amorphous silicon. Moreover, our previous study [17] clearly showed that the increase in deep states exhaustively explains the conduction mechanism via VRH for poly-SiNWs with small diameters and presents clear insight into their structure. Moreover, the DOS measurements of Le Borgne et al. [14] confirm our results, showing a high density of acceptor

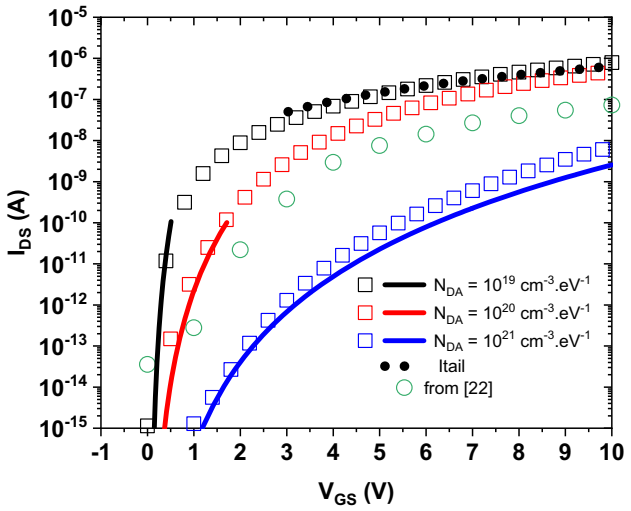

Fig. 8 $I_{DS}(V_{GS})$ at $V_{DS}=0.5$ V for various N_{DA} ($W_{TA}=0.04$ eV, $N_{TA}=10^{21}$ cm^{-3} eV^{-1}, $W_{DA}=0.1$ eV). Symbol: simulated; line: modeled

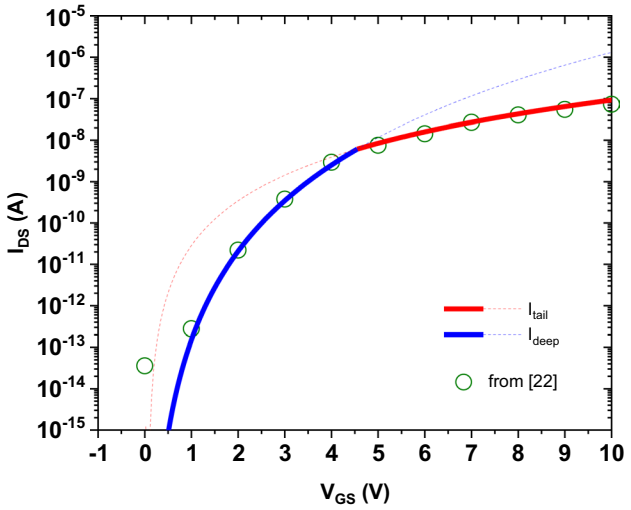

Fig. 9 Transfer characteristics fitted with experimental data [20] for $N_{TA}=10^{21}$ cm^{-3} eV^{-1}; $W_{TA}=0.06$ eV; $N_{DA}=2.10^{20}$ cm^{-3} eV^{-1}; $W_{DA}=0.1$ eV

states for the TFT back gate based on poly-SiNWs realized by the spacer method.

In addition to the performance analysis of poly-SiNW TFTs exhibiting a high defect density, the analytical drain current model developed in this work has an interesting advantage. The explanation for all acceptor DOS parameters in the formulation of the model affords a good understanding of the impact of each parameter on the device behavior. Let us recall, among other things, the expression of the ionized acceptor trap density as a function of the potential, the involvement of each parameter, and its effect on operating below or above the threshold regions via the expressions of the densities N_{02} and N_{03}.

In the case of FETs based on poly-SiNWs, the literature often mentions simulation studies [23–25] and shows similar effects of the variation in the DOS on the performance without presenting an analytical formulation. Hence, the importance of our model is that it can be adopted as a reference to develop other models intended for other devices, such as biochemical sensors based on poly-SiNWs whose operation is governed by the interaction of chemical species surrounding the defects present on the surface of the nanowires [26]. Note that although our model concerns the case of an architecture in which the gate modulates the channel on a single face, it can be extended to other architectures such as the double gate or the gate-all-around.

4 Conclusion

We investigated the performance of poly-SiNW TFTs fabricated using the spacer method by developing an analytical model of the drain current, explicitly showing the DOS parameters described by two exponentials. The impact of these parameters on the transfer characteristics demonstrated that the deep states significantly affect the subthreshold region while the tail states affect the region above the threshold. The fit of the model with the experimental data revealed a higher density of deep states than that for polysilicon, which provides extensive insight into the distribution of acceptor traps in the gap, agreeing well with our previous studies on the conduction mechanism and DOS measurement for poly-SiNWs. On the other hand, the explanation of the DOS parameters in the model of the drain current, in the particular case of TFTs based on poly-SiNWs, presents an interesting advantage for the analytical study of the performance of these devices. This supports the proposal of this model as a reference for the study and development of other models for other devices based on poly-SiNWs.

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Declarations

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