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Single OTA-based tunable resistorless grounded memristor emulator and its application

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Abstract
This paper presents a new systematic design of a grounded memristor emulator circuit. It uses only one active device, namely an operational transconductance amplifier, and one passive element, namely a capacitor. Moreover, the used capacitor is grounded, which is suitable for monolithic integration. The proposed memristor is simple in design and can be used for both incremental and decremental memristor emulators by changing a switch positions. An application of the proposed grounded memristor as a first-order high-pass filter is also realized. Furthermore, the comparison of the proposed memristor emulator with available literature has been included. The proposed memristor emulator provides the following advantageous features such as low active and passive component counts, resistorless, grounded capacitor suitable for monolithic integration, low power consumption, and small area. The obtained results are included which are verified on Cadence Virtuoso at 180-nm Generic Process Design Kit CMOS technology parameter. The proposed emulator occupies the (76.94)·(33.75) μm^2 layout area excluding the capacitor. The pre-layout and post-layout simulation results of the memristor emulator are also presented.

Keywords Current-mode · Memristor emulator · Operational transconductance amplifier · MOSFET · Integrated circuits

1 Introduction

In circuit theory, three basic elements, resistor, capacitor, and inductor, define the relationship between charge, voltage, current, and flux. In 1971, Leon O. Chua postulated the existence of a fourth fundamental two-terminal circuit element called a memristor, which defines the missing relation between charge and flux [1]. Memristors are useful for a wide range of applications, which include amplifier [2], digital logic [3], memory [4], neuromorphic computing [5], neural network [6, 7], synaptic circuit [8], chaotic circuits [9], and oscillators [10].

The first physical memristor was implemented in the HP laboratory in 2008, but unfortunately, this is not commercially available [11]. Over the years, researchers have developed a large number of memristor emulators using various analog building blocks (ABBs) [12–33], some of them are using commercially available ABBs [13, 15–23, 30, 33]. The different ABBs used for the realizations are: operational amplifier (OA) [13, 15], operational transconductance amplifier (OTA) [17, 18, 22, 28], current feedback operational amplifier (CFOA) [16, 19, 21], differential difference current conveyor (DDCC) [12, 14], second-generation current conveyor (CCII) [20, 23], current backward transconductance amplifier (CBTA) [24], current conveyor transconductance amplifier (CCTA) [25, 29], differential voltage current conveyor transconductance amplifier (DVCCTA) [26], voltage differential current conveyor (VDCC) [32], and voltage differencing transconductance amplifier (VDTA) [27, 30, 31, 33]. The critical review reveals that the reported circuits suffer from one or more of the following weaknesses: excessive use of the active components [12, 13, 15–21, 23, 28, 33], excessive use of passive components [12–21, 23–27, 29, 31, 33], use of multiplier which needs precise adjustment with high accuracy [13–15, 17, 18, 20, 22–24, 27, 33], use of passive floating components [13–18, 20, 21, 23–26, 29] which are not suitable for IC fabrication, use of passive resistor [12–27, 29, 31, 33], and use of MOS

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resistor [12, 31, 32]. Moreover, the memristor circuits [13, 15–21, 23] have been realized using bipolar technology. Due to the use of bipolar technology, the memristor emulators are strictly temperature dependent. Moreover, the internal structures of [14, 22, 24–26, 29] memristor emulators suffer from the excessive number of transistors and the complexity, which results in a high-silicon area in the case of on-chip fabrication. Furthermore, topologies [19, 29] used two different types of ABBs, which is not encouraged from an IC point of view.

The authors in this paper proposed a single-OTA-based memristor emulator that overcomes all the aforementioned drawbacks. The proposed memristor emulator uses only one OTA and one capacitor. The used capacitor is grounded and hence is suitable for IC fabrication. The design is simulated using Cadence Virtuoso software with 180-nm Generic Process Design Kit (GPDK) CMOS technology parameters. To check the functionality of the proposed memristor emulator, an application as first-order high-pass filter is also included. Simulation results show that the proposed circuit agrees well with the theory. The pre-layout and post-layout results are also included.

This article is organized as follows. In Sect. 2, the design of the proposed memristor emulator is described. The performance simulation of the proposed memristor emulator is discussed in Sect. 3. In Sect. 4, the application of the proposed circuit is discussed, followed by comparison in Sect. 5. The conclusion is given in Sect. 6.

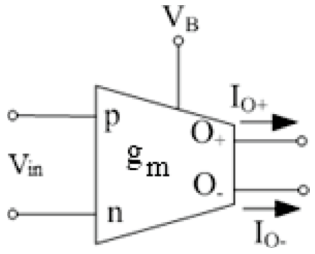


Fig. 1 Symbol of DO-OTA

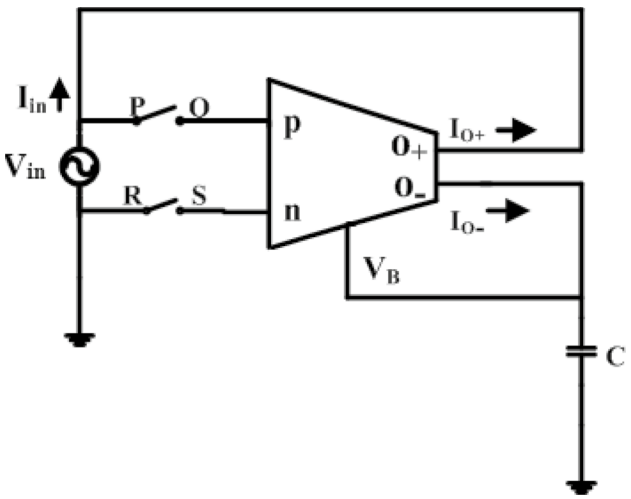


Fig. 2 Proposed memristor emulator

2 Proposed grounded memristor emulator circuits

A memristor is a two-terminal electrical component. It limits or controls the flow of electrical current in a circuit and also remembers or recollects the amount of charge that has previously flowed through it. Memristors are important because they retain memory without power, and are non-volatile. A memristor is a semiconductor that joins a capacitor, resistor, and inductor to make a fourth new kind of element whose resistance is called memristance that varies as a function of current and flux. Memristors, a combination of "memory resistors," are a kind of passive circuit element that maintains a relationship between the time integrals of current and voltage across a two-terminal element. When the current flows in one direction, the resistance increases; in contrast, when the current flows in the opposite direction, the resistance decreases. However, resistance cannot go below zero. When the current is stopped, the resistance remains in the value that it had previously [1–4].

The operational transconductance amplifier (OTA) has a voltage input and a current output device. The symbol of double output OTA (DO-OTA) is shown in Fig. 1 [34], where V_{in}, I_{O+}, I_{O-}, V_B are the differential input voltage, output current at positive terminal, output current at the negative terminal, and bias voltage, respectively.

The ideal transfer characteristics of an OTA for input V_{in} are expressed as

$$I_{O\pm} = \pm g_m V_{in} \tag{1}$$

where g_m, $I_{O\pm}$ and $V_{in} = V_{in+} - V_{in-}$ are the transconductance, output current, and differential input voltage, respectively. Moreover, the V_{in+} and V_{in-} are the applied input voltages at the positive (p) and negative (n) terminals of the OTA, respectively.

The routine analysis results in the expression of g_m as

$$g_m = \frac{k}{\sqrt{2}}\left(V_B - V_{ss} - 2V_{th}\right) \tag{2}$$

where $k = \mu_n C_{ox}\frac{W}{L}$ is MOS device parameter and μ_n, C_{ox}, W, L, and V_{th} are mobility, oxide capacitance, width, length, and the threshold voltage of the MOS transistor, respectively.

The proposed grounded memristor emulator is shown in Fig. 2. By interchanging the switch, it can perform the operation of an incremental- and decremental-type memristor

emulator. If cross-coupled connected the terminal pins of the switch, i.e., pins P, Q, and R, S are interconnected (P–S and R–Q), an incremental-type memristor emulator is obtained shown in Table 1.

The input current (I_{in}), capacitor current (I_c), and bias voltage (V_B) are obtained as

$$I_{in}(t) = -I_{O+} = g_m V_{in}(t) \tag{3}$$

$$I_c(t) = +I_{O-} = g_m V_{in}(t) \tag{4}$$

$$V_B = \frac{1}{C}\int I_c(t)\mathrm{d}t = \frac{g_m}{C}\int V_{in}(t)\mathrm{d}t = \frac{g_m \phi_{in}}{C} \tag{5}$$

where $\phi_{in} = \int V_{in}(t)\mathrm{d}t$ is the total flux obtained by the memristor. Putting the value of V_B into (2), we get

$$g_m = \frac{k}{\sqrt{2}}\left(\frac{g_m \phi_{in}}{C} - V_{ss} - 2V_{th}\right) \tag{6}$$

Substituting (6) into (3), we get the input current expression as

$$I_{in}(t) = \frac{k}{\sqrt{2}}\left(\frac{g_m \phi_{in}}{C} - V_{ss} - 2V_{th}\right)V_{in}(t). \tag{7}$$

Hence, the memconductance $W(\phi_m)$ of the proposed incremental memristor is obtained as

$$W(\phi_m) = \frac{I_{in}(t)}{V_{in}(t)} = -\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) + \frac{k}{\sqrt{2}}\left(\frac{g_m \phi_{in}}{C}\right). \tag{8}$$

Similarly, if we change the switch connections, i.e., pins P–Q and R–S changing the polarity of time-variant part of memconductance of (8), a decremental-type memristor emulator is obtained as

$$W(\phi_m) = \frac{I_{in}(t)}{V_{in}(t)} = \frac{k}{\sqrt{2}}(V_{ss} + 2V_{th}) + \frac{k}{\sqrt{2}}\left(\frac{g_m \phi_{in}}{C}\right) \tag{9}$$

where g_m is controllable by bias voltage V_B, which makes the proposed emulator electronically tunable.

Equations (8) and (9) show that the proposed circuit works as incremental and decremental memristor emulators, respectively, where $\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})$ is the constant term and $\frac{k}{\sqrt{2}}\left(\frac{g_m \phi_{in}}{C}\right)$ being the time-varying term as ϕ_{in} is the function of time-varying input signals. For $\phi_{in} = 0$, memconductance provides a constant value in both types of incremental and decremental emulators.

Table 1 Operation of the proposed memristor in the incremental and decremental mode

S. No	Connection	Operation mode
1	P–Q, R–S	Decremental
2	P–S, R–Q	Incremental

3 Simulation results

In this section, the proposed grounded memristor emulator of Fig. 2 using the CMOS structure of the DO-OTA [34] shown in Fig. 3 has been simulated. The aspect ratios of the transistors for Fig. 3 are given in Table 2. All transistors are in the saturation region. The supply voltages $V_{DD} = -V_{SS} = 1.2$ V and bias voltage $V_B = 0.45$ V are used for simulations, where V_{DD}, V_{SS}, and V_B are positive supply voltage, negative supply voltage, and bias voltage, respectively. The DC transfer characteristics of Fig. 3 are shown in Fig. 4.

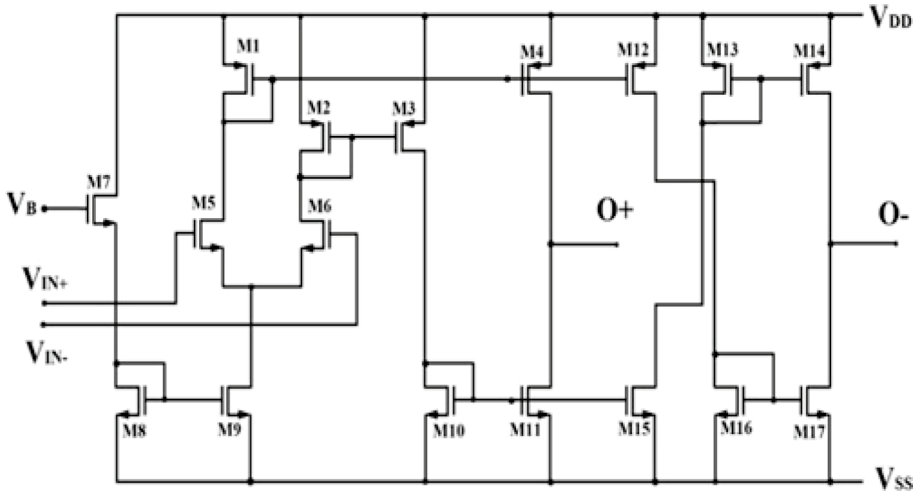


Fig. 3 CMOS implementation of DO-OTA

Table 2 OTA dimension used in the simulation

MOS transistors	W (μm)	L (nm)
M1	32	395
M2, M3, M4, M12, M13, M14	32	370
M5, M6, M7, M8, M9, M10, M11, M15, M16, M17	14	580

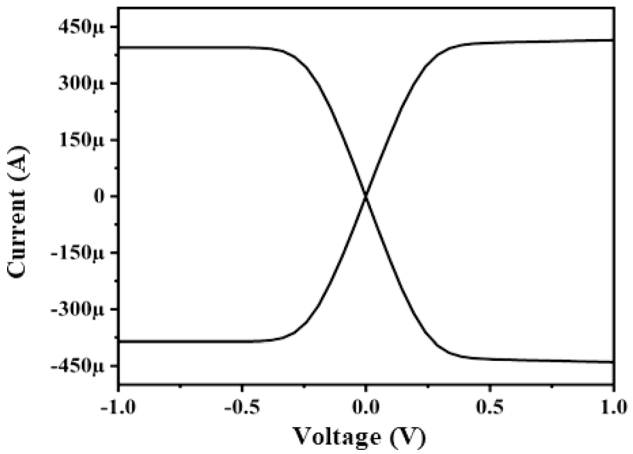


Fig. 4 DC transfer characteristics of Fig. 3

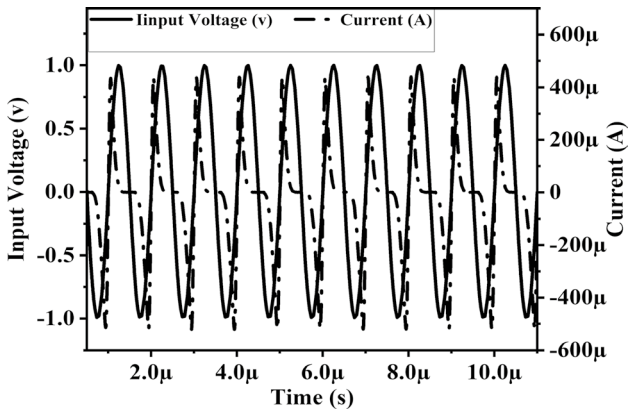


Fig. 5 Transient response of proposed memristor emulator using a 1 V sinusoidal input signal with a 1 MHz frequency

Figure 5 shows the transient response of the grounded memristor emulator of Fig. 2. For transient analysis, a sinusoidal voltage signal of amplitude 1 V and frequency 1 MHz has been applied to the input terminal of the proposed emulator. Figure 6 shows the ac response in 20 dB of Fig. 2 with 0.5 V ac magnitude of the input DC voltage and $V_B = 0.45$ V is applied.

Figure 7 is obtained when unit pulse voltage is applied for both incremental and decremental memristor emulators. The applied unit pulse voltage source value is taken as $V_1 = 0$ V and $V_2 = 1$ V. For a decremental graph, we select positive nodes of applied input unit pulse voltage and for an incremental graph, we select negative nodes of applied input unit pulse voltage. From Fig. 7, it can be observed that the current vs. time plot is increasing and decreasing with respect to the time interval for incremental and decremental topologies, respectively.

The relation between the voltage–current of the proposed grounded memristor emulator is shown in Fig. 8. The input sinusoidal voltage is applied with 1 V amplitude and different frequencies such as 200 kHz, 300 kHz, 400 kHz, 500 kHz, and 1 MHz. The hysteresis loop is shown in Fig. 8a, b by the varying capacitor at a fixed value of frequency 400 kHz, the amplitude of input signal = 1 V. It is noted that by increasing of capacitor value the current through the memristor will be decreased. From Eq. (9), it is observed that current through the memristor is inversely proportional to the capacitance and its effect is observed on the V–I curve as expected. The hysteresis loop is shown in Fig. 8c by varying the frequency at a fixed value of capacitor is 250 pF and input sinusoidal voltage is applied with 1 V amplitude and different frequencies. The simulated results clearly show that the voltage–current relationship is very sensitive to the applied frequency of the input sinusoidal signal. Figure 8d shows the effect on hysteresis loop with temperature varying [− 40°, − 32°, 56°, 80°] at fixed value of frequency 1 MHz, capacitor value of $C_1 = 50$ pF and amplitude of input signal = 1 V. The simulated results clearly show that the voltage–current relationship is very sensitive to the applied frequency of the input sinusoidal signal.

The important aspect when design moves toward the IC implementation is the process variation. The proposed grounded memristor is examined for the different processes like SS (slow N and slow P transistors), FS (fast N and slow P transistors), FF (fast N and fast P transistors), SF (slow N and fast P transistors), and NN (nominal N and nominal P transistors). Figure 9 shows the process variation at $C = 300$ pF and $f = 250$ kHz with 1 V amplitude. It reveals that the current flow in the case of FF is greater than other processes.

The layout of the proposed memristor emulator is given in Fig. 10. The layout occupies (76.94 μm)·(33.75 μm) area

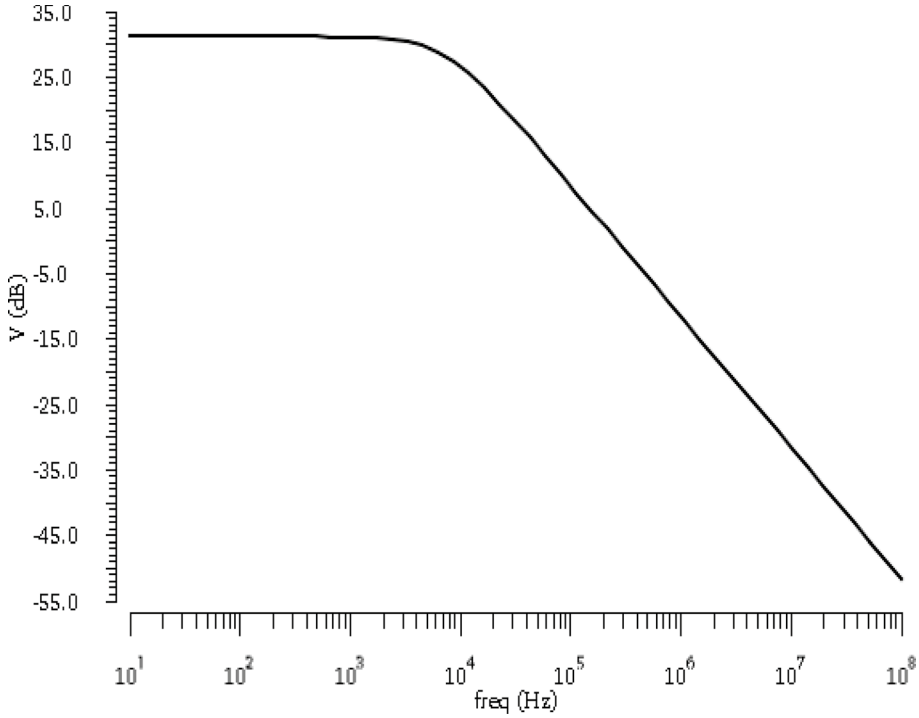


Fig. 6 Frequency response of proposed memristor emulator

excluding the capacitor. The average power consumption in the NN (normal n and normal p transistor) process of the proposed emulator is found to be 411.2 µW. The applied input signal is sinusoidal with an amplitude of 1 V, at a 1 MHz frequency. The capacitor value is chosen for 250 pF. The pre-layout and post-layout simulation results of the proposed memristor are shown in Fig. 11. The post-simulation is done after extracting the parasitic capacitance and resistance.

4 Applications of proposed memristor emulator

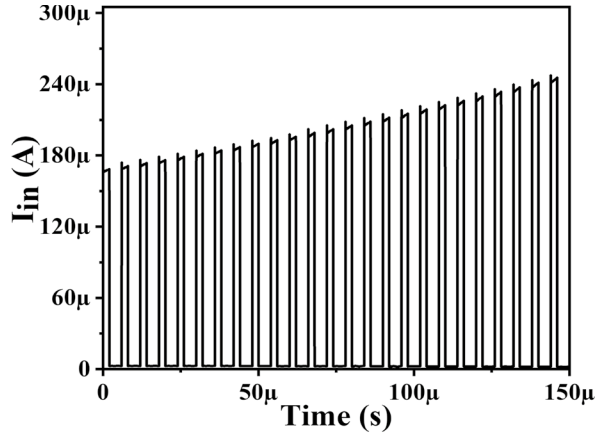
In this section, two application examples are included to verify the functionality of the proposed memristor emulator: first, as a single and parallel configuration, and second as a first-order high-pass filter (HPF).

4.1 Different combinations of memristor emulator

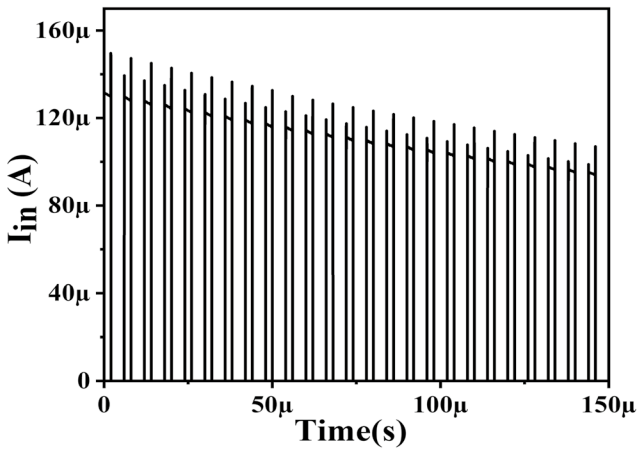
To check the performance of the proposed OTA-based memristor emulator, it is connected in a parallel configuration and compares the obtained result with a single memristor. In a parallel configuration, the memristor value is half by the single memristor, then we said, the proposed circuit is working correctly. The single and parallel combination of the memristor is shown in Fig. 12. To check, through simulation applied a sinusoidal signal with an amplitude of 1 V with 250 kHz frequency. It can see that the proposed memristor emulator works properly as shown in Fig. 13. According to that parallel memristor emulator, the value of the memristor is halved by the single memristor.

4.2 First-order high-pass filter

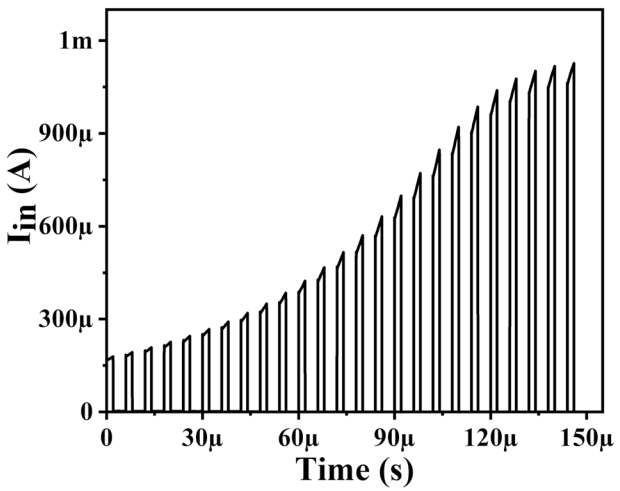
In this section, the first-order passive high-pass filter (HPF) is compared with memristor emulator-based first-order HPF. Figure 14 shows the resistor–capacitor (RC) and proposed memristor–capacitor (MC)-based first-order high-pass filter (HPF), respectively. The values chosen for simulation are $C = 10$ pF, $R = 13$ MΩ for the cut of the frequency of 1.224 kHz. The frequency response of both the RC and MC-based filters is shown in Fig. 15. This shows that the proposed emulator works very well.


300µ
240µ
180µ
120µ
60µ
0
I_{in} (A)
0
50µ
100µ
150µ
Time (s)

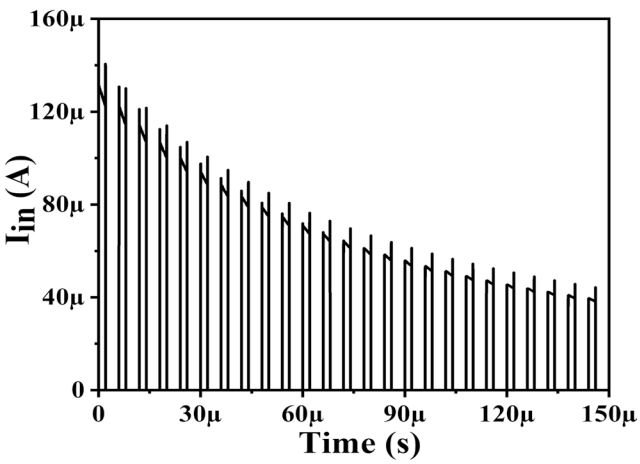
(a)


160µ
120µ
80µ
40µ
0
I_{in} (A)
0
50µ
100µ
150µ
Time(s)

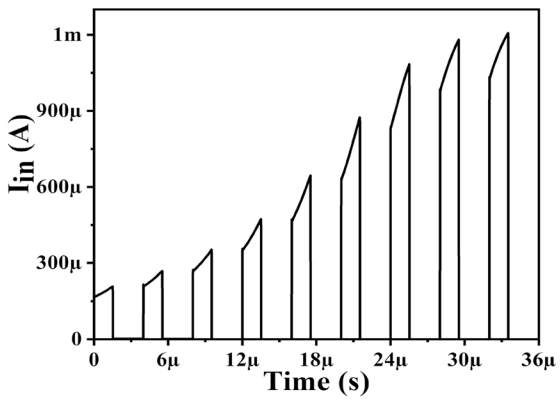
(b)


1m
900µ
600µ
300µ
0
I_{in} (A)
0
30µ
60µ
90µ
120µ
150µ
Time (s)

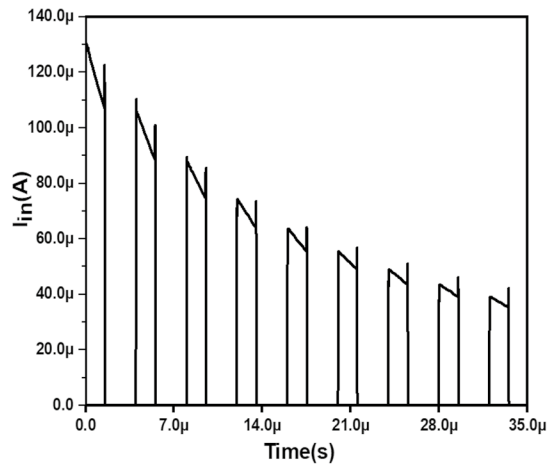
(c)


160µ
120µ
80µ
40µ
0
I_{in} (A)
0
30µ
60µ
90µ
120µ
150µ
Time (s)

(d)


1m
900µ
600µ
300µ
0
I_{in} (A)
0
6µ
12µ
18µ
24µ
30µ
36µ
Time (s)

(e)


140.0µ
120.0µ
100.0µ
80.0µ
60.0µ
40.0µ
20.0µ
0.0
I_{in}(A)
0.0
7.0µ
14.0µ
21.0µ
28.0µ
35.0µ
Time(s)

(f)

◂**Fig. 7** The various plot between current vs. time for unit pulse voltage for grounded memristor emulator at: **a** incremental topology with $C=100$ nF, time period $(t_p)=6$ µs, pulse width $(t_d)=2$ µs, **b** decremental topology with $C=100$ nF, time period $(t_p)=6$ µs, pulse width $(t_d)=2$ µs, **c** incremental topology with $C=20$ nF, time period $(t_p)=6$ µs, pulse width $(t_d)=2$ µs, **d** decremental topology with $C=20$ nF, time period $(t_p)=6$ µs, pulse width $(t_d)=2$ µs, **e** incremental topology with $C=5$ nF, time period $(t_p)=4$ µs, pulse width $(t_d)=1.5$ µs, **f** decremental topology with $C=5$ nF, time period $(t_p)=4$ µs, pulse width $(t_d)=1.5$ µs

5 Comparison of proposed memristor emulator with other available in the literature

The detailed comparative analysis of the proposed circuit with existing memristor emulators available in the literature is given in Table 3.

It is concluded from Table 3 that

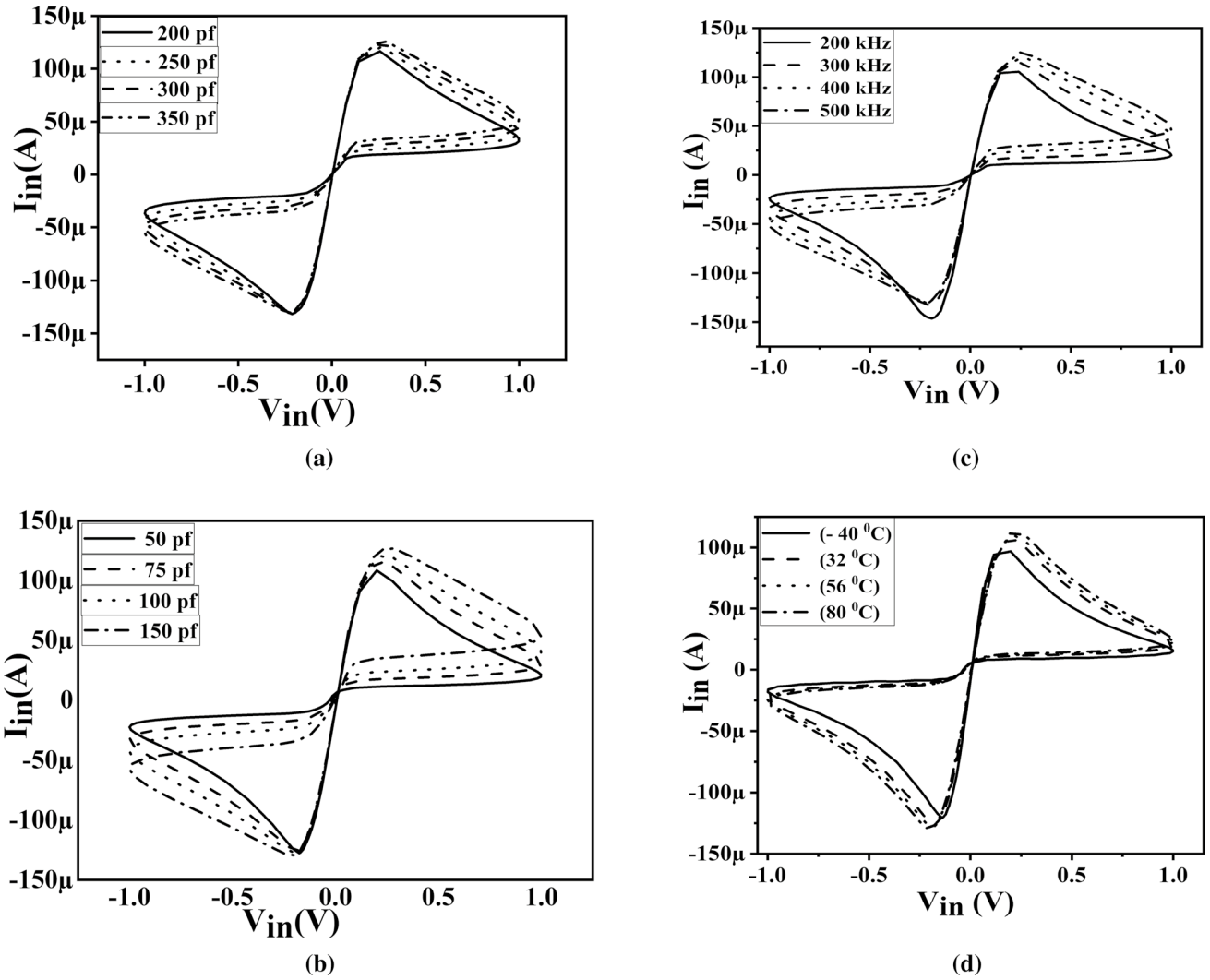


Fig. 8 Voltage–current plot characteristic for decremental memristor emulator of: **a** fixed $f=400$ kHz, and different value of capacitor, **b** fixed $f=1$ MHz, and different value of capacitor, **c** fixed $C=250$ pF, and different frequency, **d** fixed $C=50$ pF, fixed $f=1$ MHz, and different value of temperature

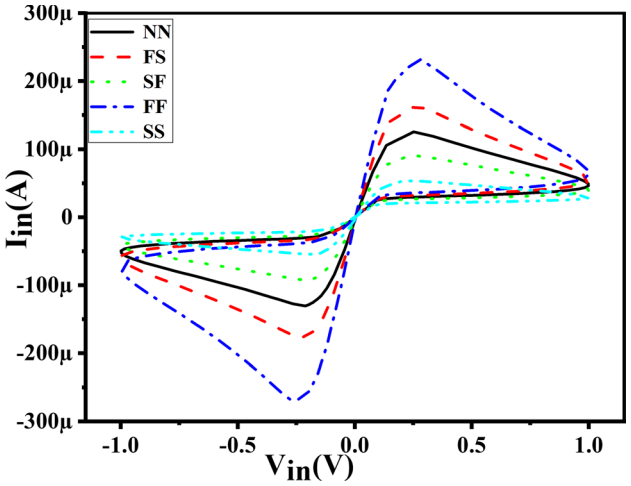


Fig. 9 Process variation effect of the proposed memristor emulator for different process

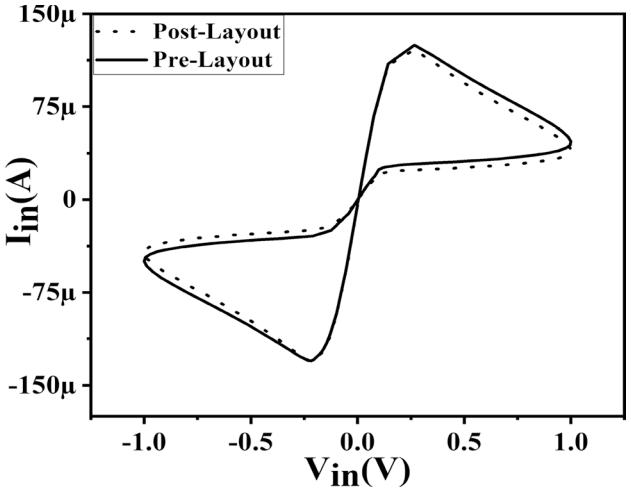


Fig. 11 Post-layout simulation results of the proposed memristor emulator

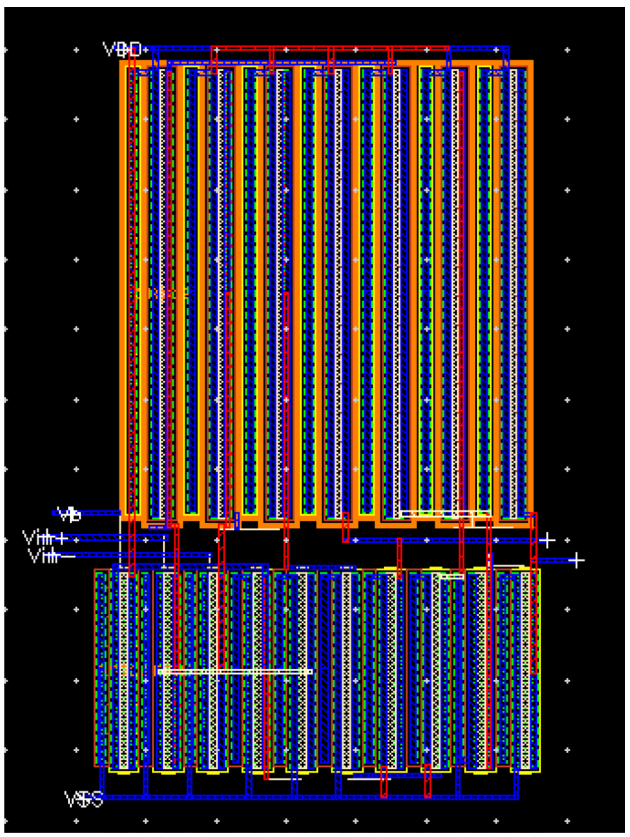


Fig. 10 The layout of the proposed memristor emulator circuit in Fig. 2

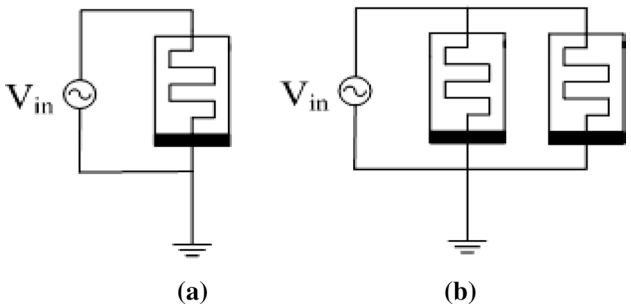


Fig. 12 Memristor combination in: **a** single, **b** parallel

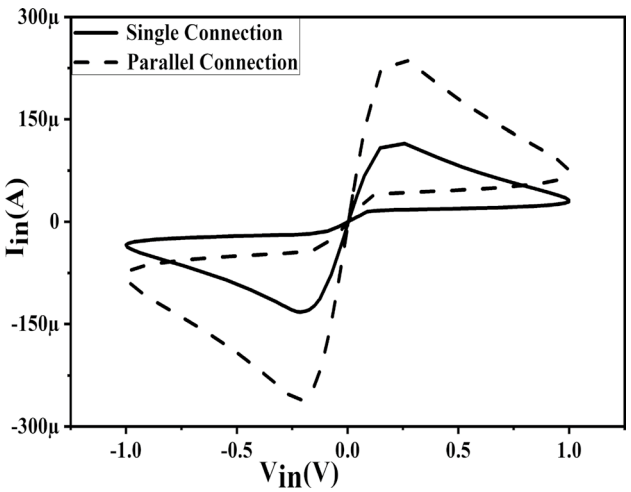


Fig. 13 V–I characteristics for an amplitude of input signal, Am = 1 V, $C = 300$ pF at 300 kHz for single and parallel combinations of the proposed emulator

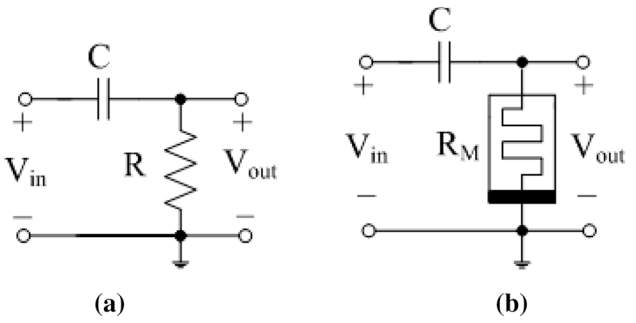


Fig. 14 Circuits diagram of high-pass filter: **a** RC based, **b** MC based

1. The topologies [12–24, 27–29, 33] use two or more analog building blocks, whereas the proposed emulator uses only one OTA.
2. The topologies [13–15, 17, 18, 20, 22–24, 27, 33] use the analog multiplier to obtain the nonlinear characteristics of the memristor emulator, and hence, circuits become complex and required precise adjustment with high accuracy. However, the proposed topology is designed without using multipliers.
3. The topologies [13–18, 20, 21, 23–26, 29] use passive floating components, whereas the proposed emulator topology uses only grounded components that are suitable for the IC fabrication point of view.
4. The reported memristor emulators in [12–27, 29, 32, 33] use resistors in the design, while the proposed topology is resistorless.
5. The maximum operating frequency achieved by the topologies [12, 13, 15–24, 30, 33] is in the range of kHz, while the proposed design can operate up to 1 MHz.
6. The topologies [13, 15–21, 23] have been realized using bipolar technology which is strictly temperature dependent, whereas the proposed emulator is MOS based.
7. The topologies [19, 29] use two different types of ABBs, which is not encouraged from an IC point of view, whereas the proposed emulator uses only a single ABB.
8. The topology [32] required more number of MOS transistors to implement ABB as compared to the proposed design that uses less transistors.

Therefore, based on the above discussion, it is concluded that the performance of the proposed memristor emulator is better than most of the designs available in the literature.

6 Conclusion

In this paper, we have proposed a new memristor emulator circuit using only one OTA as an active element and one grounded capacitor. The simple switching connection can be used to realize both the decremental and incremental types of memristor emulators. The proposed memristor emulator is simple and suitable for integrated circuit implementation. It provides the following advantageous features: (1) only one active component: OTA, (2) only one passive component: capacitor, (3) capacitor is grounded, which is suitable for monolithic integration, and (4) low power consumption. The

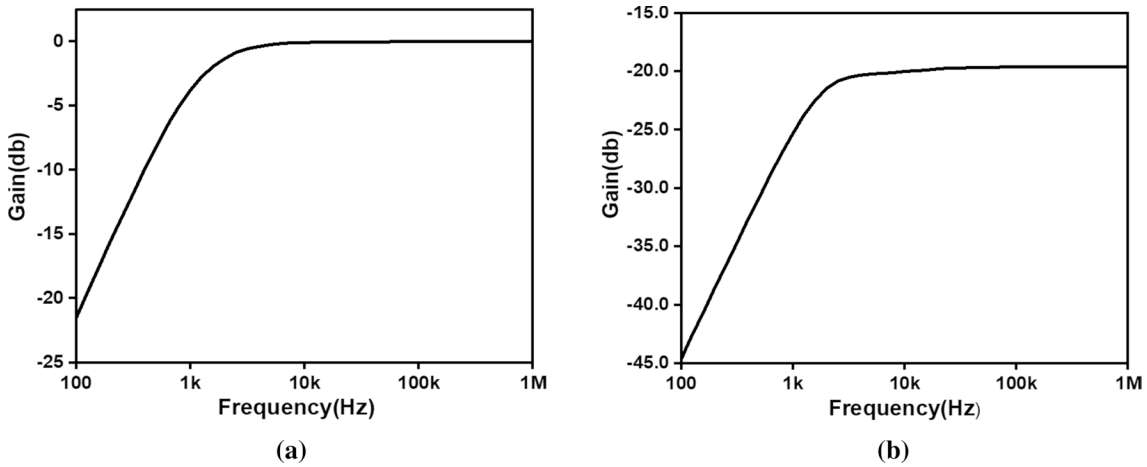


Fig. 15 Cadence result showing the frequency response for **a** RC-based HPF, **b** MC-based HPF

Table 3 Comparison of the proposed memristor emulator with available literature

References	Number of active components	Number of passive components	Resistorless	Type	Max. operating frequency
[12]	5DDCC	1C, 4R	No	Grounded	–
[13]	5OA, 1MULT	1C, 8R	No	Floating	–
[14]	1DDCC, 1MULT	1C, 2R	No	Floating	1 MHz
[15]	2OA, 1MULT	1C, 6R	No	Grounded	20.2 kHz
[16]	3 CFOA, 1D	2C, 4R	No	Grounded	–
[17]	6OTA, 1MULT	1C, 2R	No	Grounded	kHz
[18]	2OTA, 1MULT	1C, 4R	No	Floating	kHz
[19]	2CFOA, 1OTA	2C, 3R	No	Grounded	–
[20]	2CCII, 1MULT	1C, 2R	No	Grounded	160 kHz
[21]	4 CFOA, 2D	14C, 4R	No	Floating	–
[22]	1MO-OTA, 1MULT	1C, 1R	No	Grounded	kHz
[23]	4CCII+, 1MULT	1C, 3R	No	Floating	40 kHz
[24]	1CBTA, 1MULT	1C, 2R	No	Grounded	kHz
[25]	1CCTA	1C, 3R	No	Grounded	10 MHz
[26]	1DVCCTA	1C, 3R	No	Grounded	1 MHz
[27]	1VDTA, 1MULT	1C, 2R	No	Floating	2 MHz
[28]	2OTA	1C	Yes	Grounded	8 MHz
[29]	1CCTA, 1CCII	3R, 1C	No	Floating	5 MHz
[30]	1VDTA	1C	Yes	Grounded	6 kHz
[31]	1VDTA, 2MOS	2R, 1C	No	Floating	50 MHz
[32]	1VDCC, 2MOS	1C	No*	Grounded	2 MHz
[33]	2VDTA, 1MULT	2R, 1C	No	Grounded	10 kHz
Proposed	1OTA	1C	Yes	Grounded	1 MHz

MULT, multiplier; D, diode

*MOS-based resistor

pre-layout and post-layout simulation results of the proposed circuit are also included. All the theoretical concepts are verified using Cadence Virtuoso Analog Design Environment software with 180-nm generic process design kit (GPDK) technology parameters.

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Data availability All the data related to the research are included in the article. Any additional data required by any reader will be provided on request to the corresponding author.

Declarations

Conflict of interest The authors have no conflict of interest to declare that are relevant to the content of this article.

Consent to participate We agree to the terms and policies for the publication of the articles.

Consent for publication We agree to the terms and policies for the publication of the articles.

Human and animal rights Accepted principles of ethical and professional conduct have been followed. No human or animals participation is involved in the research.

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