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Temperature sensitivity analysis of dual material stack gate oxide source dielectric pocket TFET

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Abstract
The variation of the temperature-dependent performance of an electronic device is one of the major concerns in predicting the actual electrical characteristics of the device as the bandgap of semiconducting material varies with temperature. Therefore, in this article, we investigate impact of temperature variations ranging from 300 to 450K on the DC, analog/ radio frequency, and linearity performance of dual material stack gate oxide-source dielectric pocket-tunnel-field-effect transistor (DMSGO-SDP-TFET). In this regard, a technology computer-aided design simulator is used to analyze DC, and analog/radio-frequency performance parameters, such as carrier concentration, energy band variation, band-to-band tunneling rate, $I_{DS} - V_{GS}$ characteristics, transconductance (g_m), cut off frequency (f_T), gain-bandwidth product, maximum oscillating frequency (f_{max}), transconductance frequency product, and transit time (τ) considering the impact of temperature variations. Furthermore, linearity parameters, such as third-order transconductance (g_{m3}), third-order voltage intercept point (VIP3), third-order input-interception point (IIP3), and intermodulation distortion (IMD3) are also analyzed with temperature variations as these performance parameters are significant for linear and analog/radio-frequency applications. Moreover, the performance of the proposed DMSGO-SDP-TFET is compared with the conventional dual-material stack gate oxide-tunnel-field-effect transistor (DMSGO-TFET). From the comparative analysis, in terms of percentage per kelvin, the DMSGO-SDP-TFET demonstrates lesser sensitivity towards temperature variation. Hence, the proposed DMSGO-SDP-TFET is a suitable candidate for low-power switching, and biosensing applications at elevated temperatures as compared to conventional DMSGO-TFETs.

Keywords Dielectric pocket · Temperature sensitivity · Stack gate-oxide · Linearity

1 Introduction

To overcome the scaling issues of conventional MOSFETs, the tunnel field-effect transistor (TFET), based on the quantum tunneling mechanism, has emerged as an alternative device to conventional MOSFETs due to lower subthreshold swing (SS) below 60 mV/decade, immunity to various short channel effects, and low OFF-state current (I_{OFF}) [1–5]. However, TFETs have been reported some major limitations, such as ambipolar current, lower ON-state current (I_{ON}) and poor analog/radio frequency performance, due to inefficient band-to-band tunneling [6]. Therefore, to overcome the lower ON-state current issue, various methods have been reported by the researchers, such as double-gate TFET, work-function engineering, hetero-dielectric, stacked-gate structure, electrically doped (ED), pocket doping, dielectric pocket, Extended Source TFET, dual material and gate over source overlap [6–22]. Furthermore, to address the ambipolar current issue, various methods have been reported, such as hetero-dielectric, work-function engineering, stacked gate structure, pocket doping, dual material gate [23–25]. In addition to the above issues, performance variation with temperature is also one of the major causes of concern in TFETs. Several studies [26–30] have reported temperature dependence performance of various TFET structures.

In the previous work [21], to enhance the DC, analog/ radio frequency performance of the device, authors have proposed DMSGO-SDP-TFET with optimized dielectric pocket at the source-channel junction and reported an improved performance in terms of higher ON-state current ($I_{ON} = 1.47 \times 10^{-4}$ A) at ($V_{GS} = V_{DS} = 1.0$ V), smaller point subthreshold swing (SS) = 15.7 mV/decade, maximum I_{ON}

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/I_{OFF} ratio (3.14×10^{12}), transconductance ($g_m = 1.02\times10^{-3}$ S), and cut-off frequency ($f_T = 193$ GHz).

However, the operating temperature always impacts the on-chip performance of the device. With increase the number of transistors in the integrated circuits (ICs), level of heat dissipation increases, which leads to rise the operating temperature of the chip and hence of the device (transistor). Furthermore, from the perspective of transistor applications in some harsh environments (where the operating temperature differs from the room temperature) such as wireless/mobile/satellite communications, military, medical equipment, avionics, furnace temperature control, automobiles, etc. The integrated circuit chips employed for analog/RF applications needs a more accurate prediction of electrical characteristics of the device at higher temperatures. Hence, first time we have done extensive study for temperature sensitivity analysis of DMSGO-SDP-TFET as well as conventional DMSGO-TFET, also compared the temperature sensitivity of these devices under same bias conditions in terms of DC characteristics, analog/radio frequecncy, and linearity distortion performance parameters using TCAD Simulations.

The remaining part of this paper is organized as follows. Section 2 presents the structural and simulation setup details. Section 3 describes the temperature sensitivity of DMSGO-TFET and DMSGO-SDP-TFET in three parts. The first part presents a temperature sensitivity analysis of various DC parameters, the second part investigates the analog/radio frequency performance and the third part presents the linearity and distortion performance at different temperatures. Finally, the main findings of this work are concluded in Sect. 4.

2 Device structure, parameters and simulation details

Fig. 1a, b illustrate the 2D structural views of conventional DMSGO-TFET and the proposed DMSGO-SDP-TFET for the parameters listed in Table 1. A stack gate oxide approach (low-k/high-k stack gate oxide i.e. SiO_2/HfO_2 stack) is used to provide better quality oxide/channel interface which enhances the ON-state current [30]. The entire length of the stack gate (L_G) is considered 50 nm with SiO_2 oxide layer thickness of (0.8 nm) and HfO_2 oxide layer thickness of (1.2 nm) [19]. Furthermore, the total gate length (L_G) of both devices is partitioned into three parts: tunneling gate (M_1), control gate (M_2), and auxiliary gate (M_3) with different length (L_1, L_2, L_3) and work function (ϕ_1, ϕ_2, ϕ_3), respectively. The control gate workfunction (ϕ_2) is considered 4.4 eV which corresponds to the metal molybdenum (Mo) (4.36–4.95 eV). The work functions (ϕ_1 and ϕ_3) are considered 4.0 eV which corresponds to metal aluminum (Al) (4.0–4.26 eV) [24]. The combination of stack gate oxide approach with workfunction engineering ($\phi_1 = \phi_3 = 4.0$ eV $< \phi_2 = 4.4$ eV) and dielectric pocket at the source- channel interface is used to enhance the ON-state current, reduce leakage current, improve the switching ratio, subthreshold swing and analog /radio frequency performance of the device.

Table 1 List of device parameters

Parameters	DMSGO-TFET	DMSGO-SDP-TFET
Gate length (L_G)	50 nm	50 nm
SiO_2 thickness (T_{SiO_2})	0.8 nm	0.8 nm
HfO_2 thickness (T_{HfO_2})	1.2 nm	1.2 nm
Pocket thickness	–	2 nm
Pocket height	–	4 nm
Silicon film thickness (T_{si})	10 nm	10 nm
Channel doping (N_{ch})	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
Source doping(p type) (N_S)	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Drain doping(n type) (N_D)	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
HfO_2 dielectric constant (K)	25	25
Tunnel gate length (L_1)	10 nm	10 nm
Control gate length (L_2)	25 nm	25 nm
Auxiliary gate Length (L_3)	15 nm	15 nm
Tunnel gate workfunction (ϕ_1)	4.0 eV	4.0 eV
Control gate workfunction(ϕ_2)	4.4 eV	4.4 eV
Auxiliary gate workfunction(ϕ_3)	4.0 eV	4.0 eV

The temperature sensitivity of the proposed DMSGO-SDP-TFET is analyzed using TCAD simulations. For this, suitable models are incorporated such as the nonlocal band-to-band tunneling (BTBT) model is considered to measure the tunneling probability across the junctions. The Shockley-Read-Hall model is enabled to account for the minority carrier recombination effect. The bandgap narrowing model is used to consider the bandgap narrowing caused by high doping concentration. In our simulations, the Quantum confinement effect is not taken into account as it is significant only if the thickness of the Si body is less than 10 nm. In addition to these models, Newton's method was used to provide strong coupling between the resulting equations in order to improve current convergence.

3 Results and discussion

3.1 Temperature sensitivity analysis of DC parameters

This section presents the comparative temperature-sensitive performance analysis of conventional DMSGO-TFET and

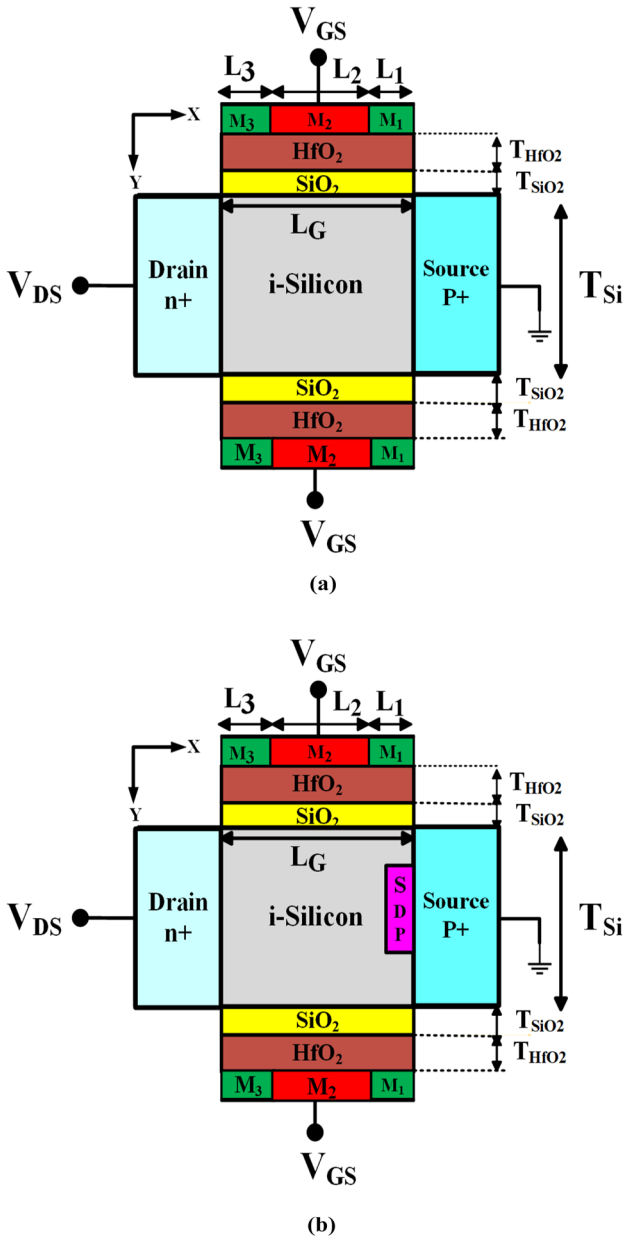

Fig. 1 2-D schematic view of **a** conventional DMSGO-TFET and **b** DMSGO-SDP-TFET [21]

proposed DMSGO-SDP-TFET in terms of carrier concentration, energy band variation, BTBT Variation, $I_{DS} - V_{GS}$ characteristics, threshold voltage variation (V_{TH}) and average subthreshold swing variation at elevated temperatures ranging from 300 to 450K.

Fig. 2a, b depict the ON-state carrier concentration variation with temperature ranging from 300 to 450K for conventional DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from these figures, due to stack gate oxide with lower work functions ($\phi_1 = \phi_3 = 4.0$ eV), at the source (drain) junctions, the electron (hole) concentration increases (decreases) in the channel, respectively, for both the devices. Moreover, as the temperature rises above room temperature, the covalent bond inside the lattice of semiconductor body material begins to break, resulting in a larger number of electron-hole pairs (EHPs) generation. The rate of EHPs generation is directly propositional to the intrinsic carrier concentration of semiconductor (n_i) [29]. The n_i is exponentially related to temperature as per the expression

$$n_i = N_a exp\left(-\frac{E_g}{2KT}\right) \tag{1}$$

Here, N_a represents the impurity (acceptor/donor) carrier concentration, E_g represents bandgap, K represents the Boltzmann constant, and T is the temperature.

To understand the BTBT process the energy band variation of DMSGO-TFET and DMSGO-SDP-TFET are illustrated in Fig. 2c, d respectively. The energy bandgap of the semiconductor material decreases as temperature increases, influencing device characteristics accordingly. The energy bandgap variation with temperature can be obtained using the equation [30, 32]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{2}$$

Where $E_g(T)$ represents energy band gap at absolute temperature T, $E_g(0)$ is the energy bandgap at T= 0 K, and α, β represents material-specific fitting parameters. The ON-state energy band variation with temperature ranging from 300 to 450K for DMSGO-TFET and DMSGO-SDP-TFET are illustrated in Fig. 2c, d respectively. These results demonstrate that at room temperature, a significant decrease in tunneling barrier width (≈ 4 nm) is observed at the source junction for DMSGO-SDP-TFET, which increases the inter-band tunneling rate for DMSGO-SDP-TFET as compared to conventional DMSGO-TFET. Furthermore, the impact of temperature variation is noted as very small in both devices.

Fig. 2e, f illustrate the inter-band tunneling rate with temperature ranging from 300 to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. The above figures show that, with temperature variation, the inter-band tunneling rate increases in both the devices as shown in the inset. Furthermore, results demonstrate that the inclusion of a low k dielectric pocket exhibits a higher tunneling rate due to a decrease in tunneling width at the source-channel junction for DMSGO-SDP-TFET compared to conventional DMSGO-TFET.

Fig. 3a, b illustrate the effect of temperature variations on $I_{DS} - V_{GS}$ characteristics for conventional DMSGO-TFET and DMSGO-SDP-TFET, respectively. These figures show a smaller I_{ON} variation with temperature for both devices because I_{ON} depends mainly on the band-to-band tunneling instead of temperature. The temperature

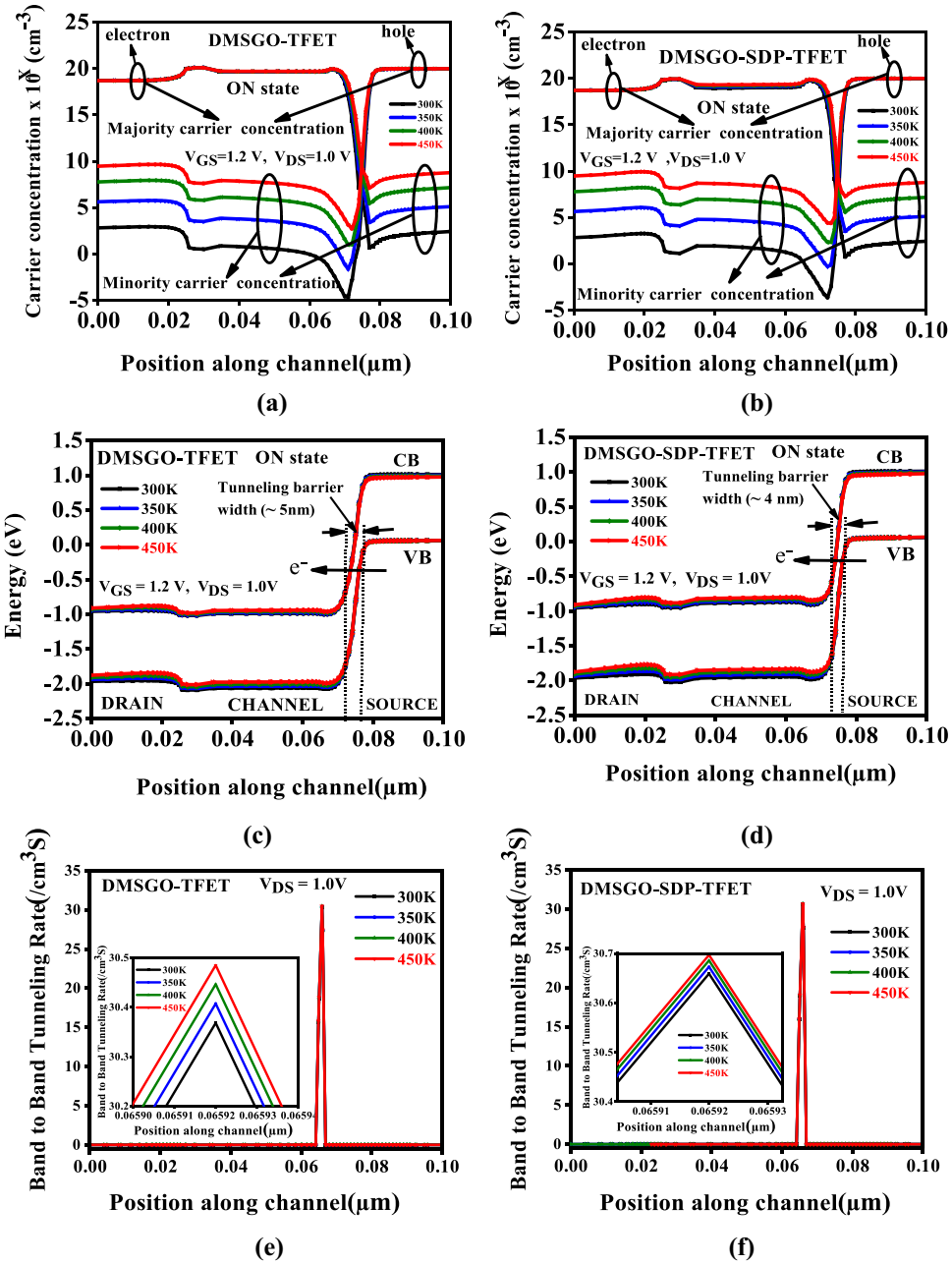

Fig. 2 Variation of carrier concentration with temperature for **a** DMSGO-TFET and **b** DMSGO-SDP-TFET, Variation of energy band with temperature for **c** DMSGO-TFET and **d** DMSGO-SDP-TFET, BTBT Variation with temperature for **e** DMSGO-TFET and **f** DMSGO-SDP-TFET

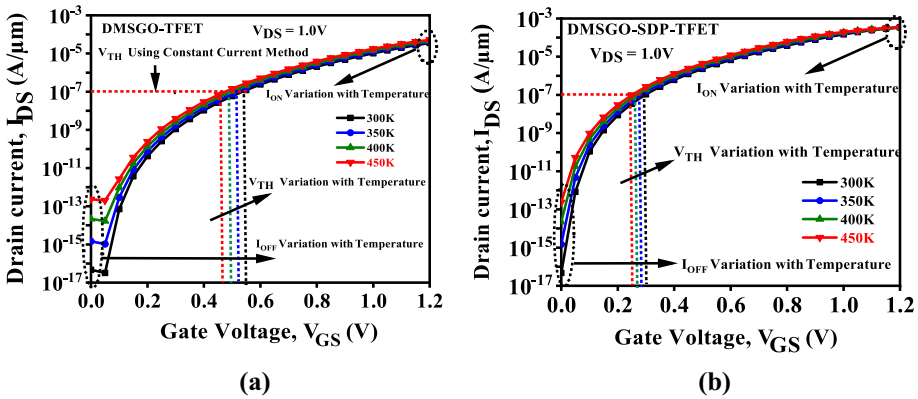

Fig. 3 Variation of $I_{DS} - V_{GS}$ characteristics with temperature for **a** conventional DMSGO-TFET, **b** DMSGO-SDP-TFET

variations have a significant impact on the OFF-state current (I_{OFF}) of the device because of its dependence on minority carrier concentration, which increases with temperature. It affects the reliability of the device for circuit-level applications because the switching (I_{ON}/I_{OFF}) ratio is highly influenced by temperature. A higher I_{ON}/I_{OFF} ratio results in faster switching. These results also demonstrate that the temperature dependence of DMSGO-SDP-TFET provides 0.23%/K change in I_{ON}. Whereas DMSGO-TFET provides 1.12%/K at $V_{GS} = 1.0$ V. Hence, the I_{ON} variation with temperature ranging from 300 to 450K is 0.89%/K lesser for the DMSGO-SDP-TFET as compared to conventional DMSGO-TFET. This indicates that DMSGO-SDP-TFET is more resistant to temperature compared to DMSGO-TFET. Furthermore, because of the dielectric pocket, DMSGO-SDP-TFET has a higher I_{ON} than DMSGO-TFET. From the $I_{DS} - V_{GS}$ characteristics shown in Fig. 3a, b various device parameters such as I_{ON}, I_{ON}/I_{OFF}, SS_{avg} and V_{TH} are extracted, presented in Tables 2 and 3.

The comparative threshold voltage (V_{TH}) variation with temperature using the constant current method for conventional DMSGO-TFET and DMSGO-SDP-TFET is shown in Fig. 4a. The results reveal that V_{TH} decreases for both devices as temperature increases. Moreover, DMSGO-SDP-TFET exhibits minimum V_{TH} because of reduced tunneling width, and the temperature dependency of DMSGO-SDP-TFET exhibits 0.095%/K change in V_{TH}, whereas it exhibits 0.069 %/K change for DMSGO-TFET. Hence, the V_{TH} variation with temperature ranging from 300 to 450K is 0.026 %/K higher for DMSGO-SDP-TFET compared to DMSGO-TFET. Hence, a substantial increase in drain current is observed at lower V_{GS} in the proposed DMSGO-SDP-TFET as shown in the transfer characteristics.

Fig. 4b illustrates the effect of temperature variation on the average subthreshold swing (SS_{AVG}) for conventional DMSGO-TFET and DMSGO-SDP-TFET. The SS_{AVG} is formulated using the expression [6].

$$SS_{AVG} = \frac{(V_{TH} - V_{OFF})}{log(I_{VTH}) - log(I_{OFF})} \quad (3)$$

The subthreshold swing is inversely proportional to the steepness of $I_{DS} - V_{GS}$ characteristics curve in the subthreshold region. Fig.4b shows that SS_{AVG} for both devices increases as the temperature rises due to an increase in OFF-state current. Moreover, temperature dependency of DMSGO-SDP-TFET provides 0.28%/K change in SS_{AVG}, whereas it exhibits 0.32%/K change for DMSGO-TFET. Hence, SS_{AVG} variation with temperature ranging from 300 to 450K is 0.04%/K lower for DMSGO-SDP-TFET due to narrow tunneling barrier width at the source-channel junction.

3.2 Temperature sensitivity analysis of analog/radio frequency performance

This section presents the temperature dependence of various analog/radio frequency performance parameters such as g_m, f_T, GBP, f_{max},TFP, τ for conventional DMSGO-TFET and the proposed DMSGO-SDP-TFET.

The parasitic capacitances (C_{gs} and C_{gd}) are crucial parameters to analyze the analog/radio frequency and linearity performance of the device. In this regard, Fig. 5a, b illustrate the C_{gs} variation with V_{GS} at the temperature range from 300 to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. A significant decrease in C_{gs} with increasing temperature in both the devices because the potential barrier at Source channel interface increases with temperature. Similarly, Fig. 5c, d illustrate the C_{gd} variation for both the devices, respectively. As the thermally generated charge carriers in the channel region increase the inversion layer. The potential barrier across the drain channel interface decreases as temperature increases. Hence, C_{gd} increases at higher gate bias in both the devices. Also, a similar trend is reported in [29]

Transconductance (g_m) is one of the most crucial parameters when evaluating a device for its analog/radio frequency

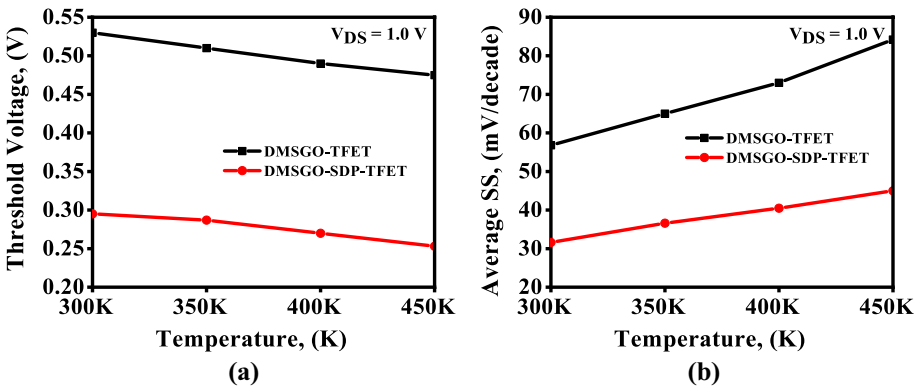

Fig. 4 **a** Comparative threshold voltage and **b** Average subthreshold swing variation with temperature for DMSGO-TFET and DMSGO-SDP-TFET

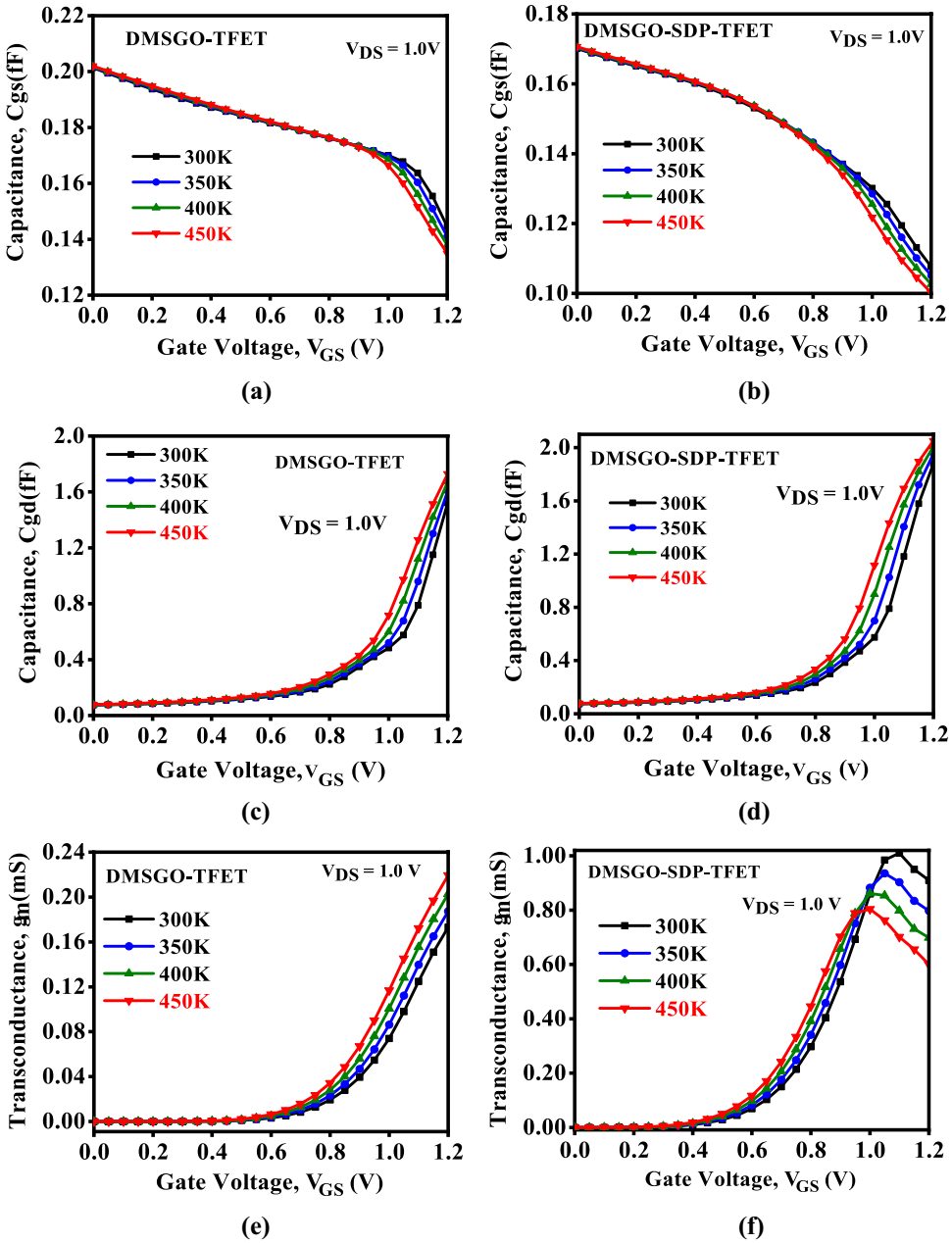

Fig. 5 C_{gs} variation with temperature for **a** DMSGO-TFET, **b** DMSGO-SDP-TFET. C_{gd} Variation with temperature for **c** DMSGO-TFET, **d** DMSGO-SDP-TFET. g_m Variation with temperature for **e** DMSGO-TFET,**f** DMSGO-SDP-TFET

and linearity performance. Therefore, higher g_m results in achieving higher gain, f_T and GBP in the design of analog circuits [31]. In this regard, Fig. 5e, f illustrate the g_m variation with temperature for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results in the subthreshold region g_m of both the devices are very small and it starts increasing due to a steep rise in the ON-state current. However, it starts decreasing after a particular value of V_{GS} because of mobility degradation [32]. The results also reveal that, with increasing temperature, a peak of g_m is shifted more towards lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve better analog/radio frequency performance as compared to DMSGO-TFET. Moreover, DMSGO-SDP-TFET exhibits 0.37%/K variation in g_m for temperature ranging from 300 to 450K at $V_{GS} = 0.75$ V, whereas for the same biasing conditions and temperature range DMSGO-TFET exhibits 0.55 %/K variation. Hence, g_m of DMSGO-SDP-TFET exhibits better immunity to temperature variations when compared to DMSGO-TFET. This indicates that the proposed device is appropriate for analog/radio frequency applications at higher temperatures.

Another critical parameter for evaluating the device's analog/radio frequency performance is the cutoff frequency (f_T). It is defined as the frequency at which current gain becomes 0 dB [28]. It is obtained using the expression

$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$. It can be noted that f_T depends on C_{gs}, C_{gd} and g_m of the device. Fig. 6a, b depict the variation in f_T with V_{GS} at temperatures ranging from 300 to 450K for DMSGO-TFET and DMSGO-SDP-TFET. As seen from Fig. 6a, b, f_T initially increases with V_{GS} due to an increase in g_m and then decreases after a certain value of V_{GS} due to the increased parasitic capacitances and reduced g_m because of mobility degradation. The results also reveal that, with increasing temperature, the peak of f_T is shifted more towards lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve better high-frequency performance as compared to DMSGO-TFET. Moreover, DMSGO-SDP-TFET exhibits 0.19%/K variation in f_T for temperature range from 300 to 450K at V_{GS} =0.75 V, whereas for the same biasing conditions and temperature range DMSGO-TFET exhibits 0.39 %/K variation. Hence, the proposed DMSGO-SDP-TFET exhibits better immunity and reliability to temperature variations for high-frequency applications at higher temperatures when compared to DMSGO-TFET.

The GBP is another important parameter for evaluating the analog/radio frequency performance of the device. It is formulated as $GBP = \frac{g_m}{20\pi C_{gd}}$. The GBP variations for DMSGO-TFET and DMSGO-SDP-TFET with V_{GS} at the temperature range from 300 to 450K, is shown in Fig. 7a, b respectively. The results reveal that GBP of conventional DMSGO-TFET is inferior to DMSGO-SDP-TFET for the same reasons discussed earlier for the f_T. Further, it is evident from the results as the temperature increases, GBP starts decreasing in both the devices due to mobility degradation. Also, the mobility degradation observed at lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve higher GBP as compared to DMSGO-TFET. Therefore, before the mobility degradation i.e, at V_{GS} =0.75 V and temperature range from 300 to 450K, in terms of %/K variation DMSGO-TFET exhibits 0.27 %/K variation in GBP and DMSGO-SDP-TFET exhibits 0.09%/K. Hence, the proposed DMSGO-SDP-TFET shows better immunity to temperature variations compared to DMSGO-TFET.

Another crucial parameter for the analog/radio frequency performance evaluation of the device is the maximum oscillating frequency (f_{max}). It is obtained as $f_{max} = \sqrt{\frac{f_T}{8\pi C_{gd} R_{gd}}}$. Fig. 7c, d illustrate the f_{max} variation with V_{GS} at temperature ranges from 300 to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results, due to higher f_T, f_{max} of DMSGO-SDP-TFET is greater than that of DMSGO-TFET. Furthermore, as temperature rises, f_{max} in both devices begins to fall due to a decrease in f_T caused by mobility degradation. Further, mobility degradation started at lower V_{GS} in DMSGO-SDP-TFET which means that a lower V_{GS} is needed to achieve higher f_{max} as compared to DMSGO-TFET. Therefore, before the mobility degradation i.e, at V_{GS} =0.75 V, and temperature range from 300 to 450K, in terms of %/K variation for f_{max}, DMSGO-TFET exhibits 0.104 %/K variation and DMSGO-SDP-TFET exhibits 0.075%/K. Hence, the proposed DMSGO-SDP-TFET shows better immunity to temperature variations and exhibits better analog/radio frequency performance at lower V_{GS} and elevated temperatures compared to DMSGO-TFET.

TFP is also an important parameter to consider for the high-frequency performance assessment of the device. It is formulated as $TFP = \left(\frac{g_m}{I_{DS}}\right) f_T$. Fig. 8a, b depict the TFP variation with temperature for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results, for both devices, TFP increases linearly up to a certain value of V_{GS} due to increased g_m. After reaching its peak value, it begins to fall due to a decrease in g_m and increased parasitic capacitance. The results also reveal that, as the temperature rises, the TFP of both devices falls due to a decrease in f_T and g_m because of mobility degradation. Moreover, the results also reveal that at V_{GS} = 0.75 V and temperature range 300 to 450*K*, in terms of %/K variation, DMSGO-TFET exhibits 0.32 %/K variation in TFP and the proposed DMSGO-SDP-TFET

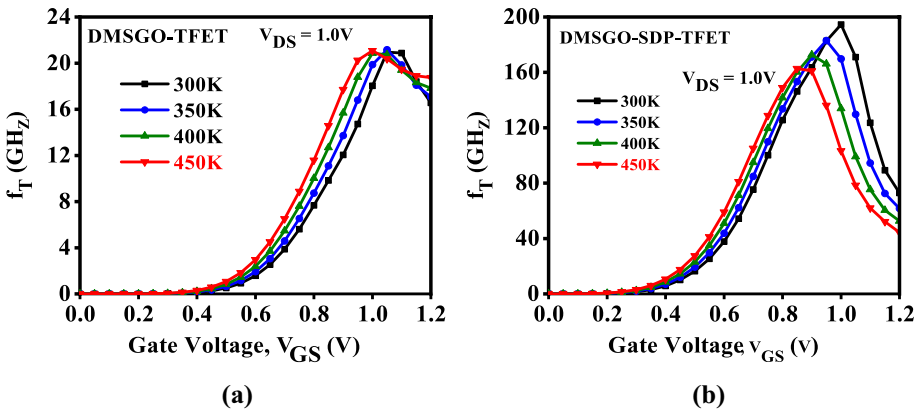

Fig. 6 variation of f_T with temperature for **a** conventional DMSGO-TFET, **b** DMSGO-SDP-TFET

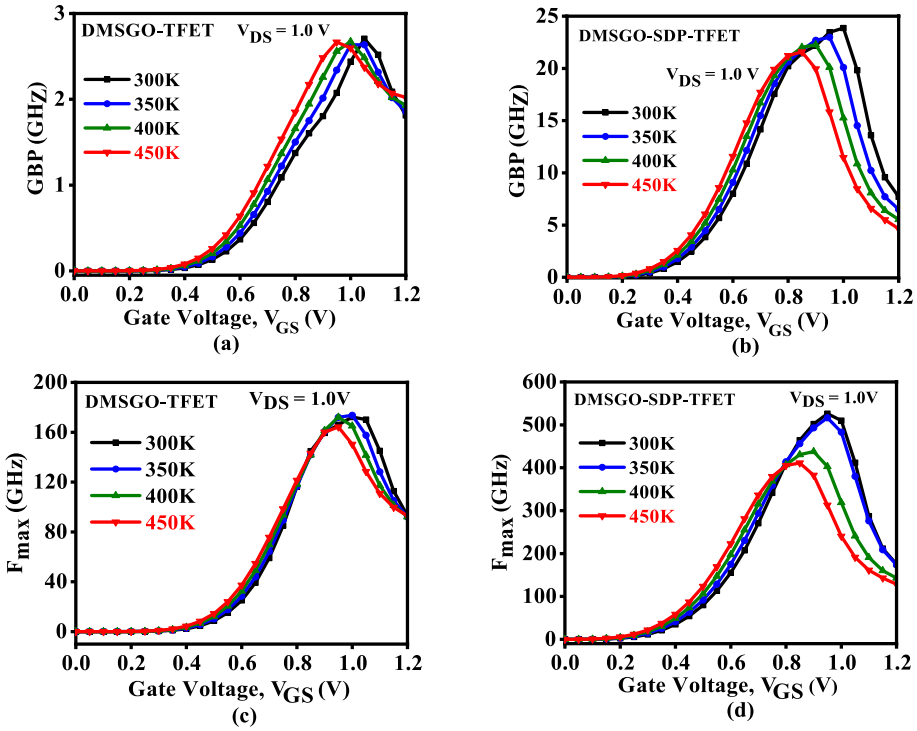

Fig. 7 Variation of GBP with temperature for **a** DMSGO-TFET, **b** DMSGO-SDP-TFET. Variation of f_{max} with temperature for **c** DMSGO-TFET, **d** DMSGO-SDP-TFET

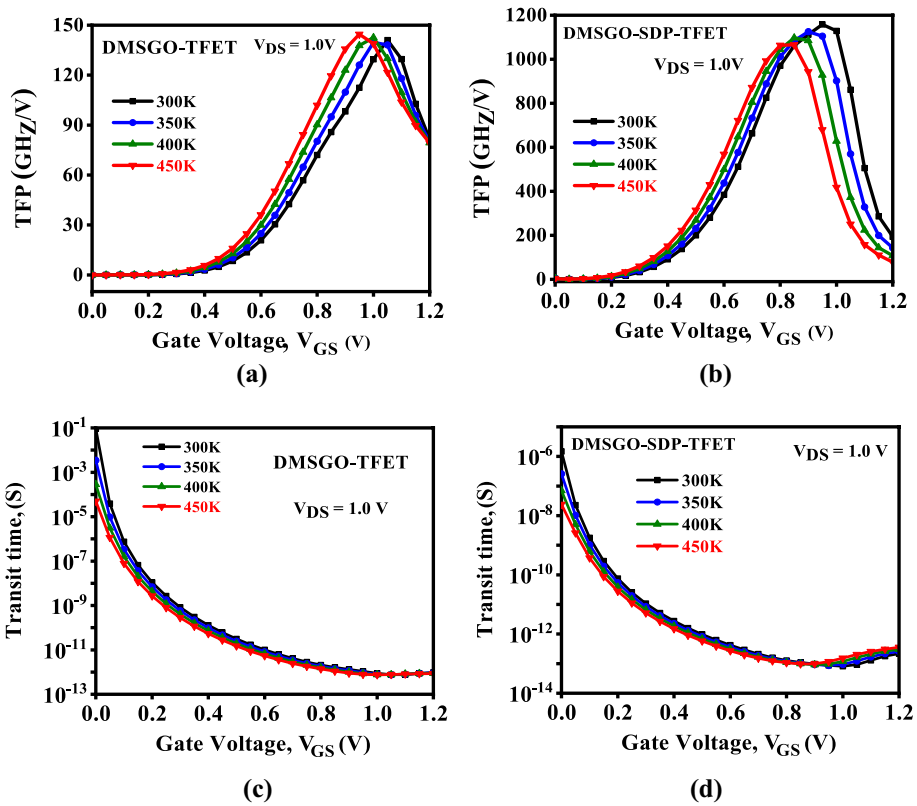

Fig. 8 TFP Variation with temperature for **a** DMSGO-TFET, **b** DMSGO-SDP-TFET. Transit time variation with temperature for **c** DMSGO-TFET, **d** DMSGO-SDP-TFET

exhibits 0.13%/K. Hence, the proposed DMSGO-SDP-TFET shows better immunity to temperature variations compared to conventional DMSGO-TFET.

The transit time (τ) is another important parameter for the radio frequency performance assessment of the device. It is defined as the time taken by the device to transfer the carriers from source to drain region [24]. It is formulated as $\tau = \frac{1}{2\pi 10 f_T}$. From the above expression, it is evident that transit time depends on f_T. Fig. 8c, d depict the transit time varies with temperature for DMSGO-TFET and DMSGO-SDP-TFET, respectively. From Fig. 8c, it can be seen that with increasing V_{GS}, τ decreases in both devices, whereas in the case of DMSGO-SDP-TFET shown in Fig. 8d after a certain V_{GS} transit time starts increasing due to decrease in f_T because of mobility degradation. Moreover, the results also reveal that the effect of temperature variations on conventional DMSGO-TFET is negligible, whereas DMSGO-SDP-TFET exhibit significant variation in transit time. Finally, the temperature sensitivity of different device parameters in % per kelvin for conventional DMSGO-TFET and the proposed DMSGO-SDP-TFET are presented in Table 2, and the performance of the proposed device is compared to recent literature in Table 3.

3.3 Temperature sensitivity analysis of linearity and distortion figure of merits

In this section, the impact of temperature variations on the linearity and distortion performance parameters for conventional DMSGO-TFET and the proposed DMSGO-SDP-TFET have been analyzed. In this regard, various linearity and distortion parameters such as g_{m3}, VIP3, IIP3, and IMD3 are considered for analysis. These parameters are defined as follows [31].

$$\mathrm{VIP3} = \sqrt{24 \times \left(\frac{g_{m1}}{g_{m3}}\right)} \tag{4}$$

$$\mathrm{IIP3} = \frac{2}{3} \times \left(\frac{g_{m1}}{g_{m3} \times R_S}\right) \tag{5}$$

$$\mathrm{IMD3} = \left[\frac{9}{2} \times (VIP3)^2 \times (g_{m3})\right]^2 \times R_S \tag{6}$$

Where R_S is assumed to be 50 Ω for most RF applications. To obtain better linearity and minimum distortion VIP3, IIP3 parameters of the device should be higher, and IMD3 parameter must be lower [26, 31]. Fig. 9a, b illustrate the impact of temperature variations ranging from 300 to 450K on higher-order transconductance (g_{m3}) for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the

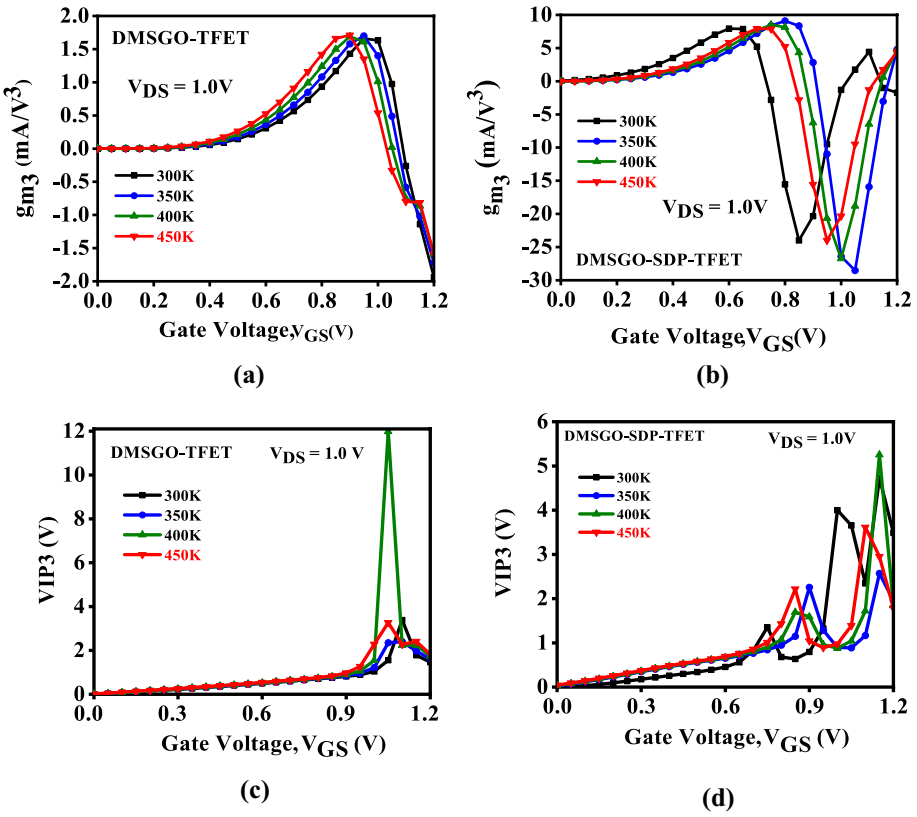

Fig. 9 Variation of g_{m3} with temperature for **a** DMSGO-TFET, **b** DMSGO-SDP-TFET. Variation of VIP3 with temperature for **c** DMSGO-TFET, **d** DMSGO-SDP-TFET

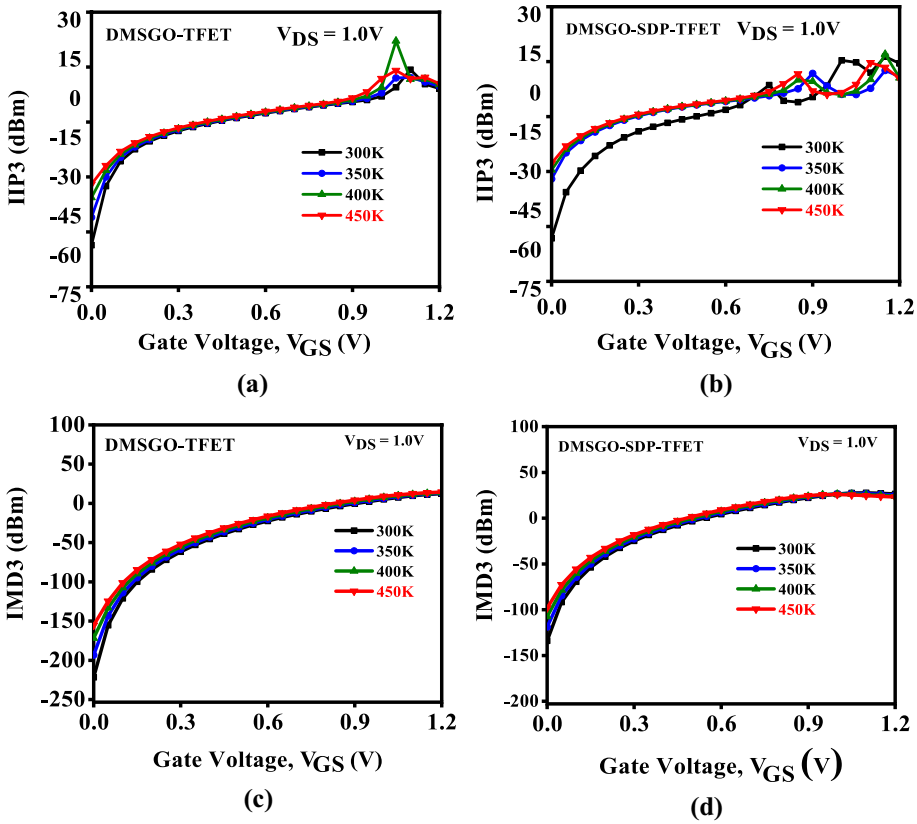

Fig. 10 Variation of IIP3 with temperature for **a** DMSGO-TFET, **b** DMSGO-SDP-TFET. IMD3 Variation with temperature for **c** DMSGO-TFET, **d** DMSGO-SDP-TFET

Table 2 Temperature sensitivity in % per kelvin for conventional DMSGO-TFET and DMSGO-SDP-TFET

Parameters	DMSGO-TFET	DMSGO-SDP-TFET
V_{TH}	0.069 %/K	0.095 %/K
SS_{AVG}	0.32 %/K	0.28 %/K
I_{ON}	1.12 %/K	0.23 %/K
g_m	0.55 %/K	0.37 %/K
f_T	0.39 %/K	0.19 %/K
GBP	0.27 %/K	0.09 %/K
f_{max}	0.104 %/K	0.075 %/K
TFP	0.32 %/K	0.13 %/K

above figures that g_{m3} variation is negligible at lower V_{GS} for both devices. Moreover, the results also reveal that DMSGO-SDP-TFET is more sensitive to temperature variations at higher gate voltage compared to DMSGO-TFET.

A device with a higher value of VIP3 shows better linearity [25, 31]. Here, Fig. 9c, d illustrate VIP3 variation with V_{GS} at a different temperature ranging from 300 to 450K for DMSGO-TFET and DMSGO-SDP-TFET, respectively. It is evident from the results VIP3 of the proposed DMSGO-SDP-TFET is higher and shows better linearity compared to DMSGO-TFET. Further, the results also reveal that both the devices are temperature sensitive for higher V_{GS}.

Table 3 Comparison of DC, analog/RF parameters with recent literature

Parameters	DMSGO-SDP-TFET	Ref [33]	Ref [34]	Ref [35]	Ref [23]	Ref [36]
I_{ON} (A/μm)	1.47×10^{-4}	2.06×10^{-5}	1.4×10^{-4}	1.24×10^{-5}	1.21×10^{-4}	1.85×10^{-5}
I_{OFF} (A/μm)	4.56×10^{-17}	2.76×10^{-17}	7.82×10^{-17}	5.15×10^{-18}	1.23×10^{-13}	1.26×10^{-16}
I_{ON}/I_{OFF}	3.14×10^{12}	7.5×10^{11}	1.79×10^{12}	2.42×10^{12}	9.83×10^{11}	1.46×10^{11}
V_{TH}(V)	0.29	0.31	0.54	0.41	0.41	0.7
SS_{avg}(mV/decade)	29.4	26	34.5	39.8	–	40.44
$g_m(s)$	1.02×10^{-3}	66×10^{-6}	2.61×10^{-4}	6.5×10^{-5}	2.9×10^{-4}	7.4×10^{-5}
f_T (GHz)	193	46	34	355	59.6	0.17
GBP (GHz)	23.6	7	3.9	36	9.97	0.16
TFP (GHz)	1158	550	–	–	–	500

The impact of temperature variations on the IIP3 for DMSGO-TFET and DMSGO-SDP-TFET are illustrated in Fig. 10a, b respectively. It is evident from the results that IIP3 of the proposed DMSGO-SDP-TFET is higher than DMSGO-TFET, this increase in the IIP3 parameter indicates improvement in the linearity performance of the device. Therefore, DMSGO-SDP-TFET shows better linearity compared to DMSGO-TFET. Further, the results also reveal that as the temperature increases from 300 to 450K, both the devices are temperature sensitive at lower and higher V_{GS}.

A lower IMD3 parameter indicates that the device can withstand higher distortions [31]. In this regard, Fig. 10c, d illustrate the IMD3 variation with temperature. Results demonstrate that DMSGO-SDP-TFET exhibits 0.10%/K variation in IMD3 with temperature ranging from 300 to 450K at $V_{GS} = 1.2$ V and $V_{DS} = 1.0$ V, whereas, for the same operating temperature and biasing conditions, DMSGO-TFET exhibits 0.41 %/K variation. Hence, DMSGO-SDP-TFET shows better intermodulation distortion performance and more reliable to temperature variations as compared to conventional DMSGO-TFET.

4 Conclusions

A comparative temperature sensitivity analysis of DC, analog/radio frequency, linearity, and distortion performance has been carried out for conventional DMSGO-TFET and the proposed DMGOSDG-TFET at the temperature ranging from 300 to 450K. Based on this study, it can be stated that for the same biasing conditions and temperature range, the DC, analog/radio frequency, and linearity performance parameters of the proposed DMSGO-SDP-TFET are less sensitive to the temperature variation compared to conventional DMSGO-TFET. Further, the results summarized in Table 2 in % variation per kelvin, and Table 3 performance comparison with recent literature indicate that DMSGO-SDP-TFET is more reliable when compared to DMSGO-TFET. Hence, it can be concluded that the proposed DMSGO-SDP-TFET is a better choice for low power switching and analog/radio frequency applications for elevated temperature range .

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Data availability All the data taken from another resource has been given the corresponding reference. The data, for which reference is not provided, is the original data.

Code availability The code has been implemented using technology computer-aided design (TCAD) tool.

Declarations

Conflict of interest No conflicts of interest.

Ethical standard The manuscript follows all the ethical standards, including plagiarism.

Consent to participate Yes.

Consent for publication Yes.

References

1. Young, K.K.: Short-channel effect in fully-depleted SOI MOSFETs. IEEE Trans. Electron Devices **36**(2), 399–402 (1989)
2. Bangsaruntip, S., Cohen, G.M., Majumdar, A., Sleight, J.W.: Universality of short-channel effects in undoped-body silicon nanowire MOSFETs. IEEE Trans. Electron Devices **31**(9), 903–905 (2010)
3. Choi, W.Y., Park, B., Lee, J.D., Liu, T.K.: Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett. **28**(8), 743–745 (2007)
4. Saurabh, S., Kumar, M.J.: Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. IEEE Trans. Electron Devices **58**(2), 404–410 (2010)
5. Pal, A., Sachid, A.B., Gossner, H., Rao, V.R.: Insights into the design and optimization of tunnel-FET devices and circuits. IEEE Trans. Electron Devices **58**(4), 1045–1053 (2011)
6. Boucart, K., Ionescu, A.M.: Double gate tunnel FET with high k gate dielectric. IEEE Trans. Electron Devices **54**(7), 1725–1733 (2007)
7. Ionescu, A.M., Riel, H.: Tunnel field-effect transistors as energy efficient electronic switches. Nature **479**(7373), 329–337 (2011)
8. Lee, M.J., Choi, W.Y.: Effects of device geometry on hetero-gate-dielectric tunneling field-effect transistors. IEEE Electron Device Lett. **33**(10), 1459–1461 (2012)
9. Jain, P., Prabhat, V., Ghosh, B.: Dual metal-double gate tunnel field-effect transistor with mono/hetero dielectric gate material. J. Comput. Electron. **14**(2), 537–542 (2015)
10. Kale, S., Kondekar, P.N.: Charge plasma-based source/drain engineered Schottky Barrier MOSFET: Ambipolar suppression and improvement of the RF performance. Superlattices Microstruct. **113**, 799–809 (2018)
11. Vijayvargiya, V., Vishvakarma, S.K.: Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance. IEEE Trans. Nanotechnol. **13**(5), 974–981 (2014)
12. Vivek Anand, I., Arun Samuel, T.S., Vimala, P.: Modeling and simulation of a dual-material asymmetric heterodielectric-gate TFET. J. Comput. Electron. **19**, 1450–1462 (2020). https://doi.org/10.1007/s10825-020-01563-w
13. Raad, B.R., Sharma, D., Nigam, K., Kondekar, P.: Group III-V ternary compound semiconductor materials for unipolar conduction in tunnel field-effect transistors. J. Comput. Electron. **16**(1), 24–29 (2017)
14. Kale, S., Kondekar, P.N.: Ferroelectric Schottky barrier tunnel FET with gate-drain underlap: Proposal and investigation. Superlattices Microstruct. **89**, 225–230 (2016)

15. Kondekar, P.N., Nigam, K., Pandey, S., Sharma, D.: Design and analysis of polarity controlled electrically doped tunnel FET with bandgap engineering for analog/RF applications. IEEE Trans. Electron Devices **64**(2), 412–418 (2017)
16. Loan, S.A., Rafat, M.: A high-performance inverted- C tunnel junction FET with source-channel overlap pockets. IEEE Trans. Electron Devices **65**(2), 763–768 (2018)
17. Kale, S., Kondekar, P.N.: Design and investigation of dielectric engineered dopant segregated Schottky Barrier MOSFET With NiSi source/drain. IEEE Trans. Electron Devices **64**(11), 4400–4407 (2017)
18. Rawat, G., Talukdar, J., Mummaneni, K.: A Novel Extended Source TFET with δp^+ - SiGe Layer. Silicon **12**, 2273–2281 (2020)
19. Kumar, S., Singh, S., Nigam, K., Tikkiwal, V.A.: Dual material dual-oxide dual-gate TFET for improvement in DC characteristics, analog/RF and linearity performance. Appl. Phys. A **125**(5), 3531–3538 (2019)
20. Joshi, T., Singh, Y., Singh, B.: Extended-source double-gate tunnel FET with improved DC and analog/RF performance. IEEE Trans. Electron Devices **67**(4), 1873–1879 (2020)
21. Nigam, K.: Low-K dielectric pocket and workfunction engineering for DC and analog/RF performance improvement in dual material stack gate oxide double gate TFET. Silicon **13**, 2347–2356 (2020)
22. Chandan, B.V., Gautami, M., Nigam, K., Sharma, D., Tikkiwal, V.A., Yadav, S., Kumar, S.: Impact of a metal-strip on a polarity-based electrically doped TFET for improvement of DC and analog/RF performance. J. Comput. Electron. **18**(1), 76–82 (2018)
23. Raad, B.R., Nigam, K., Sharma, D., Kondekar, P.: Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement. Electron. Lett. **52**(9), 770–772 (2016)
24. Nigam, K., Kondekar, P.N., Sharma, D.: Approach for ambipolar behavior suppression in tunnel FET by workfunction engineering. IET Micro Nano Lett. **11**(8), 460–464 (2016)
25. Nigam, K., Pandey, S., Kondekar, P., Sharma, D., Parte, P.K.: A barrier controlled charge plasma-based TFET with gate engineering for ambipolar suppression and RF/linearity performance improvement. IEEE Trans. Electron Devices **64**(6), 2751–2757 (2017)
26. Madan, J., Chaujar, R.: Temperature-associated reliability issues of heterogeneous gate dielectric gate all around Tunnel FET. IEEE Trans. Nanotechnol. **17**(1), 41–48 (2018)
27. Paras, N., Chauhan, S.S.: Temperature sensitivity analysis of vertical tunneling based dual metal Gate TFET on analog/RF FOMs. Appl. Phys. A **125**, 316 (2019)
28. Nigam, K., Pandey, S., Kondekar, P.N., Sharma, D., Parte, P.K.: Temperature sensitivity analysis of polarity controlled electrostatically doped tunnel field-effect transistor. Superlattices Microstruct. **97**, 598–605 (2016)
29. Singh, P., Yadav, D.S.: Impact of temperature on analog/RF, linearity and reliability performance metrics of tunnel FET with ultra-thin source region. Appl. Phys. A **127**, 1–15 (2020)
30. Kumar, S.: Temperature dependence of analogue/RF performance, linearity, and harmonic distortion for dual-material gate-oxide-stack double-gate TFET. IET Circuits Devices Syst. (2021). https://doi.org/10.1049/cds2.12049
31. Ghosh, P., Haldar, S., Gupta, R.S., Gupta, M.: An investigation of linearity performance and intermodulation distortion of GME CGT MOSFET for RFIC design. IEEE Trans. Electron Devices **59**(12), 3263–3268 (2012)
32. Varshni, Y.P.: Temperature dependence of the energy gap in semiconductors. Physica **34**(1), 149–154 (1967)
33. Tripathy, M.R., Singh, A.K., Baral, K., Singh, P.K., Jit, S.: III-V/Si staggered heterojunction-based source-pocket engineered vertical TFETs for low power applications. Superlattice Microstruct. **142**, 106494 (2020)
34. Shaikh, M.R.U., Loan, S.A.: drain-engineered TFET with fully suppressed ambipolarity for high-frequency application. IEEE Trans. Electron Devices **66**(4), 1628–1634 (2019)
35. Yadav, S., Sharma, D., Soni, D., Aslam, M.: Controlling ambipolarity with improved RF performance by drain/gate work function engineering and using high K dielectric material in electrically doped TFET: proposal and optimization. J. Comput. Electron. **16**, 721–731 (2017)
36. Chauhan, S.S.: Design of double gate vertical tunnel field-effect transistor using HDB and its performance estimation. Superlattice Microstruct. **117**, 1–8 (2018)