Journal of Computational Electronics (2022) 21:348–359
https://doi.org/10.1007/s10825-021-01828-y

Crosstalk noise analysis of coupled on-chip interconnects using a multiresolution time domain (MRTD) technique

Bhaskar Gugulothu[1] · **Rajendra Naik Bhukya**[1]

Received: 7 April 2021 / Accepted: 29 November 2021 / Published online: 7 February 2022

Abstract
In this paper, crosstalk noise analysis of coupled on-chip interconnects is presented. The multiresolution time domain (MRTD) method is used to analyze the crosstalk noise model. The crosstalk-induced propagation time delay and crosstalk peak voltage on the victim line of interconnects are determined. The results obtained for the proposed MRTD model are compared with the conventional finite difference time domain (FDTD) method and validated with HSPICE simulations at the 22-nm technology node. The results show that crosstalk induced a propagation delay which is dynamic in-phase and dynamic out-of-phase, and peak voltage timing and the peak voltage value of functional crosstalk in the copper interconnects have an average error of less than 0.53% when compared with HSPICE simulations. The results for the proposed model are very similar to those of HSPICE simulations. Electromagnetic interference and electromagnetic compatibility of on-chip interconnects can also be addressed using the proposed method.

Keywords Crosstalk · On-chip interconnects · Delay · FDTD · MRTD

1 Introduction

Advances in very large-scale integration (VLSI) technology offer gigascale integrated circuits in a system on a chip. The use of interconnects is particularly important in the integration of electronic devices. Because of these requirements, chip complexity and the number of sources of variations have increased, and tightly packed interconnects emit transient crosstalk at high operating frequencies [1, 2]. Accurate peak noise timing and peak crosstalk noise estimation in a driver-interconnect-load (DIL) system has long been a key architectural objective [3]. On the basis of lumped and distributed RC interconnects, various crosstalk and delay models have been proposed [4, 5]. Masoumi et al. [6] computed crosstalk noise effects in a capacitively coupled RC interconnect line using closed-form expressions. Ismail et al. [7] strengthened the model by integrating self-inductance effects and estimated the RLC line propagation delay. With the introduction of low-resistivity interconnect materials and fast operating switching frequencies, parasitic inductance has begun to play an important role in on-chip interconnect efficiency. To accurately estimate the output of on-chip interconnects, they must be viewed as scattered RLC lines or transmission lines [8].

For evaluation of crosstalk noise, previous models have interpreted the nonlinear complementary metal–oxide–semiconductor (CMOS) driver to be a simple linear resistor [9, 10], which appears to deviate from the effects. Approximately 50% of MOSFET operation is in the saturation region during the transient period and later in the linear (or) cutoff regions. Several methods with different analytical solutions have been proposed, including the finite difference time domain (FDTD) approach and SPICE [simulation program with an integrated circuit emphasis], the results of which have been documented in recent works for DIL systems [11]. In the current state of the art, several studies have investigated crosstalk results based on the algorithm of the traditional FDTD, as it offers high precision [12], and Vobulapuram et al. [13] applied the FDTD approach to a nonlinear CMOS driver using the alpha-power law and *n*th-power law models, respectively, and they studied the effects of crosstalk in Cu interconnects.

✉ Bhaskar Gugulothu
bhaskargugulothu@osmania.ac.in

Rajendra Naik Bhukya
rajendranaikb@osmania.ac.in

[1] Deptartment of ECE, UCE, Osmania University, Hyderabad, India

The FDTD approach is an important computational procedure used to solve problems of electromagnetic and partial differential equations. The FDTD method is numerically dispersive [14, 15] during the propagation along the discretization. As a result, there is a need for a novel method with advantageous numerical dispersion properties. Krumpholz and Katehi [16] proposed a multiresolution time domain (MRTD) approach with an additional advantage of numerical dispersion characteristics. Grivet-Talocia [17] proposed an MRTD model using the Haar scaling function as the basis function, and achieved the same precision as with the FDTD model. Fujii et al. [18] proposed a model using MRTD as a basis function based on the Daubechies scaling function as three and four vanishing moments, which was more precise than the FDTD system. For effective field computation, Massy and Ney [19] hybridized the Battle–Lemarié-based MRTD model and the FDTD model to take advantage of the characteristics of both models, including the low dispersion characteristics of the MRTD model and the faster computation of the FDTD model. Tong et al. [20, 21] proposed an MRTD model for transient analysis of two-conductor transmission lines which outperformed conventional FDTD in terms of numerical dispersion and accuracy when compared with SPICE. Rebelli et al. [22, 23] proposed an MRTD approach to evaluate the signal integrity of coupled copper interconnects driven by a linear resistive and nonlinear CMOS dependent on the Daubechies scaling function at four vanishing moments. Rebelli et al. [24] applied the MRTD approach to a nonlinear CMOS using the *n*th-power law model to evaluate crosstalk noise in mutually coupled multiwalled carbon nanotube (MWCNT) interconnects at 32-nm technology. In the current state of the art, the MRTD method has not been used to calculate crosstalk noise, and the delay of the CMOS driver is analyzed using a modified alpha-power law model for coupled on-chip interconnects.

In this paper, the crosstalk effects of on-chip interconnects are analyzed using a Daubechies scaling function-based MRTD technique and considering the nonlinear CMOS driver modeled using a modified alpha-power law model which includes a drain conductance parameter. The most effective time domain model is presented to analyze both functional and dynamic crosstalk issues of two mutually coupled on-chip interconnect lines at 22-nm technology. The results obtained by the present model are compared with those of the conventional FDTD model and validated using HSPICE simulations.

The remainder of the paper is organized as follows. The transmission line-based MRTD model is discussed in Sect. 2, and the MRTD model comparisons and evaluation are presented in Sect. 3. Finally, conclusions are given in Sect. 4.

2 MRTD model of on-chip interconnects

The model of two mutually coupled on-chip interconnects with driver and load is shown in Fig. 1. The parasitic capacitance of the CMOS is expressed by C_m, which represents the gate-to-drain coupled capacitance, and C_d, which represents the drain/source diffusion capacitance. R_1 and R_2 are the line resistance values, C_1 and C_2 are the line capacitance, L_1 and L_2 are the line inductance, and C_{L1} and C_{L2} are the load capacitance values of line 1and line 2, respectively. All these values are obtained per unit length (p.u.l.). Both capacitance and inductance are coupled to the interconnect lines. C_c and L_m are the p.u.l. coupling capacitance and mutual inductance of coupling interconnect lines, respectively. The position and time of the interconnect lines are denoted by x and t, respectively.

The MRTD model for two mutually coupled on-chip interconnects is built in this section using the basis function of Daubechies' scaling function with four vanishing moments (D_4).

2.1 Model formulations for two mutually coupled on-chip interconnect lines

The telegrapher's equations can be used to mathematically describe the coupled interconnects. The coupled on-chip interconnects are defined as in [24, 25] using the following equations.

$$\frac{\partial V(z,t)}{\partial z} + L\frac{\partial I(z,t)}{\partial t} = -I(z,t)R \tag{1}$$

$$\frac{\partial I(z,t)}{\partial z} + C\frac{\partial V(z,t)}{\partial t} = 0 \tag{2}$$

where x and t are the positions and time, respectively; R, L, and C are two-dimensional interconnect impedance that is measured using [25]. The current and voltage variables

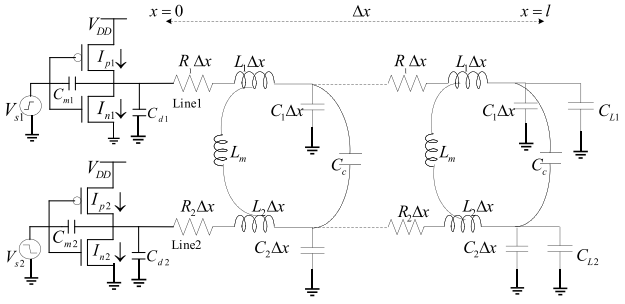

Fig. 1 CMOS drivers driving two-coupled on-chip interconnect lines, which are terminated by capacitive loads

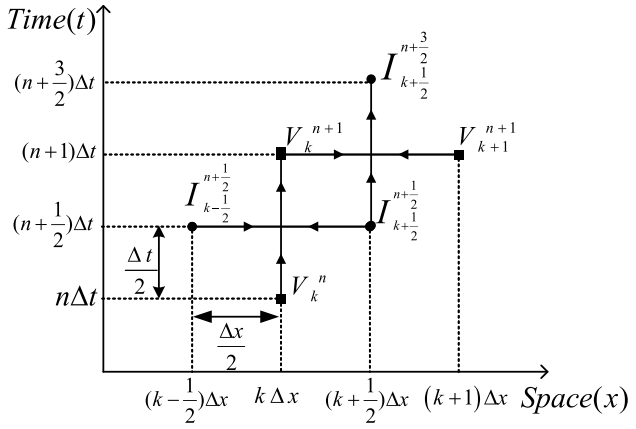

Fig. 2 Space and time discretization on an on-chip interconnect line

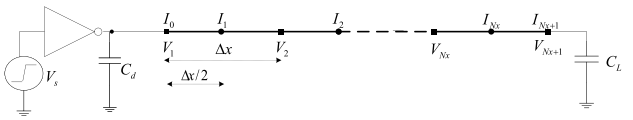

Fig. 3 Spatial discretization for I and V on an on-chip interconnect line

for a the coupled interconnect lines are $I = \left[I_1, I_2\right]^T$ and $V = \left[V_1, V_2\right]^T$.

$$R = diag\left[R_1, R_2\right]$$

$$L = \begin{bmatrix} L_1 & L_m \\ L_m & L_2 \end{bmatrix}$$

$$C = \begin{bmatrix} C_1 + C_c & -C_c \\ -C_c & C_2 + C_c \end{bmatrix} \tag{3}$$

where subscript 1 corresponds to line 1 and subscript 2 corresponds to line 2. The voltage and current evaluation points on interconnect line 1 are shown in Fig. 3.

Alternatively, current and voltage points are considered in time and space to evaluate telegrapher equations. The current and voltage are separated by $\frac{\Delta t}{2}$ in time and $\frac{\Delta x}{2}$ in space for better accuracy, as shown in Fig. 2, where Δt is time and Δx is space represented in discretization intervals.

The interconnect line l of length is the resistive driver at $x = 0$ and terminated at $x = l$ is capacitive load. The line is divided consistently into Nx segments of length $\Delta x = \frac{l}{Nx}$ indicating the discretization voltage (V) and current (I) nodes, which are unknown coefficients, as seen in Fig. 3, where the source current is represented by I_0.

The voltage and current terms can be extended using a known function ($h_n(t)$ and $\boldsymbol{\Phi}_k(x)$). In order to solve Eqs. (1) and (2), the unknown coefficients can be found by following the method defined in [16] as:

$$V(x,t) - \sum_{n,k=-\infty}^{+\infty} V_k^n \boldsymbol{\Phi}_k^n(x) h_n(t) = 0 \tag{4a}$$

$$I(x,t) - \sum_{n,k=-\infty}^{+\infty} I_{k+\frac{1}{2}}^{n+\frac{1}{2}} \boldsymbol{\Phi}_{k+\frac{1}{2}}^n(x) h_n(t) = 0 \tag{4b}$$

where $I_{k+\frac{1}{2}}^{n+\frac{1}{2}}$ is the coefficient of current expansion and V_n^k is the coefficient of voltage expansion in terms of function scaling, and the indices n and k are discrete time and space. Indices related to time and space are organized via $t = n\Delta t$ and $x = k\Delta x$. Functions $h_n(t)$ and $\boldsymbol{\Phi}_k(x)$ are defined as:

$$h_n(t) - h(\frac{t}{\Delta t} - n) = 0 \tag{5a}$$

where pulse function h(t) is defined as

$$h(t) = \begin{cases} 1 \;\; for|t\langle| < \frac{1}{2} \\ \frac{1}{2} \; for|t| = \frac{1}{2} \\ 0 \; for|t| > \frac{1}{2} \end{cases} \tag{5b}$$

$$\boldsymbol{\Phi}_k(x) = \boldsymbol{\Phi}(\frac{x}{\Delta x} - k) \tag{5c}$$

where $\boldsymbol{\Phi}(x)$ signifies the Daubechies scaling function, and h(t) represents the Haar scaling function.

The following integrals [26] are considered in order to derive the MRTD technique for Eqs. (1) and (2):

$$\int_{-\infty}^{+\infty} h_n(t) h_{n'}(t) dt = (\delta_{n,n'} \Delta t) \tag{6a}$$

$$\int_{-\infty}^{+\infty} h_n(t) \frac{\partial h_{n'+\frac{1}{2}}(t)}{\partial t} dt = (\delta_{n,n'} - \delta_{n,n'+1}) \tag{6b}$$

$$\int_{-\infty}^{+\infty} \boldsymbol{\Phi}_k(x) \boldsymbol{\Phi}_{k'}(x) dx = (\delta_{k,k'} \Delta x) \tag{6c}$$

$$\int_{-\infty}^{+\infty} \boldsymbol{\Phi}_k(x) \frac{\partial \boldsymbol{\Phi}_{k'+\frac{1}{2}}(t)}{\partial x} dx = \sum_{i=-L_s}^{L_s-1} b(i) \delta_{k+i,k'} \tag{6d}$$

where the Kronecker delta is represented by $\delta_{k,k'}$ and $\delta_{n,n'}$. The effective support sizes of the basis functions are indicated by L_s by considering the Daubechies scaling function as the basis function with four vanishing moments (D4). The coefficient b(i) is called the connection coefficient. Table 1 shows b(i) for $1 \le i \le L_s$, whereas b(i) for $i < 1$ can be found

Table 1 Connection coefficient b(i) for Daubechies' scaling function (D4) [18]

b(i)	b(i) for D4
1	1.3110340773
2	−0.1560100110
3	0.0419957460
4	−0.0086543236
5	0.0008308695
6	0.0000108999
7	0.0000000041

by symmetry condition b(−1−i) =−b(i) and equals zero for $i > L_s$

$$b(i) = \frac{1}{\Pi}\int_0^{\infty} \left|\hat{\Phi}(\lambda)\right|^2 \lambda sin\lambda(i+\frac{1}{2})d\lambda \tag{7}$$

where the scaling function of Fourier transform f(x) is $\hat{\Phi}(\lambda)$.

The following iterative calculations for current and voltage were carried out by employing the Galerkin technique [16] in Eqs. (1) and (2) and by using the test functions $\Phi_k h_{n+\frac{1}{2}}(t)$ and $\Phi_{k+\frac{1}{2}} h_n(t)$:

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = PI_{k+\frac{1}{2}}^{n+\frac{1}{2}} - \frac{\Delta t}{\Delta z} L^{-1} Q\left(\sum_{i=1}^{L_s} b(i)\left(V_{k+i}^n - V_{k-i+1}^n\right)\right) \tag{8a}$$

$$V_k^{n+1} = V_k^n - \frac{\Delta t}{\Delta z} C^{-1} \sum_{i=1}^{L_s} b(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{8b}$$

where

$$P = \left(1 + \frac{\Delta t}{2} RL^{-1}\right)^{-1}\left(1 - \frac{\Delta t}{2} RL^{-1}\right)$$

$$Q = \left(1 + \frac{\Delta t}{2} RL^{-1}\right)^{-1}$$

In the iterative Eqs. (8a) and (8b), the near-end voltage V_1^{n+1} and the far-end voltage V_{Nx+1}^{n+1} are obtained, and the iterative equations of the current and voltage near the boundary need to be modified. Near the boundary, the current is expressed by $I_{j+\frac{1}{2}}^{n+\frac{1}{2}}$ and $I_{Nx+1-i+\frac{1}{2}}^{n+\frac{1}{2}}$ for $i = 1, 2, 3, \cdots, L_s - 1$ and the voltage is V_i^{n+1} and V_{Nx-i+1}^{n+1} for $i = 2, 3, \cdots, L_s$ Many of these current and voltage values have a number of terms that surpass the index ranges in iterative Eqs. (8a) and (8b)

Equations (8a) and (8b) need to be decomposed using the relationship in [27] to update the iterative equations of current and voltage, which satisfies the connection coefficient b(i) given by

$$\sum_{i=1}^{L_s} (2i-1)b(i) = 1 \tag{9}$$

By substituting (9) into (8b), we get

$$\sum_{i=1}^{L_s} b(i)(2i-1)V_k^{n+1} = \sum_{i=1}^{L_s} b(i)(2j-1)V_k^n - \sum_{i=1}^{L_s} \frac{\Delta t}{(2i-1)\Delta x} C^{-1}\left((2i-1)b(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right) \tag{10}$$

We decompose (8b) considering a corresponding term with i as:

$$b(i)(2i-1)V_k^{n+1} = b(i)(2i-1)V_k^n - \frac{\Delta t}{(2i-1)\Delta x} C^{-1} \times \left((2i-1)b(i)\left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}}\right)\right) \tag{11}$$

for at $i = 1, 2, 3, \cdots, L_s - 1$.

Equation (11) is further adapted by employing the boundary conditions as proved in Sects. 2.3 and 2.4.

2.2 Modeling of CMOS driver

The equivalent electrical circuit model for two mutually coupled on-chip interconnect lines is shown in Fig. 2. The input voltage (Vs) is a two-dimensional vector with the formula $V_s = \left[V_{s1}, V_{s2}\right]^T$. The interconnect lines are driven by a CMOS driver [28] that follows a modified alpha-power law model. The velocity saturation effects and the finite drain conductance parameters are included.

$$I_n = \begin{cases} K_{sn}\left(V_s - V_{tn}\right)^{\alpha_n}\left(1 + \sigma_n V_1\right) \\ K_{ln}\left(V_s - V_{tn}\right)^{\frac{\alpha_n}{2}} V_1 \\ 0 \end{cases} \tag{12}$$

$$I_p = \begin{cases} K_{sp}\left(V_{DD} - V_s - \left|V_{tp}\right|\right)^{\alpha_p}\left(1 + \sigma_p\left(V_{DD} - V_1\right)\right) \\ K_{lp}\left(V_{DD} - V_{tp} - V_s\right)^{\frac{\alpha_p}{2}}\left(-V_1 + V_{DD}\right) \\ 0 \end{cases} \tag{13}$$

The latest equations for PMOS and NMOS are signified by $m \times 1$ vectors, i.e. $I_p = \left[I_{p1}, I_{p2}\right]^T$ and $In = \left[I_{n1}, I_{n2}\right]^T$. The linear region transconductance parameter, threshold voltage, saturation region transconductance parameter, drain conductance parameter and velocity saturation index of NMOS (PMOS) are $K_{ln}(K_{lp}), V_{tn}(V_{tp}), K_{sn}(K_{sp}), \sigma_n(\sigma_p)$, and $\alpha_n(\alpha_p)$, respectively. The NMOS/PMOS model parameter values for the 22-nm technology node as shown in Table 2 are used for this analysis.

2.3 Modeling at the near-end boundary condition

The DIL system is modeled under boundary conditions. The current and voltage node points are at the near-end terminals defined by I_0 and V_1 , respectively, where the nodal analysis of the terminal equation is given by

$$I_0 = C_m \frac{\mathrm{d}(V_s - V_1)}{\mathrm{d}x} - C_d \frac{\mathrm{d}V_1}{\mathrm{d}x} + I_p - I_n \tag{14}$$

Applying discretization and the Galerkin technique to (14), then

$$\begin{aligned} \Delta x I_0 = {} & \Delta x C_m \frac{1}{\Delta t}\left[\left(V_s^{n+1} - V_s^n\right) - \left(V_1^{n+1} - V_1^n\right)\right] \\ & - \Delta x C_d \left(V_1^{n+1} - V_1^n\right) + \Delta x I_p^{n+1} - \Delta x I_n^{n+1} \end{aligned} \tag{15a}$$

and

$$\begin{aligned} V_1^{n+1} = {} & V_1^n + \left(\frac{C_m + C_d}{\Delta t}\right)^{-1} \times \\ & \left[C_m \frac{1}{\Delta t}\left(V_s^{n+1} - V_s^n\right) + \left(I_p^{n+1} - I_n^{n+1} - I_0^{n+1}\right)\right] \end{aligned} \tag{15b}$$

The near-end terminal voltage is carried out at k=1 from (8b)

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta x} C^{-1} \sum_{i=1}^{L_s} b(i)\left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-i+\frac{3}{2}}^{n+\frac{1}{2}}\right) \tag{16}$$

By following the steps from Eqs. (9)–(11), Eq. (16) is decomposed as

$$b(1)V_1^{n+1} = b(1)V_1^n - b(1)\frac{\Delta t}{\Delta x} C^{-1}\left(I_{\frac{3}{2}}^{n+\frac{1}{2}} - I_{\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{17a}$$

$$3b(2)V_1^{n+1} = 3b(2)V_1^n - 3b(2)\frac{\Delta t}{3\Delta x} C^{-1}\left(I_{\frac{5}{2}}^{n+\frac{1}{2}} - I_{-\frac{1}{2}}^{n+\frac{1}{2}}\right) \tag{17b}$$

$$\vdots$$

$$\begin{aligned} b(L_s)(2L_s - 1)V_1^{n+1} = {} & b(L_s)(2L_s - 1)V_1^n \\ & - (2L_s - 1)b(L_s)\frac{\Delta t}{(2L_s - 1))\Delta x} C^{-1}\left(I_{L_s+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-L_s+\frac{3}{2}}^{n+\frac{1}{2}}\right) \end{aligned} \tag{17c}$$

Iterative Eqs. (17a)–(17c) are considered computer-aided design (CAD), i.e., central difference equations. In the particular calculations, the subscript to the terms $I_{-\frac{1}{2}}^{n+\frac{1}{2}}, I_{-\frac{3}{2}}^{n+\frac{1}{2}}, \cdots, I_{-L_s+\frac{3}{2}}^{n+\frac{1}{2}}$ has surpassed the index range. To solve this, we substitute the central difference scheme by using the forward difference scheme. By leaving the weight coefficient in each equation unchanged, iterative equations can also be obtained.

$$b(1)V_1^{n+1} = b(1)V_1^n - b(1)\frac{\Delta t}{\Delta x} C^{-1}\left(I_{\frac{3}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \tag{18a}$$

$$3b(2)V_1^{n+1} = 3b(2)V_1^n - b(2)\frac{\Delta t}{3\Delta x} C^{-1} 3\left(I_{\frac{5}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \tag{18b}$$

$$\vdots$$

$$\begin{aligned} & b(L_s)(2L_s - 1)V_1^{n+1} = b(L_s)(2L_s - 1)V_1^n \\ & - \frac{\Delta t}{(2L_s - 1))\Delta x} C^{-1}(2L_s - 1)b(L_s)\left(I_{L_s+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \end{aligned} \tag{18c}$$

From the above iterative Eqs. (18a)–(87c), at the near-end boundary node a voltage of V_1^{n+1} is obtained through the following:

$$V_1^{n+1} = V_1^n - \frac{\Delta t}{\Delta x} C^{-1} \sum_{i=1}^{L_s} 2b(i)\left(I_{i+\frac{1}{2}}^{n+\frac{1}{2}} - I_0^{n+\frac{1}{2}}\right) \tag{19}$$

In Eq. (19), substituting by $I_0^{n+\frac{1}{2}} = \frac{I_0^n + I_0^{n+1}}{2}$ and Eq. (15a) we obtain the equation

$$\begin{aligned} V_1^{n+1} = {} & V_1^n - AB \sum_{i=1}^{L_s} 2b(i) I_{i+\frac{1}{2}}^{n+\frac{1}{2}} \\ & - AB \sum_{i=1}^{L_s} b(i)\left(I_0^{n+1} + I_p^{n+1} - I_n^{n+1} + C_m\left(\frac{V_s^{n+1} - V_s^n}{\Delta t}\right)\right), \end{aligned} \tag{20}$$

where

$$A = \left(1 + (C_m + C_d)\frac{C^{-1}}{\Delta x}\sum_{i=1}^{L_s} b(i)\right)^{-1}, \; B = \frac{\Delta t}{\Delta x} C^{-1}$$

Table 2 Model parameters of 22 nm [28]

Parameter	PMOS	NMOS
$K_l(mho)$	0.005	0.009
$K_s(mho)$	1.3×10^3	1.5×10^3
$\sigma(V^{-1})$	3.43	1.25
$V_t(V)$	0.35	0.32
α	1.065	0.977

2.4 Modeling at the far-end boundary condition

Similarly, the nodal analysis equation at load current I_{Nx+1} given by the far-end terminal ($k = N_x + 1$)is:

$$I_{Nx+1} = C_L \frac{\mathrm{d}V_{Nx+1}}{\mathrm{d}t} \tag{21}$$

Then the final iterative equation given at the far end of the terminal is

$$V_{Nx+1}^{n+1} = V_{Nx+1}^{n} - EF \left(\sum_{i=1}^{L_s} b(i) I_{Nx+1}^{n+\frac{1}{2}} - \sum_{i=1}^{L_s} 2b(i) I_{Nx+1-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{22}$$

where $E = \left(1 + \frac{C_L}{\Delta t} C^{-1} \sum_{i=1}^{L_s} a(i)\right)$

$F = \frac{\Delta t}{\Delta x} C^{-1}$

where some of the term indices surpass the index ranges for all the nodes between the terminals in the algorithm extension to obtain and update the iterative equations, so a truncation method is applied by taking V_k^{n+1} as an example for $k = 2, 3, \cdots, L_s$, and by subsequent steps of Eqs. (10) and (11) it can be decomposed (8b) as an example for $k = 2, 3, \cdots, L_s$

$$b(1)V_k^{n+1} = b(1)V_k^n - b(1)\frac{\Delta t}{\Delta x} C^{-1} \left(I_{k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{23a}$$

$$3b(2)V_k^{n+1} = 3b(2)V_k^n - 3b(2)\frac{\Delta t}{3\Delta x} C^{-1} \left(I_{k+\frac{3}{2}}^{n+\frac{1}{2}} - I_{K-\frac{3}{2}}^{n+\frac{1}{2}} \right) \tag{23b}$$

$$\vdots$$

$$b(k-1)(2k-3)V_k^{n+1} = b(k-1)(2k-3)V_k^n - b(k-1)(2k-3)\frac{\Delta t}{(2k-3))\Delta x} C^{-1} \left(I_{2k-\frac{3}{2}}^{n+\frac{1}{2}} - I_{1+\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{23c}$$

$$b(k)(2k-1)V_k^{n+1} = b(k)(2k-1)V_k^n - b(k)(2k-1)\frac{\Delta t}{\Delta x(2k-1))} C^{-1} \left(I_{2k-\frac{1}{2}}^{n+\frac{1}{2}} - I_{\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{23d}$$

$$b(k+1)(2k+1)V_k^{n+1} = b(k+1)(2k+1)V_k^n - (2k+1)b(k+1)\frac{\Delta t}{(2k+1))\Delta x} C^{-1} \left(I_{2k+\frac{1}{2}}^{n+\frac{1}{2}} - I_{-\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{23e}$$

$$\vdots$$

$$b(L_s)(2L_s-1)V_k^{n+1} = b(L_s)(2L_s-1)V_k^n - b(L_s)\times (2L_s-1)\frac{\Delta t}{(2L_s-1))\Delta x} C^{-1} \left(I_{k+L_s-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-L_s+\frac{1}{2}}^{n+\frac{1}{2}} \right) \tag{23f}$$

From Eqs. (23a)–(23f) stated above, it is also observed that the indices of the equation do not surpass the index ranges for the first k terms. In addition, all calculations for which the index terms surpass the index spectrum appear in the remaining $L_s - k$ term. As $L_s - k$ terms are out of bound, these equations are not available for iterative equations in the MRTD model. To prevent this problem, a truncation is built into the calculations where the index range is surpassed.

The first k terms can be found by summing Eqs. (23a)–(23f), and the iterative equations can be updated at $k = 2, 3, \cdots, L_s$

$$V_k^{n+1} = V_k^n - Q\left(\sum_{i=1}^{k} (2i-1)b(i) \right)^{-1} \left(\sum_{i=1}^{k} b(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right) \tag{24}$$

Using the same steps illustrated in Eqs. (23a)–(23f), an altered iterative equation of voltage at interior points, as presented in Eq. (25), and voltage near the load, as presented in Eq. (26), become $k = L_s + 1, L_s + 2, \cdots, Nx - L_s, Nx - L_s + 1$

$$V_k^{n+1} = V_k^n - Q\left(\sum_{i=1}^{L_s} b(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right) \tag{25}$$

for $k = Nx - L_s + 2, Nx - L_s + 3, \cdots, N_x$.

$$V_k^{n+1} = V_k^n - Q\left(\sum_{i=1}^{Nx-k+1} b(i)(2i-1) \right)^{-1} \times \left(\sum_{i=1}^{Nx-k+1} b(i) \left(I_{k+i-\frac{1}{2}}^{n+\frac{1}{2}} - I_{k-i+\frac{1}{2}}^{n+\frac{1}{2}} \right) \right) \tag{26}$$

Current iterative equations can also be modified by the same voltage iterative equations with minor modifications. As seen in Fig. 3, at the half-integer points, the current nodes appear, implying that all the current is located at the interior points of the terminals. Therefore, the current near the terminals needs alteration. For iterative current equations near the terminals, it is necessary to decompose (8a) using the steps of iterative voltage of the equations. The final updated iterative current equations are given as

for k =1, near at the source

$$I_{1+\frac{1}{2}}^{n+\frac{3}{2}} = PI_{1+\frac{1}{2}}^{n+\frac{1}{2}} - \frac{\Delta t}{\Delta x} L^{-1} Q \left(\sum_{i=1}^{L_s} b(i)\left(V_{i+1}^{n+1} - V_1^{n+1}\right) \right) \tag{27}$$

for k=2, 3, ...⋯, L_s

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = PI_{k+\frac{1}{2}}^{n+\frac{1}{2}} - Q\left(\sum_{i=1}^{k} b(i)(2i-1) \right)^{-1} \times \frac{\Delta t}{\Delta x} L^{-1} \left(\sum_{i=1}^{k} b(i)\left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1}\right) \right) \tag{28}$$

for $k = L_s + 1, L_s + 2, \cdots, Nx - L_s, Nx - L_s + 1$. at the interior point iterative equations

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = PI_{k+\frac{1}{2}}^{n+\frac{1}{2}} - QL^{-1} \times \frac{\Delta t}{\Delta x} \left(\sum_{i=1}^{L_s} b(i)\left(V_{i+k}^{n+1} - V_{k-i+1}^{n+1}\right) \right) \tag{29}$$

for $k = Nx - L_s + 2, Nx - L_s + 3, \cdots, Nx$ Near the load, iterative equations are

$$I_{k+\frac{1}{2}}^{n+\frac{3}{2}} = PI_{k+\frac{1}{2}}^{n+\frac{1}{2}} - Q\frac{\Delta t}{\Delta x} L^{-1} \times \left(\sum_{i=1}^{Nx-k+1} b(i)(2i-1) \right)^{-1} \times \left(\sum_{i=1}^{Nx-k+1} b(i)\left(V_{k+i}^{n+1} - V_{k-i+1}^{n+1}\right) \right) \tag{30}$$

In the context of this bootstrapping method, modified voltage and current iterative equations are tested. Firstly, in terms of historical voltage and current values, voltage iterative equations are solved at a rigid time using Eqs. (20), (22), (24)–(26). Then, Eqs. (27)–(30) solve the iterative equations of current in terms of voltage measured initially and past values of current. The Courant stability condition [20, 27] is thus known as the stable output for MRTD iterative equations.

$$\Delta t \le \frac{q\Delta x}{\vartheta} \tag{31}$$

which states that for each cell, the time of propagation must be higher than the time step, where q is the current number given by $q = 1/\sum_{i=1}^{L_s} |b(i)| = \vartheta \Delta t/\Delta x$ and ϑ, and v is the phase velocity of the line propagation. However, the boundary conditions will always satisfy the stability requirement, as these are explicitly derived from an implicit expression.

3 MRTD model validation and benchmark

The performance analyses of the structure of the two mutually coupled on-chip interconnect lines are presented in this section. The proposed model is validated in comparison to the conventional FDTD model and HSPICE simulations. The numerical computations are carried out using MATLAB. The interconnect load is driven by a CMOS driver; the interconnect dimensions are taken from the International Technology Roadmap for Semiconductors (ITRS) [29, 30]. At the 22-nm technology node, the interconnect is placed 99 nm from a ground plane. The thickness of the line is 66 nm. The width and space between the lines are equal, at 33 nm. The inter-level dielectric medium permittivity is 2.3. The length and load capacitance of the interconnects are 1 mm and 2 fF. The Vdd voltage is 0.8 V. The signal voltage swings from 0 to 0.8 V (low→high) or 0.8 to 0 V (high→low). The input source voltages have a transition time of 20 ps. The parasitic values of RLC for the coupled interconnect line structure are

$$R = \begin{bmatrix} 10.10 & 0 \\ 0 & 10.10 \end{bmatrix}_{2\times2} \frac{M\Omega}{m},\ L = \begin{bmatrix} 2.082 & 1.86 \\ 1.86 & 2.082 \end{bmatrix}_{2\times2} \frac{uH}{m}$$

$$C = \begin{bmatrix} 90.75 & -75.16 \\ -75.16 & 90.75 \end{bmatrix}_{2\times2} \frac{pF}{m}$$

3.1 Transient and crosstalk analysis in two mutually coupled on-chip interconnects

This section covers the transient and crosstalk analysis of the -coupled on-chip interconnect system. Line 1 is the aggressor and line 2 is the victim line, as shown in Fig. 1. On the other side of the victim line, the crosstalk effects for functional, dynamic in-phase, and dynamic out-of-phase switching are found using the proposed model, the conventional FDTD model and HSPICE simulations [31]. The transient response is investigated on the victim line. The effect of functional crosstalk is explored by modifying line 1 (aggressor) input from 0.8 V to 0 V while holding line 2 (victim) in quiescent mode. When both aggressor and victim

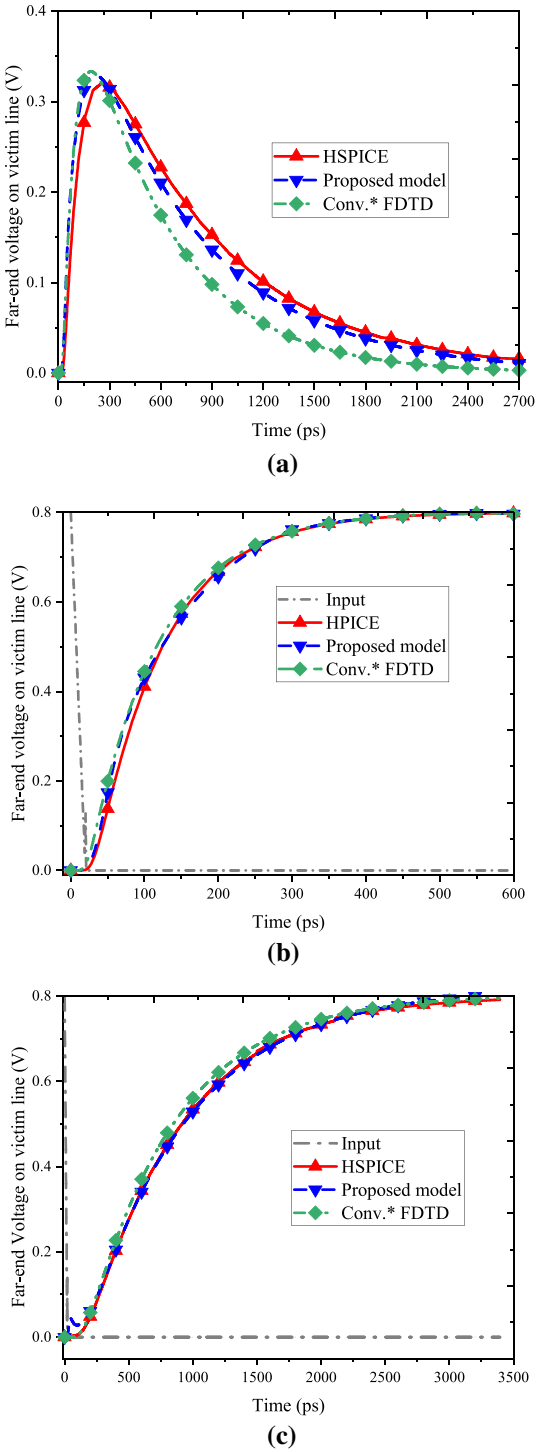

Fig. 4 Transient response comparison at the far-end voltage on victim line for (**a**) functional, (**b**) in-phase, and (**c**) out-of-phase switching

line stimuli turn at the same time, the impact of in-phase or out-of-phase is also explored. At the far end of the victim line, the transient graph results based on the above conditions are compared. The functional, dynamic in-phase, and dynamic out-of-phase transient responses on the victim line

Table 3 Victim line's computational error for peak voltage timings in functional crosstalk

Input transition time (ps)	Peak voltage timing (ps)				
	HSPICE	Proposed model	Conventional FDTD	%error proposed model	%error Conventional FDTD
10	254.55	253	251	0.60	1.39
20	274.08	274	273	0.03	0.39
30	279.22	279	277	0.07	0.79
40	287.39	287	286	0.13	0.48
50	297.55	297	295	0.18	0.85
60	311.49	310	308	0.47	1.12
70	318.37	315	314	1.05	1.37
80	328.14	326	324	0.65	1.26
90	339.88	338	337	0.55	0.84
100	343.72	342	341	0.50	0.79

are shown in Fig. 4a–c, respectively. Figure 4b and c demonstrate that the victim line peak solution has higher dispersion errors in the conventional FDTD method. The proposed model is superior to the conventional FDTD model in terms of precision due to its significant superiority in numerical dispersion properties. Figure 4c illustrates how the Miller effect increases the capacity, which allows signal transitions to take longer during out-of-phase than in-phase switching. The results of the proposed MRTD model correctly matched with HSPICE in all input switching situations and outperform the conventional FDTD method.

Table 3 shows the computational error associated with the estimation of functional crosstalk effects over the victim line for conventional FDTD and the proposed MRTD model in comparison to HSPICE. The efficiency of the proposed model at multiple input transition times shows an average error for crosstalk peak voltage timing of 0.42% versus 0.92% for the conventional FDTD method when compared with HSPICE. Table 4 also indicates that the proposed model correctly predicts the peak voltage, with an average error of 0.27% versus 1.05% using the conventional FDTD method when compared with HSPICE.

The computational error associated with estimating dynamic in-phase crosstalk effects over the victim line for the conventional FDTD and proposed MRTD models is shown in Table 5. The sturdiness of input transitions of the proposed model at different times has an average error of 0.53% versus 1.4% average error in the conventional FDTD method for propagation delay estimation when compared to HSPICE.

Table 6 shows the computational error associated with the estimation of dynamic out-of-phase crosstalk effects over the victim line for the conventional FDTD and proposed MRTD

Table 4 Victim line's computational error for peak voltage values in functional crosstalk

Input transition time (ps)	Peak voltage value (V)				
	HSPICE	Proposed model	Conventional FDTD	%error proposed model	%error Conventional FDTD
10	0.31998	0.3190	0.3230	0.30	−0.94
20	0.31901	0.3189	0.3228	0.03	−1.18
30	0.3190	0.3187	0.3226	0.09	−1.12
40	0.3188	0.3184	0.3222	0.12	−1.06
50	0.31792	0.3116	0.3208	1.98	−0.90
60	0.31746	0.3174	0.3203	0.02	−0.89
70	0.31652	0.3176	0.3201	−0.34	−1.13
80	0.31635	0.3171	0.3196	−0.23	−1.02
90	0.31588	0.3156	0.3185	0.08	−0.82
100	0.31493	0.3127	0.3195	0.70	−1.45

Table 5 Computational error for dynamic in-phase switching propagation delay for various transition times

Input transition time (ps)	In-phase propagation delay (ps)				
	HSPICE	Proposed model	Conventional FDTD	%error proposed model	%error Conventional FDTD
10	91.906	91	90	0.98	2.07
20	97.72	97	96	0.73	1.76
30	103.18	103	102	0.17	1.14
40	108.7	107	106	1.56	2.48
50	114.12	114	113	0.10	0.98
60	119.51	119	118	0.42	1.26
70	124.7	124	123	0.56	1.36
80	130.13	130	129	0.09	0.86
90	136.79	136	135	0.57	1.30
100	141.21	141	140	0.14	0.85

Table 6 Computational error for dynamic out-of-phase switching propagation delay for various transition times

Input transition time (ps)	Out-of-phase propagation delay (ps)				
	HSPICE	Proposed model	Conventional FDTD	%error proposed model	%error Conventional FDTD
10	697.86	696	695	0.26	0.40
20	702.5	700	699	0.35	0.49
30	707.72	706	704	0.24	0.52
40	713.21	712	710	0.16	0.45
50	719.28	718	717	0.17	0.31
60	725.46	725	724	0.06	0.20
70	729.19	728	726	0.16	0.43
80	737.5	736	735	0.20	0.33
90	740.37	740	738	0.04	0.32
100	746.29	745	743	0.172	0.44

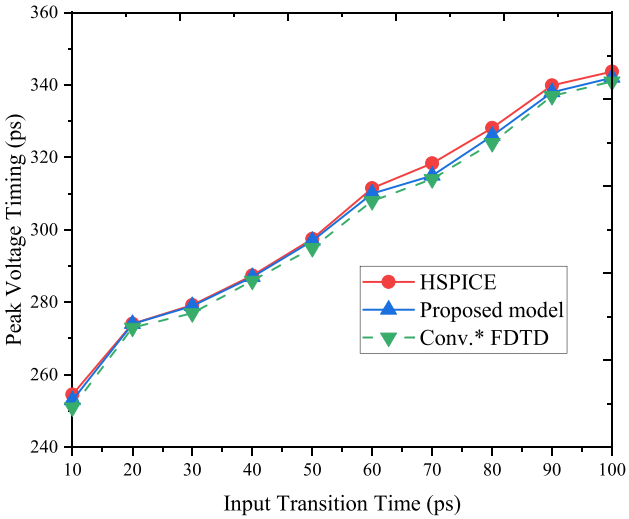

Fig. 5 Peak voltage timing with varied input transition time for the victim line

models. The sturdiness of input transitions at different times for the proposed model has an average error of 0.18% versus 0.38% average error in the conventional FDTD method for propagation delay estimation when compared with HSPICE. The simulation results for the proposed MRTD model match HSPICE correctly in all input switching situations and outperform the conventional FDTD model.

The graphs for peak voltage timing and peak voltage value on the victim line results in functional crosstalk generated by varying input transition time, which is shown in Figs. 5 and 6, respectively. Figures 7 and 8 illustrate the dynamic in-phase and out-of-phase crosstalk propagation delays at different input transition times. The results for both functional and dynamic crosstalk of the MRTD model are validated with HSPICE, and the proposed model outperforms the conventional FDTD model.

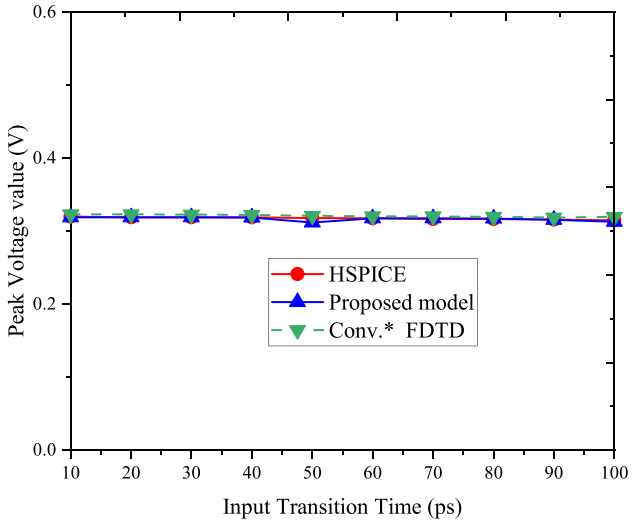

Fig. 6 Peak voltage with varied input transition time for the victim line

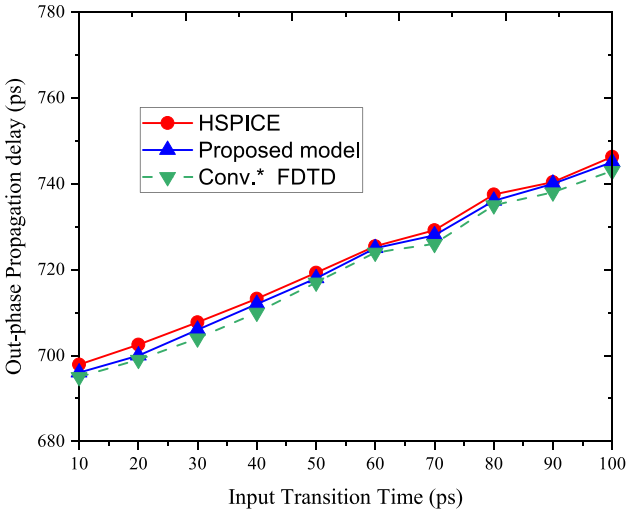

Fig. 8 Dynamic out-of-phase 50% propagation delay with varied input transition time for the victim line

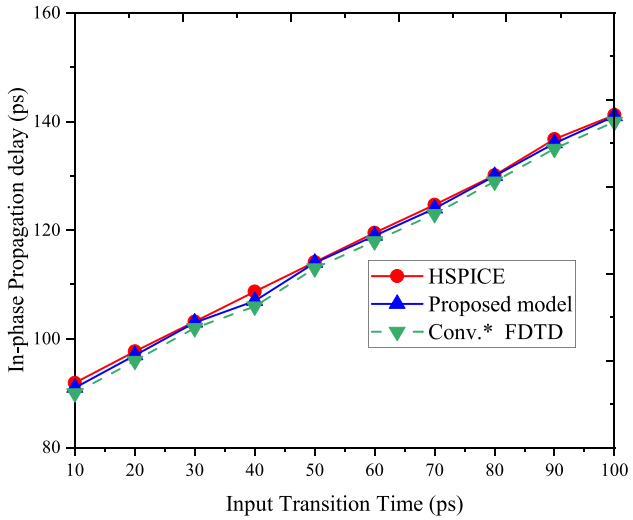

Fig. 7 Dynamic in-phase 50% propagation delay with varied input transition time for the victim line

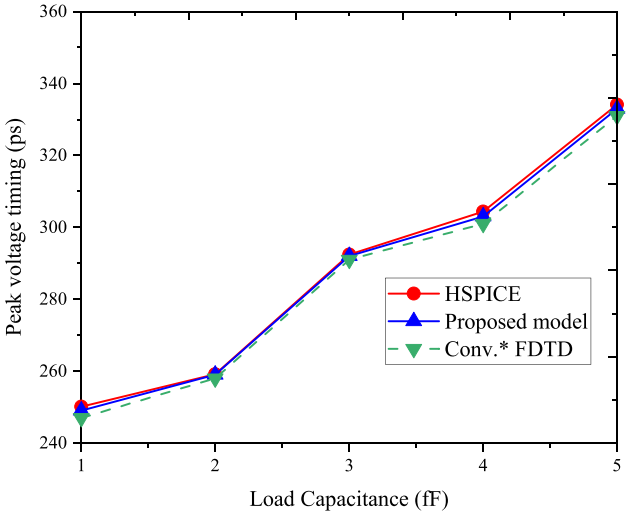

Fig. 9 Peak voltage timing with varying load capacitance for the victim line

Figures 9 and 10 demonstrate the peak voltage timing and peak voltage on the victim line for functional switching with varying values of load capacitance C_L. For instance, using an interconnect length of 1 mm with 20 space segments and 3500 time segments, the elapsed CPU time for the proposed MRTD model, the conventional FDTD model, and the HSPICE is measured using a PC Intel® Xeon® CPU operating at 3.30 GHz. The elapsed CPU times are shown in Fig. 11. The figure demonstrates the elapsed CPU times for crosstalk analysis of the coupled on-chip interconnect lines in various functional, dynamic in-phase, and dynamic out-of-phase switching. In terms of simulation time, HSPICE has a higher CPU runtime than both the MRTD and conventional FDTD models. However, the MRTD is slightly slower than the conventional FDTD due to the higher number of iterations required for better accuracy. As a result, there exists a trade-off between simulation time and accuracy.

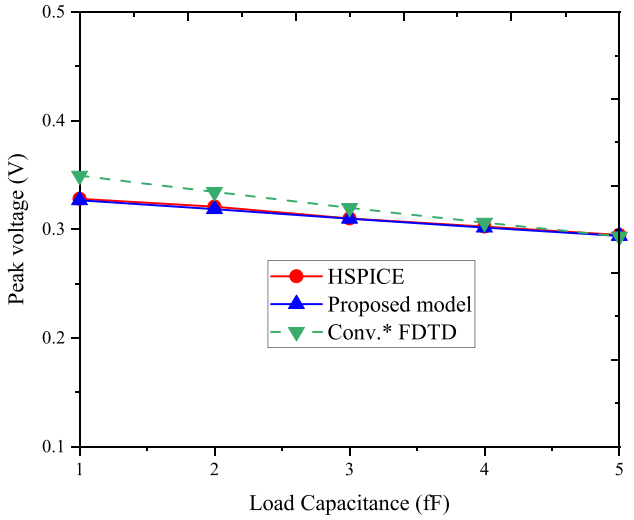

Fig. 10 Peak voltage with varying load capacitance for the victim line

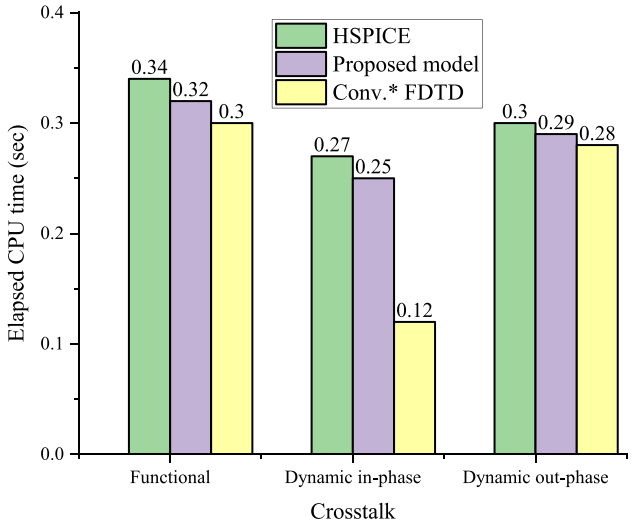

Fig. 11 Computational time with different crosstalk switching

4 Conclusion

The modified alpha-power law model is used in this paper to build an analytically dependent MRTD model for functional and dynamic crosstalk study of two mutually coupled transmission lines driven by a CMOS driver. This work provides a detailed study of a two-line coupled on-chip interconnects for functional, dynamic in-phase, and dynamic out-of-phase switching which induced crosstalk effects on the victim line. The Courant condition is strictly followed by the proposed model's stability. The influence of input transition time on crosstalk propagation delay under dynamic and peak voltage timing is investigated, as well as the peak voltage value for functional crosstalk. With regard to HSPICE, the proposed MRTD model and the FDTD confirm that the proposed MRTD model is in good agreement with HSPICE. According to the proposed model, the results show average errors of crosstalk-induced propagation delays in dynamic in-phase and out-of-phase on-chip interconnects of 0.53% and 0.18%, respectively, and functional crosstalk has peak voltage timing of 0.42% and a peak voltage value of 0.27%. Furthermore, the proposed MRTD model and FDTD model are validated with HSPICE for peak voltage timing and peak voltage value on the victim line for functional cases of various values of load capacitance, with average error of less than 1%. When compared to HSPICE, the elapsed CPU runtime for the MRTD model is significantly less. The analysis was performed on two mutually coupled interconnect lines but it can also be extended to M mutually coupled on-chip interconnect lines.

Acknowledgements This research was sponsored by the University Grants Commission (UGC) fellowship. The authors would like to thank the Principal, UCE(A) Osmania University for all their support.

Data availability Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

References

1. Moaiyeri, M.H., Hajmohammadi, Z., Khezeli, M.R., Jalali, A.: Effective reduction in crosstalk effects in quaternary integrated circuits using mixed carbon nanotube bundle interconnects. ECS J. Solid State Sci. Technol. **7**(5), M69 (2018). https://doi.org/10.1149/2.0111805jss
2. Khezeli, M.R., Moaiyeri, M.H., Jalali, A.: Active shielding of MWCNT bundle interconnects: an efficient approach to cancellation of crosstalk-induced functional failures in ternary logic. IEEE Trans. Electromag. Compat. **61**(1), 100–110 (2018). https://doi.org/10.1109/temc.2017.2788500
3. Rabaey, J.M., Chandrakasan, A.P., Nikolić, B.: Digital integrated circuits: a design perspective, vol. 7. Pearson education, Upper Saddle River, NJ (2003)
4. Alpert, C.J., Devgan, A., Kashyap, C.V.: RC delay metrics for performance optimization. IEEE Trans. Comput. Aid. Des. Integr. Circuits. Syst. **20**(5), 571–582 (2001). https://doi.org/10.1109/43.920682
5. Rubinstein, Jorge, Penfield, Paul, Horowitz, Mark A.: Signal delay in RC tree networks. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **2**(3), 202–211 (1983). https://doi.org/10.1145/62882.62932
6. Masoumi, M., Masoumi, N., Javanpak, A.: A new and efficient approach for estimating the accurate time-domain response of single and capacitive coupled distributed RC interconnects. Microelectron. J. **40**(8), 1212–1224 (2009). https://doi.org/10.1016/j.mejo.2009.04.004
7. Ismail, Yehea I., Friedman, Eby G., Neves, Jose L.: Equivalent Elmore delay for RLC trees. IEEE Trans. Comput. Aided Des.

Integr. Circuits Syst. **19**(1), 83–97 (2000). https://doi.org/10.1109/43.822622
8. Ismail, Y.I., Friedman, E.G.: Effects of inductance on the propagation delay and repeater insertion in VLSI circuits. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **8**(2), 195–206 (2000)
9. Agarwal, K.: Sylvester, Dennis, Blaauw, David: Modeling and analysis of crosstalk noise in coupled RLC interconnects. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **25**(5), 892–901 (2006). https://doi.org/10.1109/TCAD.2005.855961
10. Cui, J.P., Zhao, W.S., Yin, W.Y., Jun, H.: Signal transmission analysis of multilayer graphene nano-ribbon (MLGNR) interconnects. IEEE Trans. Electromag. Compat. **54**(1), 126–132 (2011). https://doi.org/10.1109/TEMC.2011.2172947
11. Li, X.C., Mao, J.F., Swaminathan, M.: Transient Analysis of CMOS-Gate-Driven *RLGC* Interconnects Based on FDTD. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **30**(4), 574–583 (2011). https://doi.org/10.1109/TCAD.2010.2095650
12. Liang, F., Wang, G., Lin, H.: Modeling of crosstalk effects in multiwall carbon nanotube interconnects. IEEE Trans. Electromag. Compat. **54**(1), 133–139 (2011). https://doi.org/10.1109/temc.2011.2172982
13. Kumar, V.R., Kaushik, B.K., Patnaik, A.: Crosstalk noise modeling of multiwall carbon nanotube (MWCNT) interconnects using finite-difference time-domain (FDTD) technique. Microelectr. Reliab. **55**(1), 155–163 (2015). https://doi.org/10.1016/j.microrel.2014.09.001
14. Tentzeris, E.M., Robertson, R.L., Harvey, J.F., Katehi, L.P.B.: Stability and dispersion analysis of Battle-Lemarie-based MRTD schemes. IEEE Trans. Microwave Theory Tech. **47**(7), 1004–1013 (1999). https://doi.org/10.1109/22.775432
15. Alighanbari, A., Sarris, C.D.: Dispersion properties and applications of the Coifman scaling function based S-MRTD. IEEE Trans. Antennas Propag. **54**(8), 2316–2325 (2006). https://doi.org/10.1109/tap.2006.879194
16. Krumpholz, M., Katehi, L.P.B.: MRTD: new time-domain schemes based on multiresolution analysis. IEEE Trans. Microwave Theory Tech. **44**(4), 555–571 (1996). https://doi.org/10.1109/22.491023
17. Grivet-Talocia, S.: On the accuracy of Haar-based multiresolution time-domain schemes. IEEE Microwave Guided Wave Lett. **10**(10), 397–399 (2000). https://doi.org/10.1109/75.877224
18. Fujii, M., Hoefer, W.J.R.: Dispersion of time domain wavelet Galerkin method based on Daubechies' compactly supported scaling functions with three and four vanishing moments. IEEE Microwave Guided Wave Lett. **10**(4), 125–127 (2000). https://doi.org/10.1109/75.846920
19. Massy, I., Ney, M.M.: A hybrid MRTD-FDTD technique for efficient field computation. In: Ahmed, I., Chen, Z.D. (eds.) Computational electromagnetics-retrospective and outlook, pp. 245–278. Springer, Singapore (2015)
20. Tong, Z., Sun, L., Li, Y., Luo, J.: Multiresolution time-domain scheme for terminal response of two-conductor transmission lines. Math. Probl. Eng. (2016). https://doi.org/10.1155/2016/8045749
21. Tong, Z., Sun, L., Li, Y., Angulo, L.D., Gonzalez, G., Salvador, L.J.: Multiresolution time-domain analysis of multiconductor transmission lines terminated in linear loads. Math. Probl. Eng. (2017). https://doi.org/10.1155/2017/9845702
22. Rebelli, S., Rao, N.B.: A novel MRTD model for signal integrity analysis of resistive driven coupled copper interconnects. COMPEL-Int. J. Comput. Math. Electr. Electr. Eng. (2018). https://doi.org/10.1108/COMPEL-12-2016-0521
23. Rebelli, S., Nistala, B.R.: An efficient MRTD model for the analysis of crosstalk in CMOS-driven coupled Cu interconnects. Radioengineering **27**(2), 532–540 (2018). https://doi.org/10.13164/re.2018.0532
24. Rebelli, S., Nistala, B.R.: A multiresolution time domain (MRTD) method for crosstalk noise modeling of CMOS-gate-driven coupled MWCNT interconnects. IEEE Transactions on Electromagnetic Compatibility **62**(2), 521–531 (2019). https://doi.org/10.1109/temc.2019.2903728
25. Paul, C.R.: Incorporation of terminal constraints in the FDTD analysis of transmission lines. IEEE Trans. Electromag. Compat. **36**(2), 85–91 (1994). https://doi.org/10.1109/15.293284
26. Pan, G.W.: Wavelets in electromagnetics and device modeling, vol. 159. Wiley, London (2003)
27. Dogaru, T., Carin, L.: Multiresolution time-domain algorithm using CDF biorthogonal wavelets. IEEE Trans. Microwave Theory Tech. **49**(5), 902–912 (2001). https://doi.org/10.1109/22.920147
28. Kumar, M.G., Chandel, R., Agrawal, Y.: An efficient crosstalk model for coupled multiwalled carbon nanotube interconnects. IEEE Trans. Electromag. Compat. **60**(2), 487–496 (2017). https://doi.org/10.1109/TEMC.2017.2719052
29. International Technology Roadmap for Semiconductors (ITRS) 2013.[Online]. Available:http://www.itrs.net/
30. Badugu, D., Madhuri, S.S.: Crosstalk noise analysis of on-chip interconnects for ternary logic applications using FDTD. Microelectr. J. **93**, 104633 (2019). https://doi.org/10.1016/j.mejo.2019.104633
31. Synopsys for HSPICE tools, (2008). [Online]. Available:http://www.synopsys.com