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New tunable resistorless grounded meminductor emulator

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Abstract
In this research article, a grounded resistorless meminductor emulator is proposed. The proposed emulator uses one voltage differencing transconductance amplifier (VDTA) and one operational transconductance amplifier (OTA) with corresponding grounded capacitances. It can be operated in both decremental and incremental configurations. The comparison of the proposed emulator with available literature is also included. The proposed meminductor emulator circuit has been designed and simulated in Cadence Virtuoso Analog Design Environment using 180 nm gdpk technology parameters. Moreover, the application of the proposed emulator as a second-order bandpass filter (BPF) is also given. The simulation results agree well with the theory and confirm the meminductor functionality.

Keywords Memristor · Meminductor · Operational transconductance amplifier · Voltage differencing transconductance amplifier · Integrated circuit

1 Introduction

The essential elements of circuits are resistor, capacitor, and inductor, and these essential elements describe the relationship between the voltage, current, and charge. Other than these essential elements, in 1971, L. O. Chua [1] introduced one more component of the circuit called a memristor, which is filling the gap between the relationship between the current, charge, voltage, and flux. Now this new system, which has a mathematical relationship between charge and flux, is finally a practical design discovered by Hewlett Packard (HP), which is based on a thin film of titanium dioxide [2]. It waves the researcher toward the memristor. After the concept of memristor, two new memory elements charge controlled memcapacitor and meminductor [3] introduced, which has the same storage capacity based on the capacitance and inductance, which can be used efficiently in the absence of a power source. The problem was how to make these designs fabricate and make them compatible with the trends. Most of the circuits present in the market are based on the CMOS. In recent years, a lot of scientific studies have been done for these modern memory elements with their design and their application [4–7]. A new era of research has been started for hybrid memristors, memcapacitors, and meminductors based on CMOS devices. Now in design researcher primary motivation is toward making a memory for the real-time application in low power digital computation [8], neuromorphic circuit [9], adaptive filter [10], chaotic signal generator [11], programmable analog circuits [12, 13], adaptive learning [14, 15] and non-volatile memories [16, 17].

A lot of attention has been given to design grounded and floating meminductor emulators utilizing the different high-performance active analog building blocks (ABBs) such as operational amplifier (OA) [21], second-generation current conveyor (CCII) [22], voltage differencing transconductance amplifier (VDTA) [24], and operational transconductance amplifier (OTA) [25] have been reported. Unfortunately, these reported circuits suffer from one or more of the following weaknesses:

- Excessive use of passive components, especially external resistors [18].
- Lack of electronic tenability [18, 19, 21, 22].
- Use of floating capacitors, which is not suitable for monolithic integration [25].
- Use of multiplier, which has suffered lots of limitations [18, 19, 25].

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- Limited operating frequency range up to a few kHz [18–22, 25].
- The reported circuits [18, 19, 21] uses OA, which has suffered the gain bandwidth and slew rate limitations.
- Use of memristors [21, 22].

The authors in this article proposed a new tunable grounded meminductor emulator using VDTA and OTA that overcomes all the drawbacks mentioned above. The proposed circuit provides the following advantages features:

- The proposed circuit does not employ an external multiplier.
- The proposed circuit employs only grounded capacitors, which are advantages from the point of IC implementation. The use of grounded capacitor circuits can compensate for the stray capacitances at their nodes.
- The proposed emulator is completely resistorless, i.e., no external resistors are employed.
- The proposed circuit provides electronic tunability.
- The proposed circuit does not employ memristors.

This paper presents a resistless meminductor emulator with grounded capacitors. The paper is organized as follows. Section 2 describes the port relationship of VDTA and OTA ABBs and illustrates their symbol and CMOS implementations, followed by Sect. 3, which describes the proposed emulator with a detailed mathematical explanation of its operation. Section 4 presents the simulation results of various analyses performed. Section 5 shows the comparison of the proposed meminductor emulator with available literature. Conclusions are drawn in Sect. 6.

2 Analog building blocks with their properties

In this paper, one voltage difference transconductance amplifier (VDTA) and one operational transconductance amplifier (OTA) are used as active building blocks (ABBs). The VDTA is a simple and versatile ABB. It is composed of two cascaded transconductance amplifiers, and both transconductances (g_{m1} and g_{m2}) provide electronic tunability [12]. The port relationships of VDTA are given as:

$$I_Z = g_{m1}\left(V_P - V_N\right), \quad I_{X+} = g_{m2}V_Z, \quad I_{X-} = -g_{m2}V_Z \tag{1}$$

The schematic symbol and MOS realization of VDTA are shown in Fig. 1. The differential input voltage $\left(V_P - V_N\right)$ is the function of transconductance (g_{m1}) is transferred to a current in Z port and similarly, transconductance (g_{m2}) with voltage (V_Z) acts as a current in X port. Finally, both the transconductances are defined by $g_{m1} = \frac{g_1+g_4}{2}$, and $g_{m2} = \frac{g_5+g_8}{2}$. Here, g_i is the transconductance value of i^{th} the transistor is denoted by $g_i = \sqrt{2I_D k_{Mi}}$. Assume the following pairs $\left(M_1, M_2\right)$, $\left(M_3, M_4\right)$, $\left(M_5, M_6\right)$ *and* $\left(M_7, M_8\right)$ are identical. This results in the reduction of transconductance gains (g_{m1} and g_{m2}) of VDTA can be expressed as:

$$g_{m1} = k_1\left(V_{B1} - V_{ss} - V_{th}\right) \text{ and } g_{m2} = k_2\left(V_{B2} - V_{ss} - V_{th}\right) \tag{2}$$

where, $k_1 = \left[\frac{\sqrt{k_{M1,2}}+\sqrt{k_{M3,4}}}{2\sqrt{2}}\right]\sqrt{k_B}$ and $k_2 = \left[\frac{\sqrt{k_{M5,6}}+\sqrt{k_{M7,8}}}{2\sqrt{2}}\right]\sqrt{k_B}$

.

The OTA is a high gain high input and output impedance amplifier. The circuit symbol and its CMOS implementation of OTA are shown in Fig. 2. The characteristics of an OTA are expressed as:

$$I_O = G_M V_{in}, \quad V_{in} = \text{ differential input } = V_+ - V_- \tag{3}$$

where $V_{in} = V_+ - V_-$ is the differential input voltage and G_M is the transconductance of an OTA. The transconductance of OTA (G_M) is expressed as:

$$G_M = \frac{K}{\sqrt{2}}\left(V_B - V_{ss} - 2V_{th}\right) \tag{4}$$

where $K = \mu C_{Ox}\frac{W}{L}$ and the μ, C_{ox}, W, L, V_{th} are mobility, oxide capacitance, channel width, channel length, and the threshold voltage of MOS transistor, respectively.

3 Proposed circuit

The meminductor and memcapacitor are the elements of the memristor family. The input current (I_{in}) and flux (ϕ_{in}) relation of meminductor is defined as

$$\phi_{in}(t) = L_M(q)I_{in}(t) \tag{5}$$

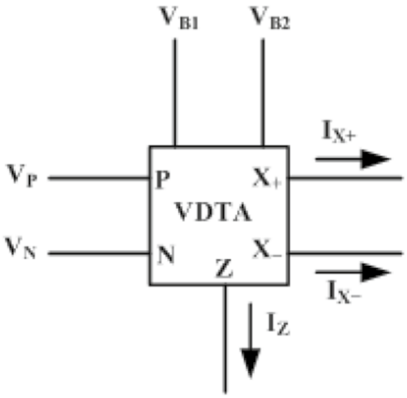
$$\frac{I_{in}(t)}{\phi_{in}(t)} = L_M^{-1}(q) \tag{6}$$

where L_M^{-1} is the inverse meminductance of the meminductor.

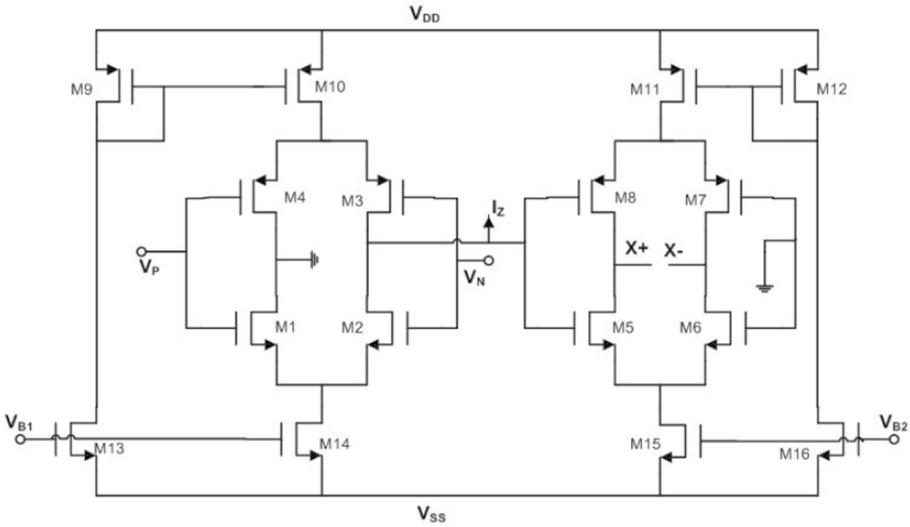
The flux control meminductor [13–15] having an initial value of inverse meminductance (x) and decremental or incremental product term (y) is generally expressed as

$$\frac{I_{in}(t)}{\phi_{in}(t)} = \left[x \pm yp(t)\right] \tag{7}$$

A proposed grounded resistorless meminductor is implemented using one VDTA, one OTA, and two grounded capacitors. The schematic diagram of the grounded meminductor is shown in Fig. 3. From Fig. 3,



(a)



(b)

Fig. 1 VDTA: **a** symbol, **b** CMOS implementation

$$V_z = V_{\text{in}}$$
$$I_{\text{in}} = -I_z = g_{m1} V_n \tag{8}$$

$$I_{X+} = g_{m2} V_{\text{in}} \tag{9}$$

$$V_n = V_1 = \frac{g_{m2}}{C_1} \int V_{\text{in}} dt = \frac{g_{m2}\phi(t)}{C_1} \tag{10}$$

From Eqs. (8) and (10)

$$I_{in} = \frac{g_{m1} g_{m2} \phi(t)}{C_1}$$
$$\frac{I_{\text{in}}}{\phi_{\text{in}}} = \frac{g_{m1} g_{m2}}{C_1} \tag{11}$$

From Eqs. (2) and (11)

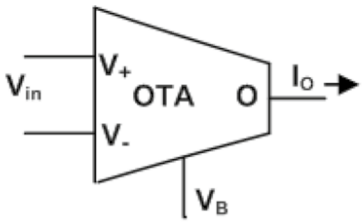
$$\frac{I_{\text{in}}}{\phi_{\text{in}}} = \frac{g_{m2}}{C_1} k_1 \left(V_{B1} - V_{\text{ss}} - V_{\text{th}}\right) \tag{12}$$

$$I_O = \pm g_{m3} V_1$$
$$I_O = \pm \frac{g_{m3} g_{m2} \phi(t)}{C_1} \tag{13}$$
$$V_{B1} = \pm \frac{g_{m3} g_{m2} p(t)}{C_1 C_2}$$

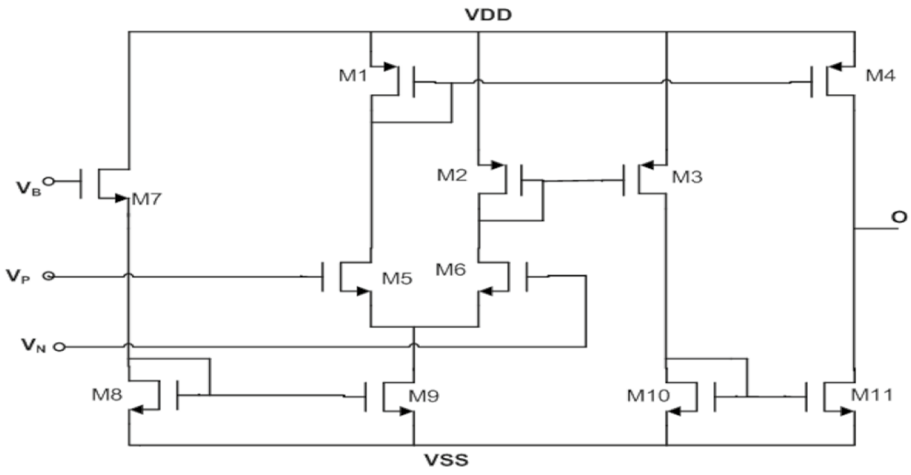
where $p(t) = \int \Phi(t) dt$. From Eqs. (12) and (13)

$$\frac{I_{\text{in}}}{\phi_{\text{in}}} = \frac{g_{m2}}{C_1} k_1 \left(\pm \frac{g_{m3} g_{m2} p(t)}{C_1 C_2} - V_{\text{ss}} - V_{\text{th}} \right) \tag{14}$$

Eq. (14) shows that the proposed circuit works as a grounded meminductor. Where g_{m3} and g_{m2} can be controlled by the



(a)



(b)

Fig. 2 OTA: **a** symbol, **b** CMOS implementation

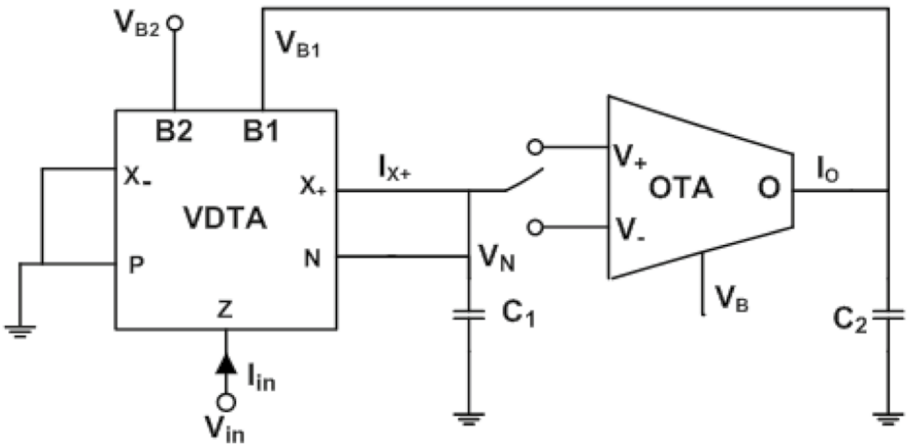


Fig. 3 Proposed grounded meminductor emulator employing one OTA, one VDTA, and two capacitors

bias voltage V_B and V_{B2}, respectively. That's why the proposed grounded meminductor circuit makes it electronically tunable. The decremental/incremental operation can be achieved by the proper switch selection between the V_+ and V_- terminal of OTA. Equation (14) represents decremental/incremental meminductor where $-K_1(g_{m2}/C_1)(V_{SS}+V_{th})$ is a constant value, and $\pm K_1(g_{m2}/C_1)(g_{m3}g_{m2}\rho(t)/C_1C_2)$ is the time-varying term as $\rho(t)$ is the function of the time-varying input signal.

4 Simulation results

The proposed meminductor emulator is theoretically proved, and all simulated results are verified on Cadence Virtuoso 180 nm gpdk technology parameters. The aspect ratio of VDTA and OTA are shown in Table 1. The supply voltages for CMOS based VDTA and OTA are $V_{DD} = -V_{SS} = 1.2$ V and biasing voltage is given

Table 1 Aspect ratio of VDTA and OTA

Device	MOS transistors	W(μm)/L(μm)
VDTA	$M_{3\text{-}4}$, $M_{7\text{-}12}$	13/0.36
	$M_{1\text{-}2}$, $M_{5\text{-}6}$, $M_{13\text{-}16}$	4/0.36
OTA	$M_{1\text{-}4}$	12/0.375
	M_{10}	12/0.510
	$M_{5\text{-}9}$, M_{11}	12/0.500

by $V_{B1} = V_{B2} = 0.1$ V. Figure 4a and b shows the transient response, and Fig. 4c shows the hysteresis loop of grounded meminductor with an input signal amplitude of 500 mV at a frequency of 3 MHz, and the capacitance values are chosen as $C_1 = 2$ pF and $C_2 = 3$ pF. The non-volatile is the most key feature of the meminductor. The characteristics behavior of the meminductor emulator is examined by considering the input pulse signal with an amplitude of 500 mV and pulse width 100 ns for the period of 250 ns. The changes in the meminductance input signal are plotted with respect to time is shown in Fig. 5 for incremental and decremental topology, respectively. During ON time, the ratio of current and flux varies, whereas it remains constant during the OFF state. Hence, we can conclude that the meminductor is non-volatile in nature.

4.1 Process variation

When the design methodology of monolithic integration is followed, then the process variation is an important design aspect that needs to take care of. The proposed grounded meminductor emulator is analyzed for the different process variation such as SS (Slow N and Slow P transistors), SF (Slow N and Fast P transistors), NN (Nominal N and Nominal P transistors), FS (Fast N and slow P transistors) and FF (Fast N and Fast P transistors). The process variation is done at 500 kHz for the values of $C_1 = 30$ pF and $C_2 = 40$ pF, as shown in Fig. 6. It's clear from Fig. 6 that the flow of current for FF mode is larger than in SS mode, which is expected for the proposed emulator.

4.2 Capacitor variation

The proposed meminductor emulator is analyzed for a different capacitor (40 pF, 45 pF, 50 pF, 60 pF), and the effect on the pinched hysteresis loop for variation of the capacitor is shown in Fig. 7, which shows a current decrease as an increase in the value of the capacitor. It concludes that the hysteresis loop shrinks with an increase in the capacitor.

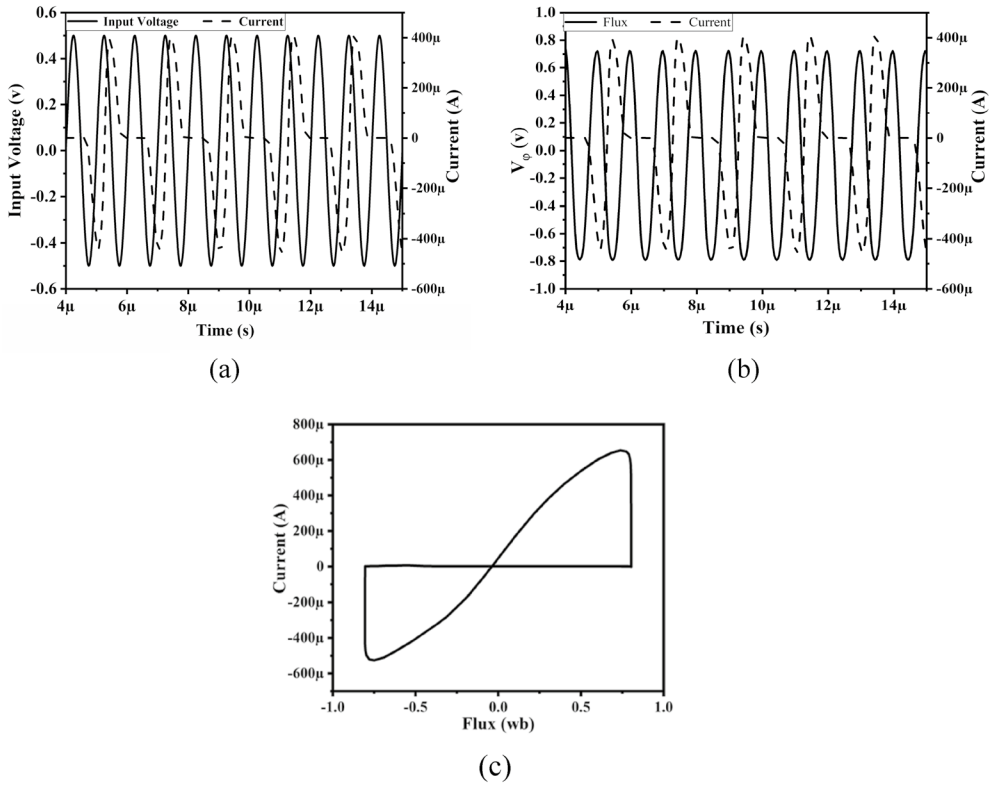


Fig. 4 Transient response of proposed meminductor emulator using a 500 mV sinusoidal input signal with a frequency of 3 MHz: **a** current–voltage characteristics, **b** current-flux characteristics, and **c** closed pinched hysteresis loop of the input current versus flux

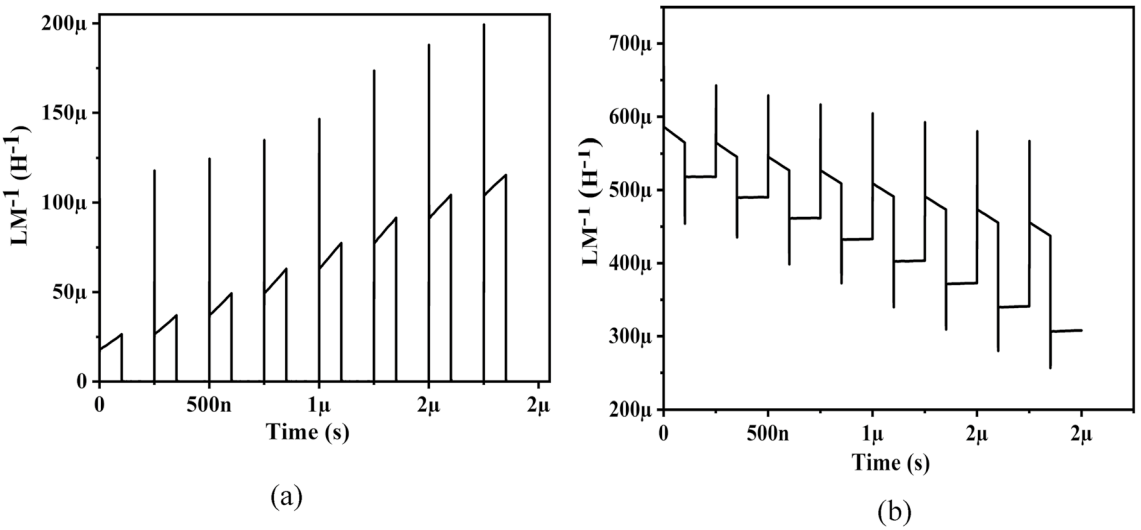


Fig. 5 Non-volatile behavior of proposed meminductor emulator for **a** incremental, and **b** decremental topology of input pulse signal with an amplitude of 500 mV and pulse width as 100 ns for a period of 250 ns shows the meminductance varies during the ON time of the input pulse signal and remains constant during the off time

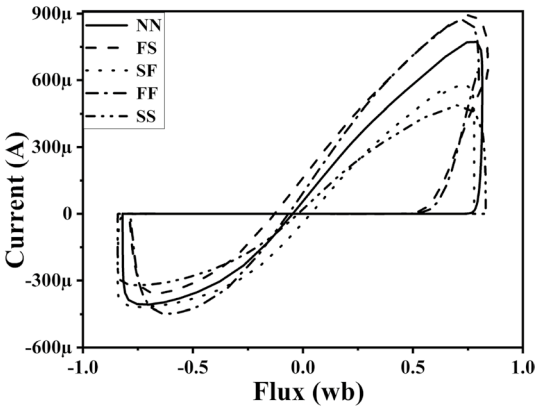


Fig. 6 Pinched hysteresis loop (waveform of 'i' versus 'φ') variation at different process corners at 500 kHz for the passive component values of $C_1 = 30$ pF and $C_2 = 40$ pF, shows that the current flow in the case of FF mode is larger than in SS mode

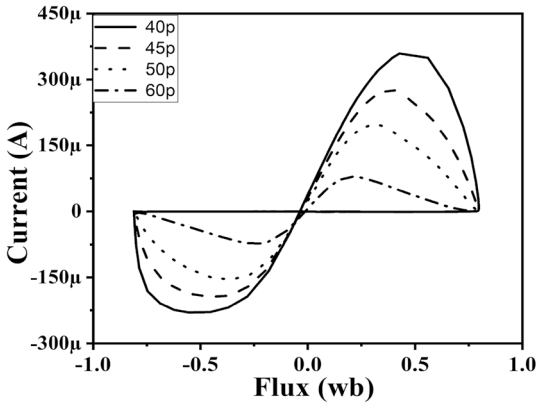


Fig. 7 The pinched hysteresis loop of the proposed meminductor emulator for the capacitor of 40 pF, 45 pF, 50 pF, and 60 pF shows the hysteresis area decreases with an increase in the capacitor

4.3 Voltage variation

In this meminductor emulator, the bias voltage of active analog block OTA is varying (50 mV, 100 mV, 200 mV, 300 mV) with fixed values of the capacitors $C_1 = 60$ pF, $C_2 = 70$ pF, and the results are shown in Fig. 8. The results show that when bias voltage increased, then the flow of current in the meminductor is also increased. This provides adjustability in different process corners.

4.4 Frequency variation

In this case, the emulator input bias voltage is fixed, and the frequency varying (200 kHz, 300 kHz, 400 kHz, and 500 kHz) and the results are shown in Fig. 9 that shows the area of the hysteresis loop decreased as increased the value of frequency. Figure 10 showed the hysteresis loop variation for simultaneously varying the values of capacitor and frequency. This shows that the area under the hysteresis loop shrinks at the frequency increase and capacitor decreases.

4.5 Temperature variation

The temperature variation is one of the factors that affect the threshold voltage, saturation velocity, and carrier mobility of integrated circuits (ICs) that affect the transistor drain current [23]. The proposed meminductor emulator is implemented by using CMOS-based VDTA and OTA

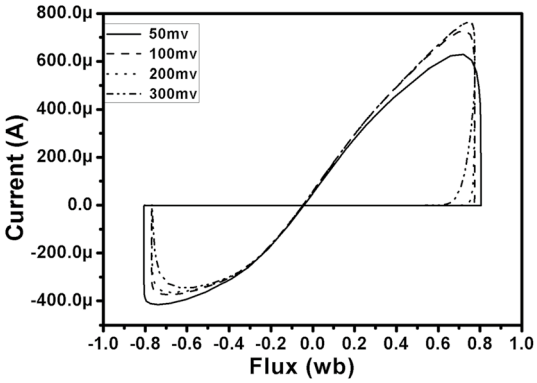


Fig. 8 Hysteresis Loop for the different bias voltages 50 mV, 100 mV, 200 mV, and 300 mV which shows an increase in current for lower bias voltage and vice versa

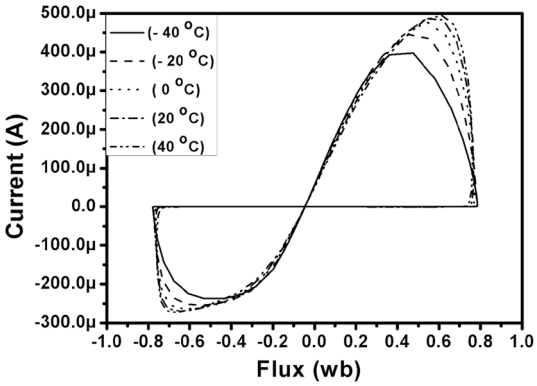


Fig. 11 Pinched hysteresis loop at various temperatures $-40^0C, -20^0C, 0^0C, +20^0C, +40^0C$

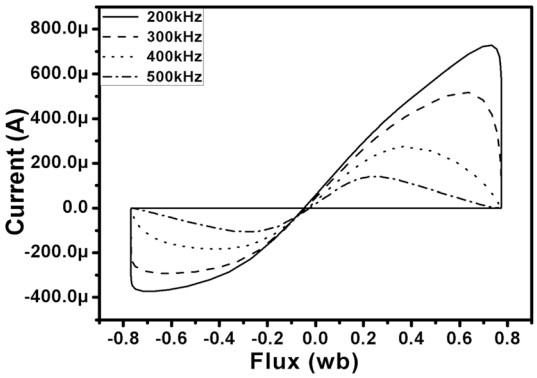


Fig. 9 The current versus flux plots illustrating at frequencies of 200 kHz, 300 kHz, 400 kHz, and 500 kHz

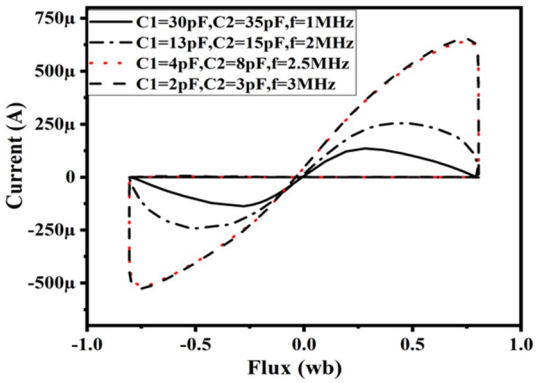


Fig. 10 Hysteresis Loop at various frequencies and capacitors (case1: $C_1 = 30$ pF, $C_2 = 35$ pF, $f = 1$ MHz; case2: $C_1 = 13$ pF, $C_2 = 15$ pF, $f = 2$ MHz; case3: $C_1 = 4$ pF, $C_2 = 8$ pF, $f = 2.5$ MHz; case4: $C_1 = 2$ pF, $C_2 = 3$ pF, $f = 3$ MHz)

structures. Therefore the temperature effect is necessary to analyze for the proposed meminductor's responses. The simulation results at various temperatures (−40 °C, 20 °C, 0 °C, 20 °C, 40 °C) are shown in Fig. 11. It concludes that the temperature effect is negligible that shows the robustness of the proposed emulator.

4.6 Application of proposed meminductor emulator

In this section, the performance of the proposed grounded meminductor emulator is verified by the implementation of a second-order bandpass filter (BPF). The second-order passive RLC based BPF is compared with a meminductor emulator-based second-order BPF if we replaced passive inductance (L) with meminductor (MEM-L). The circuit diagram of RLC and RMC based second-order BPF is shown in Fig. 12. The transfer function H(s), cut-off frequency (f_0 and quality factor (Q) of the filter are given as

$$H(s) = \frac{\frac{S}{RC}}{S^2 + \frac{S}{RC} + \frac{1}{LC}}, \quad \omega_0 = \frac{1}{\sqrt{LC}}, \quad Q = R\sqrt{\frac{C}{L}} \tag{15}$$

The values chosen for simulation are $R = 10$ GΩ, $C = 200$ pF, and $L = 15$ nH for the center frequency of 91.88 MHz and unity quality factor, respectively. The frequency response of both the RLC and RMC based filter is shown in Fig. 13a and b respectively. It is clear from Fig. 13a and b that the theoretical center frequency is 91.88 MHz, while the simulated frequency for the values of the same components is 92.00 MHz. The error is due to the non-ideality of the components. This shows that the proposed meminductor emulator works very well.

5 Comparision

The performance of the proposed meminductor emulator circuit with previously available literature is given in Table 2 in terms of the number of passive and active components, operation mode (grounded or floating), and the operating frequency. It can conclude that the operating frequency range of the proposed emulator is higher than the previous existing meminductor emulator, and it has a fewer number of transistors used.

Table 2 concludes the specialty of the proposed meminductor model in terms of the higher frequency with a minimum number of components. The proposed model has only one VDTA, one OTA, and two grounded capacitors, which is less as compared to the previous one. The literature also reveals that the meminductor model [21, 22] requires a memristor, and hence the frequency of operation depends on the memristor operating range as well. Hence the proposed meminductor emulator implement using one VDTA as well as OTA which, uses a transconductance term to vary

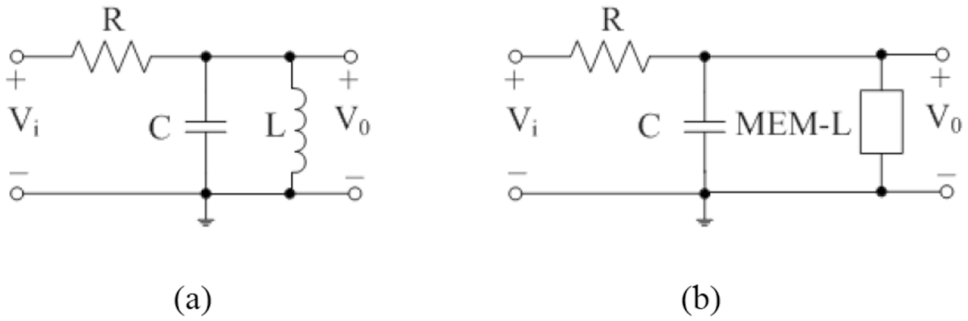


Fig. 12 Circuits diagram of second-order BPF: **a** passive RLC based, **b** RMC based

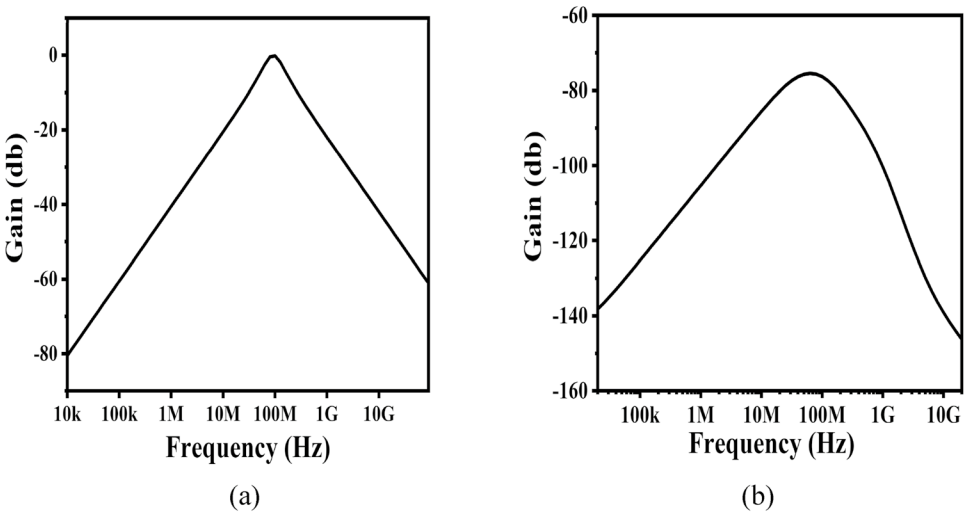


Fig. 13 Cadence result showing the frequency response for the center frequency of 91.88 MHz: **a** RLC based BPF, **b** RMC based BPF

Table 2 Comparison with previous existing meminductor emulators

Refs. no.	No. of active comp	No. of passive comp	Mode	Operating frequency
[20]	–	–	–	Few Hz
[21]	OA–1	R -1, C -1, MR -1	Grounded	Few Hz
[22]	DOCCII–2	R -1, C -1, MR -1	Floating	Few Hz
[18]	OA-2, AD844-4, AD633-1	R -7, C -2	Floating	Few Hz
[19]	OA-3, NMOS-12, AD633-1	R -2, C -2, L -1	Grounded	Few Hz
[24]	VDTA -2	C -2	Grounded	1 MHz
		R -1, C -2	Floating	1 MHz
[25]	OTA-2, MULT-1	R-2, C-2	Grounded	10 kHz
Prop	VDTA -1, OTA -1	C -2	Grounded	3 MHz

the time-dependent inductance makes the emulator suitable for higher frequency.

6 Conclusions

In this article, a new electronically tunable grounded meminductor emulator using one VDTA, one OTA, and two capacitors has presented. The advantages of the proposed meminductor are the following: (i) resistor less structure, (ii) higher operating frequency range, (iii) electronic tunability by a bias voltage, (iv) use of grounded capacitors which are suitable for monolithic IC fabrication, and (v) less number of transistor counts. An application of the proposed emulator as a BPF is also given. The Cadence Virtuoso simulation results agree well with the theory.

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