



Ultracompact all-optical full adders using an interference effect based on 2D photonic crystal nanoring resonators

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Received: 21 April 2020 / Accepted: 30 October 2020 / Published online: 22 November 2020
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Abstract

Given the special place of hybrid logic circuits such as all-optical full adders in next-generation digital systems, a new kind of these structures using two-dimensional (2D) photonic crystals (2D-PC) is designed and simulated herein. The proposed structure is made of a hexagonal nanoring resonator (NRR), a coupling rod, and several waveguides. In this all-optical full adder, the mechanism of the interference effect in the PCs is used to simplify and minimize the structure. To make the structure flexible, the radius of the dielectric rod in the whole structure and the NRR are considered based on a lattice constant of $0.2a$ and $0.04a$, respectively. The structure is operated at a wavelength of 1550 nm, considering the value of the power entering the waveguides and that exiting the Carry and Sum ports. To analyze the all-optical full adder, the plane-wave expansion method and finite-difference time-domain method are applied respectively to calculate the bandgap diagram and obtain the transmission and propagation of the optical field. In the proposed structure, the contrast ratio at the Carry and Sum has been investigated in a unique and novel way, yielding values of 10.68 and 9.03 dB, respectively. In addition, the maximum and minimum response time for the Carry and Sum are obtained as 1.6 and 0.75 ps, respectively. The total footprint of the structure is about $183 \mu\text{m}^2$. Due to its ultracompact size, low power consumption, fast response time, and simple structure, this all-optical full adder is suitable for use in low-power optical integrated circuits.

Keywords Full adder · Photonic crystals · Contrast ratio · Response time · Finite-difference time-domain method

1 Introduction

Advances resulting from new technologies and the high speed of light are important factors affecting the development of integrated optical devices. This approach will gradually result in the replacement of classical electronic systems by new-generation optical systems. Considering the importance of this issue, the rapid transfer, receipt, storage, and processing of information and most importantly all-optical logic computations using new-generation optical devices are the most important factors contributing to the realization of photonic integration technology and thus optical integrated

circuits (OICs) [1]. In this context, new photonic materials with micro–nanometer sizes such as graphene, plasmon, and photonic crystals (PC) [2–4], which offer unique capabilities including the modulation of photon emission and control modes, and the diffusion and distribution of light in the structure, are considered to be significantly important for the development of such technologies. Moreover, among the mentioned photonic materials, PCs with aperiodic structure have attracted particular attention due to their range of photonic bandgap (PBG) [5], which plays a critical role in directing and controlling light, as well as their unique features such as small size and the ability to process and transfer data quickly, combined with a simple design that facilitates their construction and is considered to be one of the basic requirements regarding the implementation of OICs. Accordingly, PCs can be used in the design and implementation of various optical devices, including optical waveguides [6, 7], optical filters [8, 9], optical sensors [10–12], multiplexer/demultiplexers [13–17], optical converters [18], lasers [19], optical power dividers [20], optical logic gates [21–26], etc.

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One of the most important and practical types of photonic structure, namely all-optical logic gates based on PCs, being considered to be one of the basic requirements for new-generation OICs, is designed herein. When all-optical logic gates are designed, parameters such as the contrast ratio (CR) [27], the response time to the input signal, the applicability, the output power, and the bit rate (BR) [28] are evaluated and compared, and the efficiency of the gate thereby determined. Optical logic gates based on PCs can be designed using three main mechanisms, namely the nonlinear Kerr effect, the self-collimation effect, and the interference effect in PCs. Herein, to optimize these parameters, the interference effect of waves in PCs is used to facilitate the design and implementation. The proposal is for an integrated structure which is not composed of different logic gates, resulting in a very compact footprint compared with previously proposed full adders. Also, the optical power intensity required at the input ports is lower than for previously proposed structures [21, 27, 29–31]. This approach also leads to the construction of a smaller structure with a higher CR than when using the other two mechanisms. Using the current method, the structure operates such that, if the light waves have a phase difference of about $2n\pi$ ($n = 1, 2, 3$, etc.), constructive interference will occur and the logic gate output will be 1 or ON. However, if the phase difference between the waves is about $(2n + 1)\pi$ with $n = 1, 2, 3$, etc., destructive interference will occur and the logic gate output will be 0 or OFF. Accordingly, using the phase difference between the waves, the output waves can be controlled using the structure of PC logic gates and a desired structure designed. For the proposed structure, the response time is calculated to be 1.1 ps while the CR for the Carry and Sum ports is 10.68 and 9.03 dB, respectively.

In general, various numerical methods can be used to analyze PCs, each having its own advantages and disadvantages. Such numerical methods can be divided into two general categories, namely those carried out in the frequency and time domain. Due to its compatibility with parallel processing and data extraction over a wide range of wavelengths, the finite-difference time-domain (FDTD) method [32] is applied herein to simulate the structure and derive the output spectrum results. Moreover, the optical devices are designed and constructed using PCs based on the range of the PBG and the plane-wave expansion (PWE) method. The PWE method has been applied to separate transverse electric (TE) and transverse magnetic (TM) modes and to calculate the frequency eigenvalues and PBG of the proposed structure [33].

The rest of this manuscript was organized as follows: Sect. 2 discusses the all-optical full-adder block and the design procedure for the proposed structure, while the simulation results are presented and discussed in Sect. 3. Finally, conclusions are drawn in Sect. 4.

2 All-optical full-adder block

Hybrid logic circuits are currently receiving much attention in the field of digital systems. These types of logic circuit generally have different inputs and outputs and can be designed and constructed using various gates. The full adder is among these important logic circuits. The structure of a full adder includes three inputs and two outputs. The two inputs A and B of this circuit represent the two most significant bits of the whole full adder, while the third input C represents the carry bit resulting from the least significant position. The two outputs in this circuit are denoted as the Sum and Carry, where the Sum represents the value of the least significant sum and the binary output variable Carry the output carry. The truth table of the whole binary full adder with its possible inputs is presented in Table 1, according to which the different modes of 1 or ON in the Sum and Carry outputs can be expressed as follows:

$$\text{Sum} = A \oplus B \oplus C = A'B'C + A'BC' + AB'C' + ABC,$$

$$\text{Carry} = A'BC + AB'C + ABC' + ABC.$$

In this work, 2D PC structures are used to design and simulate an all-optical full adder for use in next-generation digital systems. For this purpose, 23 dielectric rods along the x -axis and 21 dielectric rods along the z -axis are used. For design simplicity and to use silicon technology, the dielectric rods were made of silicon with a refractive index of $n_r = 3.46$, placed in an air background with refractive index of $n_s = 1$. The radius of the dielectric rods used was $R = 0.2a$, while the lattice constant was $a = 630$ nm, and the hexagonal lattice constant was selected. According to the desired structural parameters, the final size of the structure is estimated to be about $183 \mu\text{m}^2$. To take advantage of the unique properties of PCs for controlling and directing light in the design and construction of optical devices, the first priority is to analyze the range of the PBG and the amount of light scattering in these structures. The PWE method is thus used to determine the range of the PBG. According to the results obtained for the

Table 1 The truth table for the full adder

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

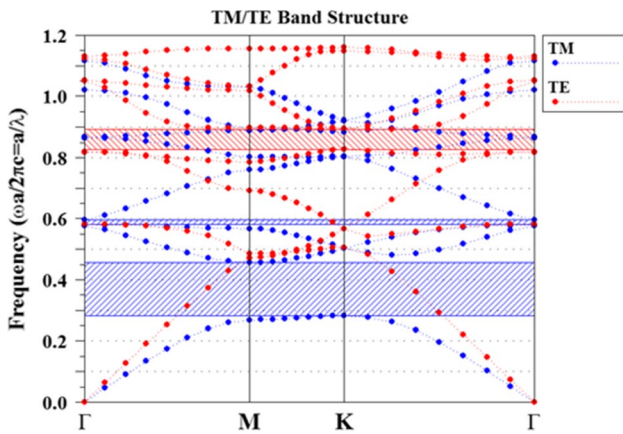


Fig. 1 The proposed PBG structure

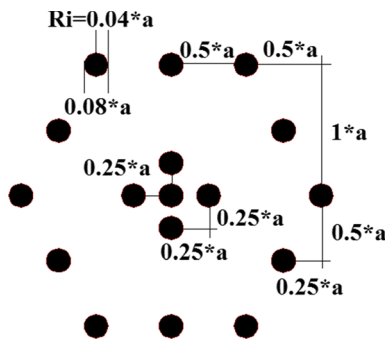


Fig. 2 A schematic of the proposed PC-NRR topology used in this paper

amount of light scattering within the given structure, the structure has three PBG ranges for the TE and TM modes (Fig. 1). The first PBG for the TM mode lies in the range of $0.285 \leq a/\lambda \leq 0.460$, and the second PBG for the TM mode lies in the range of $0.575 \leq a/\lambda \leq 0.595$, being equal to $1369 \text{ nm} \leq \lambda \leq 2210 \text{ nm}$ and $1058 \text{ nm} \leq \lambda \leq 1095 \text{ nm}$,

respectively. In addition, the PBG for the TE mode lies in the range of $0.830 \leq a/\lambda \leq 0.890$, which is equal to $707 \text{ nm} \leq \lambda \leq 759 \text{ nm}$. According to the wavelength ranges obtained for the proposed structure, the first PBG for the TM mode is considered to be optimal, due to its wide bandwidth.

The basic structure of the desired all-optical full adder is designed based on the NRR and using the interference effects between the waves. The structure consists of 23 and 21 dielectric rods in the x - and z -direction, respectively. The proposed NRR is made of a 2D hexagonal lattice of silicon. The structure of the given NRR used in the design of the full adder is shown in Fig. 2. This basic structure comprises a square with diameter of 0.5 and rotation of 45° within a hexagon. The length of the sides of the hexagon is equal to a , while the diameter of the dielectric rods constituting the structure is equal to $0.08a$. The length of the sides of the square is 0.353 , while the radius of the dielectric rods constituting it is $0.04a$.

The structure of the proposed all-optical full adder is shown in Fig. 3. In this structure, to create a full adder with three input ports (A , B , and C) and two output ports (Sum and Carry), five waveguides, four 120° bends, and a hexagonal NRR with a coupling rod are used to control and guide the light to implement the different logic states. The input Gaussian pulses enter the structure from each of the ports A , B , and C through the waveguides $W1$, $W2$, and $W3$, and depending on the interference between the waveguides and the hexagonal NRR, the output power in the various states of the SUM and Carry outputs exits through $W4$ and $W5$. The proposed NRR placed between the waveguides is described by parameters such as the refractive index and radius of the coupling rods, the radius of the internal rods, the relative positioning of the rods, the output wavelength range, the output power, and the quality coefficient of the output channel. The values of the main parameters and materials properties used in the simulations are presented in Table 2.

Fig. 3 A sketch of the final proposed full-adder logic gate based on the PC-NRR

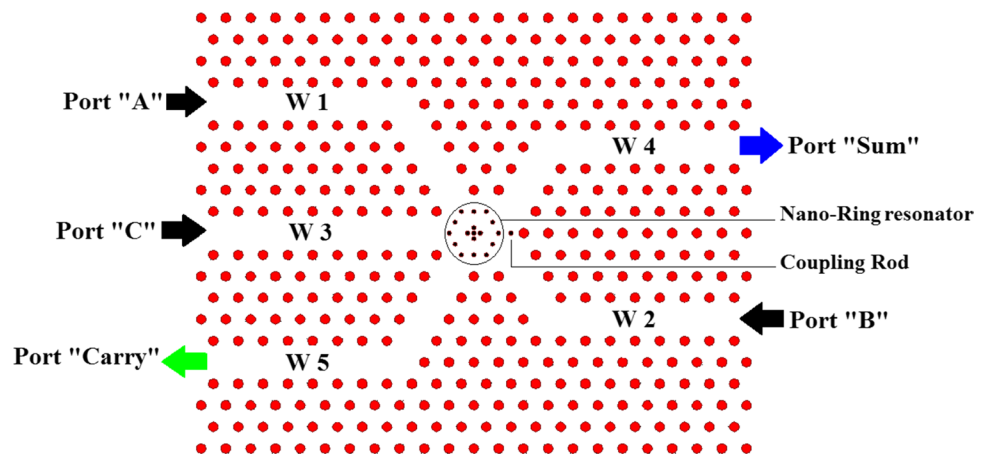


Table 2 A summary of the values of the parameters used for the proposed full-adder logic gate based on the PC-NRR

Parameter	Symbol	Quantity	Unit
Normalized bandgap (TM)	a/λ	0.285–0.480 0.575–0.595	–
Normalized bandgap (TE)	a/λ	0.830–0.890	–
Center wavelength	λ	1550	nm
Background refractive index	n_s	1	–
Refractive index of dielectric rods	n_r	3.46	–
Lattice constant	a	630	nm
Radius of dielectric rods	R	$0.2a$	nm
Radius of nanoring resonator rods	R_i	$0.04a$	nm
Radius of coupling rod	R_c	$0.04a$	nm
Length of waveguides (W1, W2, W4, and W5)	–	5.4	μm
Length of waveguide (W3)	–	6.1	μm
Width of waveguides (W1–W5)	–	1	μm
Footprint of the proposed structure	–	183	μm^2

3 Results and discussion

In the proposed structure, depending on the power P_{in} entering waveguides W1, W2, and W3 from the input ports A , B , and C , the power exiting the Carry and Sum output ports varies between 0 and 1. When analyzing the different logic states at the outputs obtained from the simulations, powers between 0% and 30% correspond to logic state 0 while those between 70% and 100% correspond to logic state 1. Thus, according to the electromagnetic field distribution profile shown in Fig. 4a, when the power entering waveguides W1 and W2 is 0 and the power entering waveguide W3 is P_{in} , or in other words, $A=0$, $B=0$, and $C=1$, the light coupled to the NRR is directed to the Sum output, and the Carry and Sum ports adopt logic state 0 and 1, respectively. In this case, the normalized power at a wavelength of 1550 nm for the Sum and Carry outputs is equal to $86\% P_{in}$ and $6\% P_{in}$, respectively. These results are also shown in Fig. 4b, c.

According to Fig. 5a, when the power entering waveguides W1 and W3 is 0 but the power entering waveguide W2 is P_{in} , i.e., $A=0$, $B=1$, and $C=0$, the Carry and Sum ports adopt the logic state 0 and 1, respectively, considering the presence of a single pulse coupled to the NRR. In this case, the normalized power at a wavelength of 1550 nm for the Sum and Carry output is equal to $89\% P_{in}$ and $7\% P_{in}$, respectively. These results are also shown in Fig. 5b, c.

According to Fig. 6a, when the power entering waveguides W2 and W3 is P_{in} but the power entering waveguide W1 is 0, i.e., $A=0$, $B=1$, and $C=1$, the Carry and Sum ports adopt logic state 1 and 0, respectively, considering the presence of two Gaussian pulses coupled simultaneously to the NRR. In this case, the normalized power at a wavelength of 1550 nm for the Sum and Carry outputs is $85\% P_{in}$ and $5.5\% P_{in}$, respectively. These results are also shown in Fig. 6b, c.

According to Fig. 7a, when the power entering waveguides W2 and W3 is 0 but the power entering waveguide W1 is P_{in} , i.e., $A=1$, $B=0$, and $C=0$, similar to the two first cases, the Carry and Sum ports adopt logic state 0 and 1, respectively, considering the presence of a single pulse coupled to the NRR. In this case, the normalized power at a wavelength of 1550 nm for the Sum and Carry outputs is equal to $92\% P_{in}$ and $4.5\% P_{in}$, respectively. These results are also shown in Fig. 7b, c.

According to Fig. 8a, when the power entering waveguides W1 and W3 is P_{in} and the power entering waveguide W2 is 0, i.e., $A=1$, $B=0$, and $C=1$, the Carry and Sum ports adopt logic state 1 and 0, respectively, considering the presence of two Gaussian pulses coupled to the NRR. In this case, the normalized power at a wavelength of 1550 nm for the Sum and Carry outputs is equal to $10.5\% P_{in}$ and $85\% P_{in}$, respectively. These results are also shown in Fig. 8b, c.

According to Fig. 9a, when the power entering waveguides W1 and W2 is P_{in} but the power entering waveguide W3 is 0, i.e., $A=1$, $B=1$, and $C=0$, the Carry and Sum ports adopt logic state 1 and 0, respectively, considering the presence of the two Gaussian pulses coupled to the NRR. In this case, the normalized power at a wavelength of 1550 nm for the Sum and Carry outputs is equal to $9.7\% P_{in}$ and $86\% P_{in}$, respectively. These results are also shown in Fig. 9b, c.

Finally, as shown in Fig. 10a, when the power entering waveguides W1, W2, and W3 is equal to P_{in} , i.e., $A=1$, $B=1$, and $C=1$, the Carry and Sum ports adopt logic state 1, considering the presence of the three Gaussian pulses coupled to the NRR. In this case, the NRR acts as a divider and the normalized power at a wavelength of 1550 nm for the Sum and Carry outputs is equal to $84.1\% P_{in}$ and $82\% P_{in}$, respectively. These results are also shown in Fig. 10b, c.

Note that, if the power entering waveguides W1, W2, and W3 is 0, there will be no output power due to the lack of

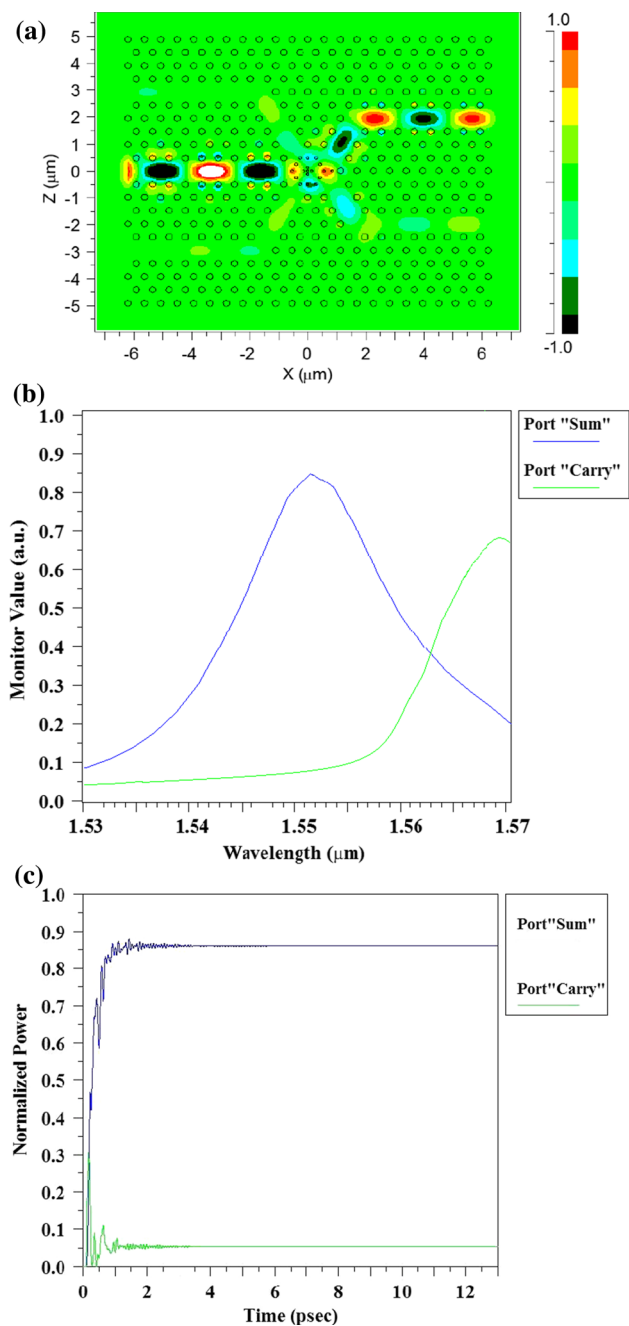


Fig. 4 The results for the all-optical full adder when $A=0$, $B=0$, and $C=1$: **a** the electromagnetic field, **b** the output intensity, and **c** the output power level

coupling of the optical pulse to the NRR, and the Sum and Carry ports will adopt logic state 0.

Table 3 presents the truth table describing the performance of the proposed full adder, including the various logic states, the power sent to each input and waveguide, the power received by each of the Sum and Carry outputs and their logic states, as well as the response time in each of these states. According to these results, the response

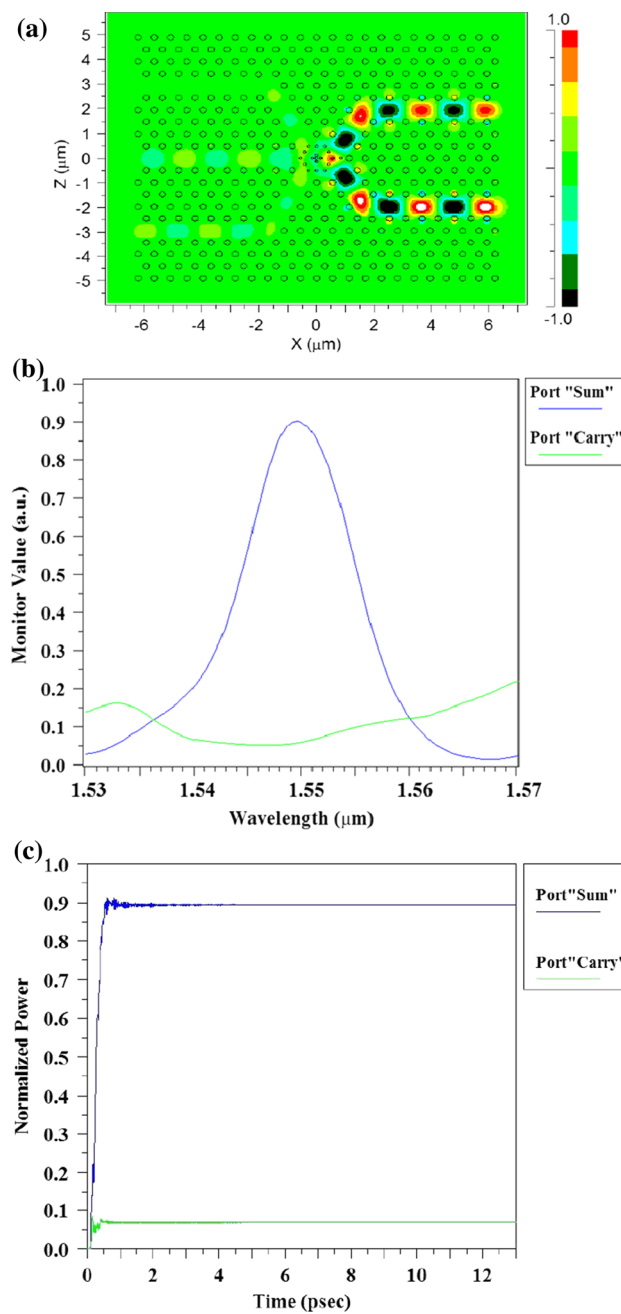


Fig. 5 The results for the all-optical full adder when $A=0$, $B=1$, and $C=0$: **a** the electromagnetic field, **b** the output intensity, and **c** the output power level

time of the proposed all-optical full-adder structure varies from 0.75 to 1.6 ps. Another important parameter in the design of all-optical logic gates is the contrast ratio, so the contrast ratio of 0 and 1 is also presented for each logic level. According to the following equation, the higher the power difference level between these two logic states, the better the performance of the logic gate [27].

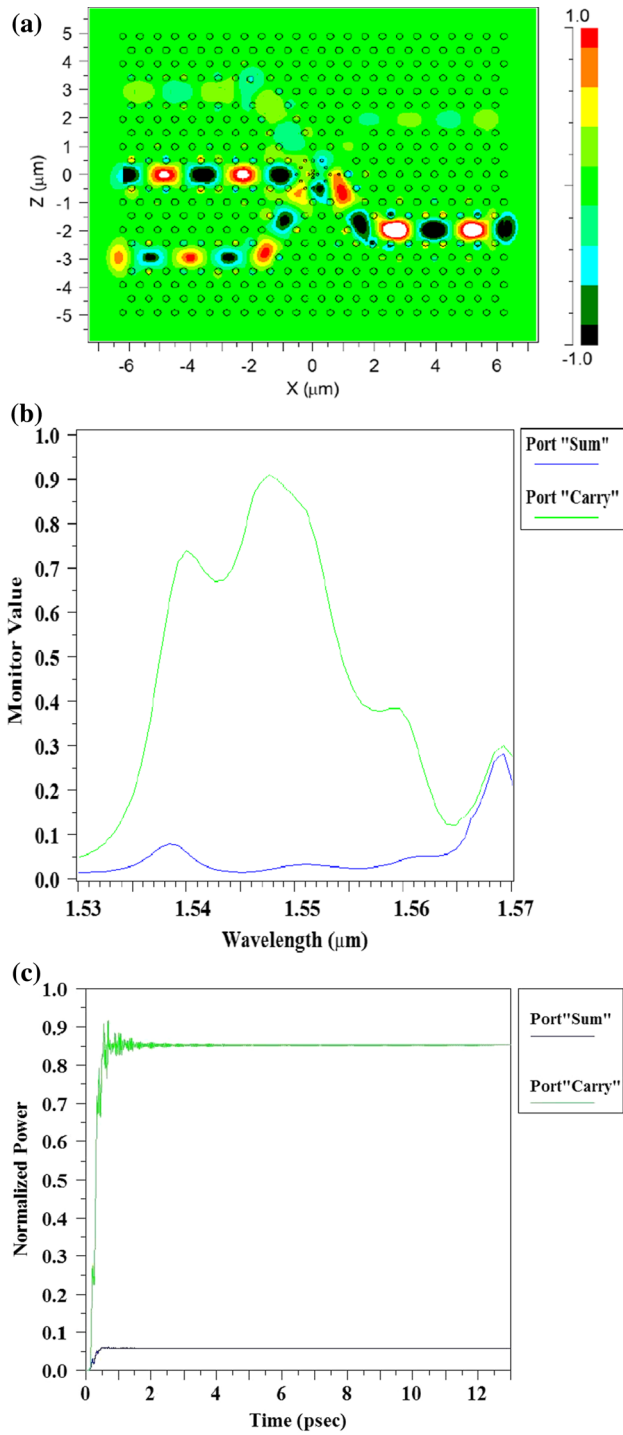


Fig. 6 The results for the all-optical full adder when $A=0$, $B=1$, and $C=1$: **a** the electromagnetic field, **b** the output intensity, and **c** the output power level

$$CR \text{ (dB)} = 10 \times \log \left(\frac{P_{\text{on}}}{P_{\text{off}}} \right),$$

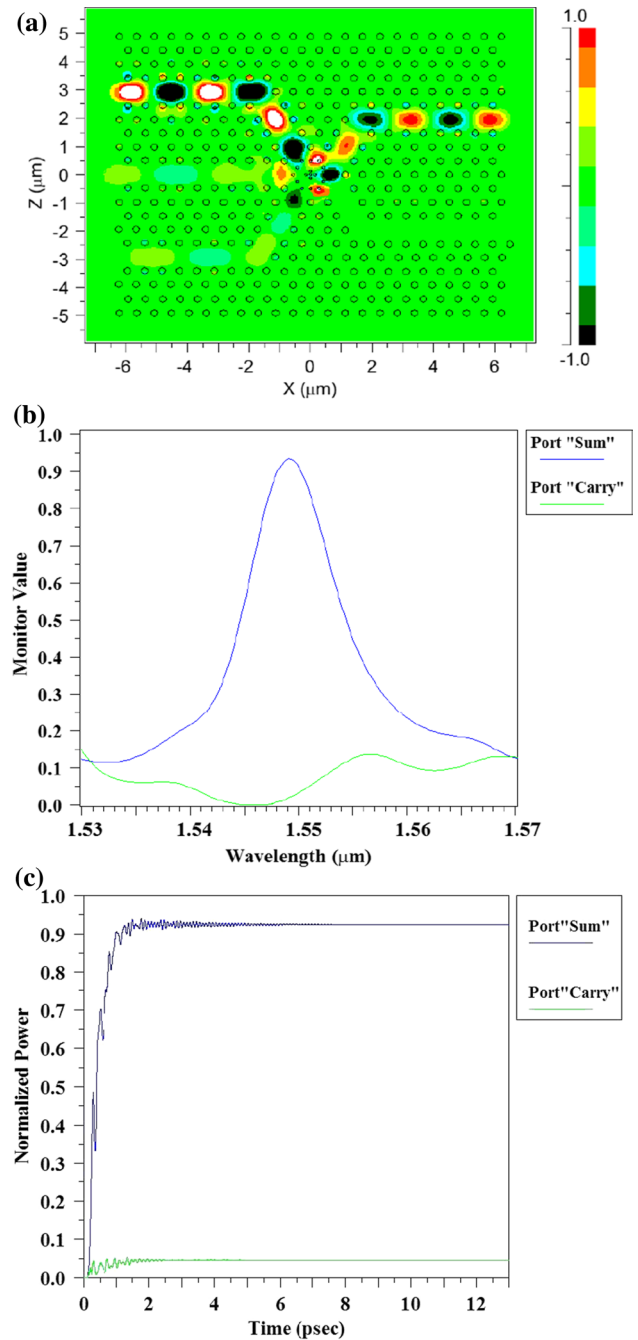


Fig. 7 The results for the all-optical full adder when $A=1$, $B=0$, and $C=0$: **a** the electromagnetic field, **b** the output intensity, and **c** the output power level

where P_{on} is the power in logic state 1 or ON state and P_{off} is the power in logic state 0 or OFF state. According to this equation, the CR for the Sum and Carry outputs is 9.03 and 10.68 dB, respectively, for the proposed structure.

Table 4 compares the important parameters of the proposed structure with other (full- and half-adder) logic

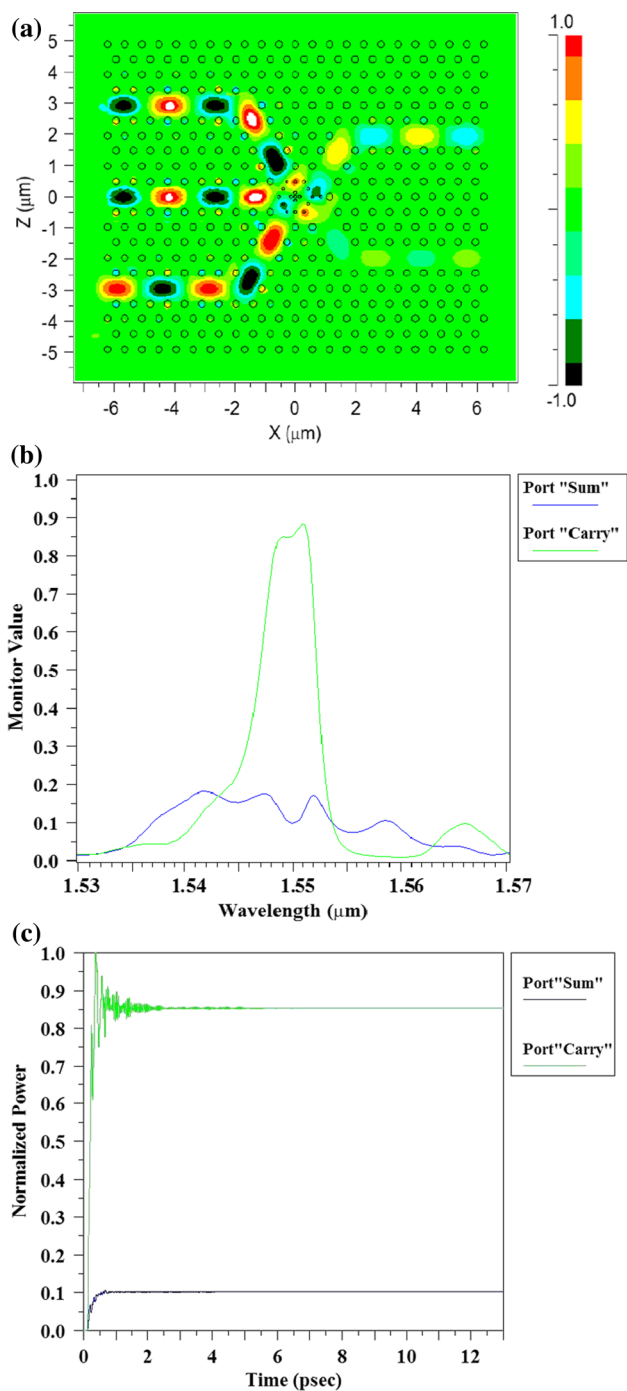


Fig. 8 The results for the all-optical full adder when $A=1$, $B=0$, and $C=1$: **a** the electromagnetic field, **b** the output intensity, and **c** the output power level

gates presented in recent years. According to this table, the response time and output CR of the proposed logic gate are highly desirable compared with those of structures

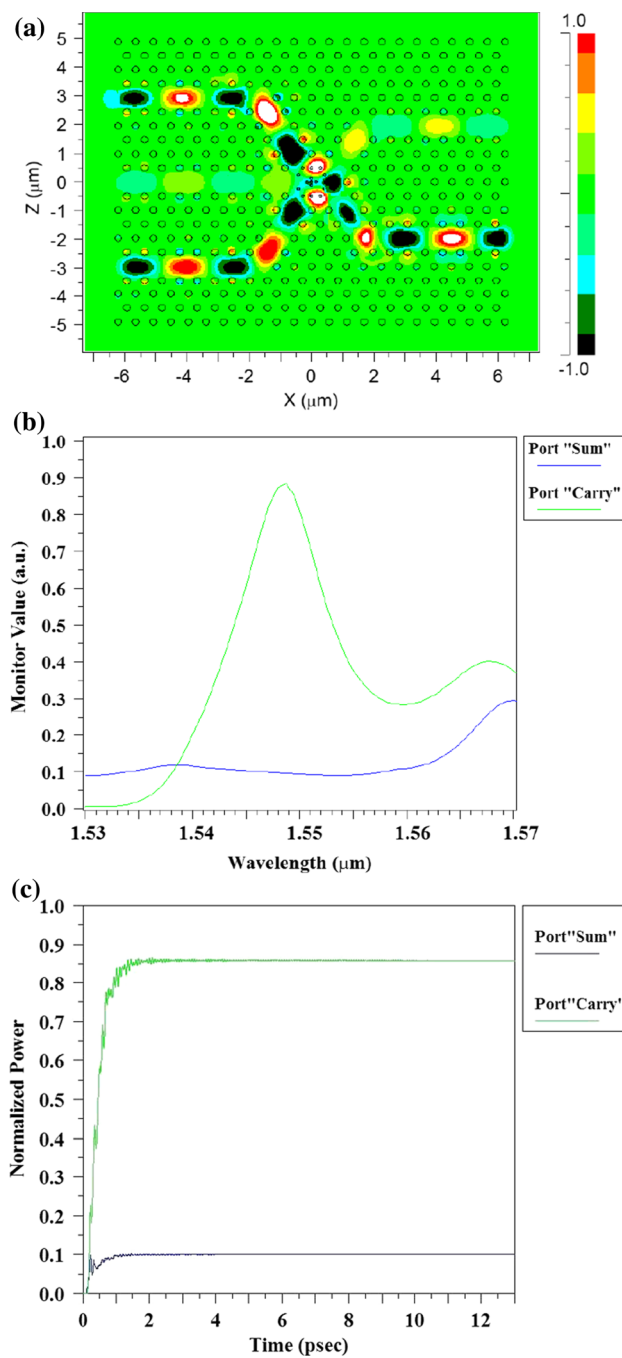


Fig. 9 The results for the all-optical full adder when $A=1$, $B=1$, and $C=0$: **a** the electromagnetic field, **b** the output intensity, and **c** the output power level

presented in recent years. Additionally, the structure proposed herein is highly applicable due to the use of the interference principle between the waveguides and NRR, its very small structural size, as well as not requiring a

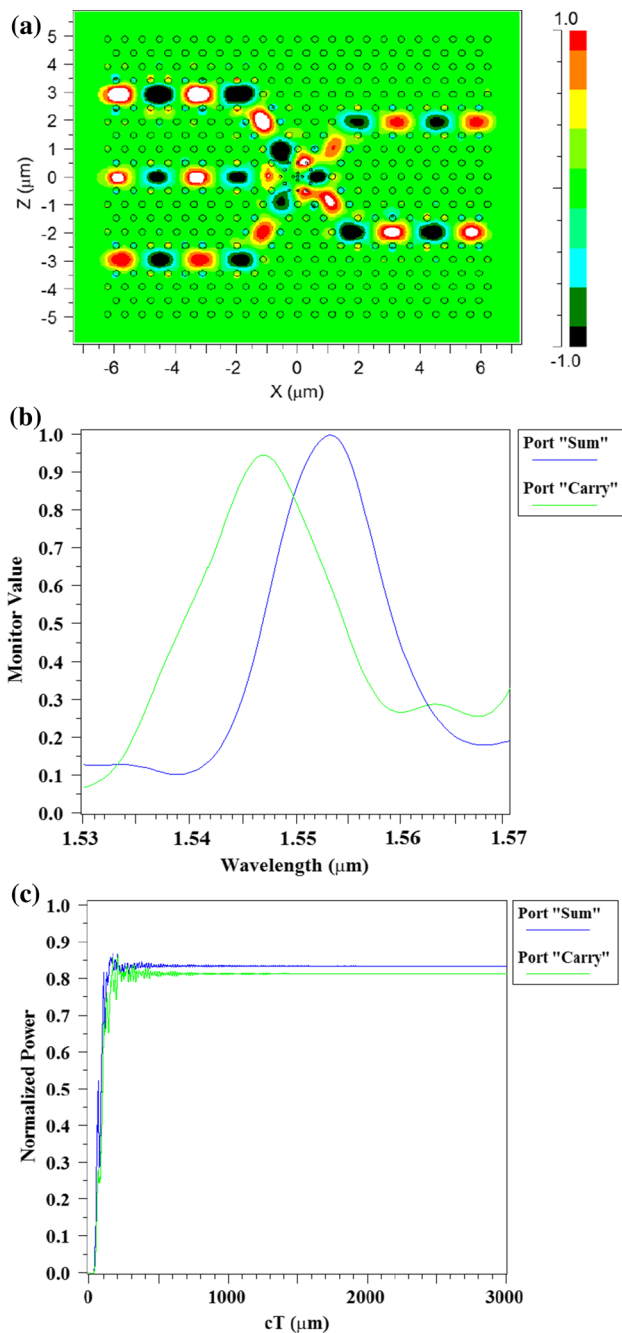


Fig. 10 The results for the all-optical full adder when $A=1$, $B=1$, and $C=1$: **a** the electromagnetic field, **b** the output intensity, and **c** the output power level

Table 3 The simulation results for the proposed structure

Input ports			Normalized output ports		
A	B	C	Carry (%)	Sum (%)	Response time (ps)
0	0	0	0	0	***
0	0	P_{in}	6	86	1.2
0	P_{in}	0	7	89	0.75
0	P_{in}	P_{in}	85	5.5	1
P_{in}	0	0	4.5	92	1.6
P_{in}	0	P_{in}	86	10.5	1
P_{in}	P_{in}	0	86	9.7	1.2
P_{in}	P_{in}	P_{in}	82	84.1	1

***This parameter is not discussed in the article

change in the refractive index of materials. The maximum output delay of the proposed structure is 1.1 ps, which is very good compared with structures proposed in recent years.

4 Conclusions

We propose and design an all-optical full adder using a hexagonal NRR and five waveguides. In this design, the NRR between the waveguides controls the output parameters, depending on the refractive index and radius of the internal coupling rods as well as their relative positioning. The input Gaussian pulse enters the structure through three waveguides (W1, W2, and W3), and based on the principle of interference between the waveguides and NRR, the output power exits in various states from the output ports. Additionally, the management of the power entering the waveguides W1, W2, and W3 controls the power exiting the Carry and Sum ports between 0 and 1, corresponding to the OFF and ON states. The response time of the proposed full-adder structure varies from 0.75 to 1.6 ps. The maximum output delay of the proposed structure is 1.6 ps, and the CR for the Carry and Sum ports is 10.68 and 9.03 dB, respectively. To optimize the output parameters of the proposed structure, the interference effect in the PC is used, thereby simplifying its design.

Table 4 A comparison of the proposed full adder with recently reported devices

Ref	Logic gates type	Mechanism	Response time (ps)	CR (dB)	Footprint (μm^2)
[34]	Half adder	Interference	4	6.98	1054
[35]	Half adder	Nonlinear	1.5	***	***
[36]	Half adder	Self-collimation	***	4.81	169
[37]	Half adder	Interference	0.22	8.22	137
[38]	Half adder	Nonlinear	3	***	303
[29]	Full adder	Nonlinear	2	***	***
[27]	Full adder	Nonlinear	1.6	***	345
[30]	Full adder	Nonlinear	8	***	396
[21]	Full adder	Nonlinear	2	***	439
[31]	Full adder	Nonlinear	3	***	***
[24]	Full adder	Interference	2	11	72
Our structures	Full adder	Interference	1.1	9.03	183

***This parameter is not discussed in the article

Acknowledgements This work was supported by Shahid Rajaei Teacher Training University.

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