Journal of Computational Electronics (2020) 19:1433–1443
https://doi.org/10.1007/s10825-020-01540-3

Study of the electrical parameters of a dual-material double-gate TFET using a strained type II staggered $Ge_{1-x-y}Si_xSn_y/Ge_{1-a-b}Si_aSn_b$ heterojunction

Namrata Shaw[1] · Bratati Mukhopadhyay[1] · Gopa Sen[1]

Published online: 30 June 2020

Abstract
A strained $Ge_{1-x-y}Si_xSn_y/Ge_{1-a-b}Si_aSn_b$ direct type II staggered heterojunction *n*-channel tunneling field-effect transistor (FET) with a dual-material double gate is proposed herein. A high-*K* gate dielectric is used to improve the overall device performance. The energy bandgap for strained $Ge_{1-x-y}Si_xSn_y$ grown on a relaxed $Ge_{1-a-b}Si_aSn_b$ layer is determined using the generalized approach of Menendez and Kouvetakis (MK). Poisson's equation is solved by using a parabolic approximation to determine the surface potential and electric field. The drain current is calculated using the tunneling generation rate obtained from Kane's model. A significant improvement of the drain current is observed as compared with that of previously reported Si-based TFETs.

Keywords Band-to-band tunneling · Drain current · SCE · Strained DGTFET

1 Introduction

Aggressive downscaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) to achieve higher packing densities and increased values of the ON-current I_{ON} leads to severe degradation of the device performance due to short-channel effects (SCEs) such as drain-induced barrier lowering (DIBL), leakage current, etc. [1]. The subthreshold swing of such devices is also restricted to 60 mV/decade at room temperature [2], which results in power dissipation problems when used in nanoscale circuits. To overcome such limitations, alternative devices with a reduced subthreshold swing must be explored to achieve higher ON-currents and reduced leakage currents for use in low-power applications [3–5].

The TFET uses band-to-band tunneling for carrier transport across the junctions instead of the conventional drift–diffusion current mechanism in MOSFETs. This makes it suitable for use in low-power applications. The TFET device has a built-in tunnel barrier that prevents SCEs and helps to achieve subthreshold swing values below the 60 mv/decade threshold [5–7]. Also, there is scope to improve the overall device characteristics of TFETs by simultaneously optimizing the I_{ON}, I_{OFF}, V_T, subthreshold slope, nature of the output characteristic, and immunity against SCEs, especially DIBL effects [8].

However, TFETs also suffer from certain drawbacks such as low I_{ON} as compared with conventional MOSFETs and ambipolar issues when used in switching applications. Also, device reliability can be a major concern, as TFET devices suffer from degradation of the device performance in terms of the drain current and threshold voltage due to the presence of interface traps and oxide charges at the gate dielectric–channel interface near the source–channel region [9]. The performance of TFETs can be improved by improving their I_{ON} and overcoming the ambipolar issues, which can be achieved by structural or material engineering of the device architecture. Recently, several structural modifications have been observed to address the shortcomings of the conventional TFET. A gate–source overlap with the addition of an Esaki tunneling diode in the source region of a TFET device is seen to improve the I_{ON}/I_{OFF} ratio and reduce the ambipolarity and leakage current [10]. The performance of conventional TFETs is seen to be greatly improved by modifying the channel shape (e.g., by using a T-shaped channel) and the positioning of the drain [11]. The

✉ Namrata Shaw
namrata.shaw05@gmail.com

[1] Institute of Radio Physics and Electronics, University of Calcutta, 92, A.P.C Road, Kolkata, West Bengal 700009, India

scaling limitations of TFET devices (due to the emergence of SCEs) can be overcome by introducing a ground plane into the buried oxide of silicon-on-insulator (SOI) TFETs [12]. The addition of a source pocket at the source–channel interface greatly improves the ON current [13]. The use of heterojunctions in junctionless TFETs can improve the overall device performance and allow their use in digital applications [14]. The strained double-gate TFET (DGTFET) using dual-material and high-K dielectric has also shown encouraging results [15–17]. The use of a narrower-bandgap material also greatly improves the I_{ON} [19].

Dramatic improvements have been achieved in this field over the last 10–15 years, including the successful growth of GeSn [20] and the discovery of practical chemical vapor deposition (CVD) routes to high-quality $Ge_{1-x}Sn_x$ films and alloys of GeSiSn directly on Si substrates [21–25].

An interesting feature of this alloy is the crossover observed from an indirect to direct bandgap when the Sn concentration in the alloy exceeds 8% [26–28]. A material with a direct nature can also be obtained by applying strain. All the layers and virtual substrates (VS) can be grown on a Si substrate, highlighting the possibility of integrating the electronics and photonics onto a Si platform. It has also been proved that a type II direct bandgap configuration can be realized by using a strained GeSiSn layer with Sn content below 25% [29]. This type II direct bandgap can lead to significant band-to-band tunneling (BTBT) even at low voltages. Also, heterojunctions with such type II staggered band alignment have been shown to boost the performance [30, 31] of TFETs based on GeSiSn alloy.

Material engineering using new and novel materials must be combined with structural engineering to obtain devices with optimum performance. A heterojunction n-channel TFET built with a direct bandgap type II staggered strained $Ge_{1-x-y}Si_xSn_y$/$Ge_{1-ab}Si_aSn_b$ junction is proposed herein. The $Ge_{1-x-y}Si_xSn_y$ layer is strained, whereas the $Ge_{1-a-b}Si_aSn_b$ layer is relaxed. The method used to calculate the energy bands is a generalization of Van de Walle's approach along with the inclusion of the strain-dependent spin–orbit Hamiltonian [25]. An analytical model for the above-mentioned device is derived by solving the two-dimensional (2-D) Poisson equation using the parabolic approximation technique. The surface potential and electric field are thus obtained using appropriate boundary conditions. The drain current is also obtained using the generation rate derived from Kane's band-to-band tunneling generation rate model [32–34].

2 Theory

2.1 Device structure

A schematic of the structure of the proposed device is shown in Fig. 1. The p-type source and n-type drain are considered to have doping concentrations of $10^{20}/cm^3$ and $5\times10^{18}/cm^3$, respectively. The use of a lower doping concentration on the drain side ensures a lower OFF-current, while the higher source doping provides a higher ON-current due to the increased bandgap narrowing at the tunneling junction [18]. On the other hand, the channel doping concentration is chosen as $10^{17}/cm^3$ to enhance the carrier mobility. Being an n-channel device, tunneling occurs at the source side of the source–channel interface. A high-K gate dielectric HfO_2 ($K=25$) is used to reduce the gate leakage. Two gate metals M1 and M2 have different work functions of 4 eV and 4.4 eV, respectively. Initially there is no band overlap on the source side, but with an increase of the gate voltage, carriers tunnel from the valence band of the heavily doped p-type source to the conduction band of the nearly intrinsic channel and then move towards the n-doped drain by the drift–diffusion mechanism.

2.2 Bandgap calculation

The energy band structure at the Γ and L points of the conduction band in the $Ge_{1-x-y}Si_xSn_y$ layer grown on $Ge_{1-a-b}Si_aSn_b$ is calculated using a generalization of the Menendez and Kouvetakis (MK) [25] approach. It is assumed that there is a reference level within each semiconductor and that this level lines up when a heterostructure is formed. This alignment process of the reference levels gives the offset $\Delta E_{V,av}$ for the *average* of the three top valence bands in the actual materials. In the

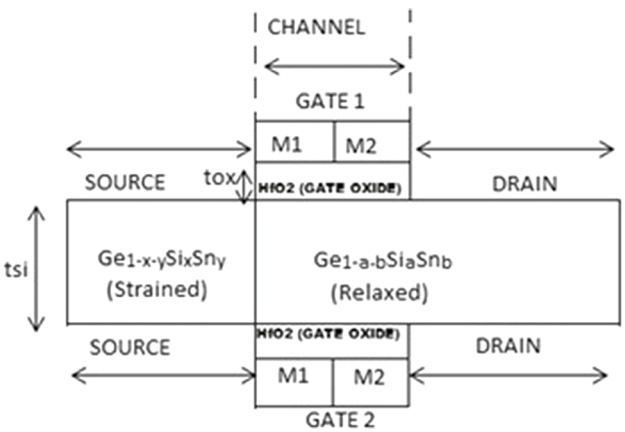

Fig. 1 A schematic diagram of the n-channel strained $Ge_{1-x-y}Si_xSn_y$/$Ge_{1-a-b}Si_aSn_b$ DG-TFET

strain-dependent spin–orbit Hamiltonian introduced by Chandrasekhar and Pollak [37], the Menendez and Kouvetakis (MK) [25] and Van de Walle [38] approaches are also included. The expressions for the band edges of a (001)-oriented $Ge_{1-x-y}Si_xSn_y$ layer lattice-matched to a relaxed $Ge_{1-a-b}Si_aSn_b$ layer are given by

$$E_{V\Gamma}(x,y) = -\frac{\Delta_0(a,b)}{3} - E_{V,av}(a,b) - \frac{\Delta_0(x,y)}{6} + \partial E_h^o + \frac{1}{4}\partial E_{001} + \frac{1}{2}\sqrt{(\Delta_0(x,y) + \frac{1}{2}\partial E_{001})^2 - 2(\partial E'_{001})^2}, \quad (1a)$$

$$E_C\Gamma(x,y) = E_V\Gamma(x,y) + E_0(x,y) + \partial E_h^C\Gamma, \quad (1b)$$

$$E_{CL}(x,y) = E_{V\Gamma}(x,y) + E_{ind}(x,y) + \partial E_h^{CL} \quad (1c)$$

where Δ_0 is the spin–orbit splitting. Here, $E_{V\Gamma}(x,y)$ is the highest valence band in the strained $Ge_{1-x-y}Si_xSn_y$ layer, and $E_{C\Gamma}(x,y)$ and $E_{CL}(x,y)$ are the conduction-band edge at the Γ and L point, respectively.

The shear components of the strain have a significant effect on the degenerate bands; they lead to splitting of the valence bands. The splitting of the energy subbands averages out to obtain $E_{V,av}$. Even when no shear strain is present, valence-band splitting occurs due to the spin–orbit effect and the topmost valence band is given by $E_V = E_{V,av} + \frac{\Delta_0}{3}$..

When strained layers are grown on a substrate, the shear components of the strain lead to additional splitting of the bands, which interacts further with the spin–orbit splitting to produce the final valence-band position. This effect is reflected in the difference of the spin–orbit splitting of the layer $\frac{\Delta_0(x,y)}{3}$ and the substrate $\frac{\Delta_0(a,b)}{3}$ [29].

$E_0(x,y)$ is the direct bandgap of $Ge_{1-x-y}Si_xSn_y$at the Γ point and $E_{ind}(x,y)$ is the indirect Γ–L bandgap, given as

$$E^n(x,y) = E^n_{Ge}(1-x-y) + xE^n_{Si} + yE^n_{Sn} - b_{GeSi}x(1-x-y) - b_{GeSn}y(1-x-y) - b_{SiSn}xy. \quad (2)$$

The indirect bandgap energy is calculated according to Vegard's law by using the values of the bowing parameters presented in Table 1. The strain shifts $\partial E_{001}, \partial E'_{001}, \partial E_h^V, \partial E_c^{C\Gamma}$ and ∂E_C^{CL} are calculated from Menendez and Kouvetakis (MK) [25] and Chuang et al. [35]. The lattice constants of the ternary alloys are calculated using the following equation:

$$a(x,y) = a_{Ge}(1-x-y) + (x)a_{Si} + (y)a_{Sn} + b'_{GeSn}(y)(1-x-y) + b'_{SiGe}(x)(1-x-y) - b'_{SiSn}(y)(x) \quad (3)$$

The lattice constant is used to calculate the strain as $e_{\parallel} = \frac{[a(a,b)-a(x,y)]}{a(x,y)}$ [25].

Table 1 The parameter values for Si, Ge, and Sn

Parameter	Si	Ge	Sn
$E_{g\Gamma}$ (eV)	4.185	0.805	− 0.413
E_{gL} (eV)	1.65	0.664	0.092
Δ_0 (eV)	0.044	0.30	0.8
E_{vav} (eV)	0.69	0	− 0.48
A (Å)	5.4307	5.6537	6.4892
C_{11} (GPa)	165.77	128.53	69
C_{12} (GPa)	63.93	48.26	29.3
a_V (eV)	2.46	1.24	1.58
a_C (eV)	10.06	− 8.24	− 6.00
a_L (eV)	− 0.66	− 1.54	− 2.14
b_V (eV)	− 2.1	− 2.9	− 2.7
E (eV) (L valley)	2.0	0.66	0.14
E (eV) (Γ valley)	4.06	0.795	− 0.413
e_r	11.9	16.2	24.0
Bandgap bowing parameters (in eV)			
	b_{SiGe}	b_{GeSn}	b_{SiSn}
Γ valley	0.21	2.1	13.2
L valley	0	0.91	0
Lattice bowing parameters			
	b'_{SiGe}	b'_{GeSn}	b'_{SiSn}
	−0.026	0.166	0

The lattice constants of Ge, Si, and Sn, the lattice bowing parameters, and the deformation potentials used to calculate the strain and strain shifts are presented in Table 1.

Using Eqs. (1)–(3), the various concentrations of Ge, Si, and Sn in the ternary alloy giving type II, direct, and staggered band alignment are obtained and presented in Table 2. We choose the composition which gives rise to type II band alignment [29]. This improves the band-to-band tunneling rate in the proposed device, as the tunneling barrier width is reduced, thereby improving the ON current as seen below. The mole fractions providing the optimum device performance are selected to obtain the desired results.

2.3 Calculation of the drain current

For the calculation of the drain current, the following assumptions are made:

- The surface potential at the source end is equal to the difference between the Fermi level of the *p*-type source and the intrinsic Fermi level.

Table 2 The values of x, y, a, and b to achieve a direct bandgap type II $Ge_{1-x-y}Si_xSn_y/Ge_{1-a-b}Si_aSn_b$ heterojunction

Si , x (%)	Sn, y (%)	Ge, z (%)	Si , a (%)	Sn, b (%)	Ge, c (%)	Strain (%)	ΔE_C (in eV)	ΔE_V (in eV)	E_g (in eV)
0.01	0.04	0.95	0.47	0.18	0.35	1.98	0.4444	0.0471	0.5013
0.01	0.06	0.93	0.41	0.21	0.38	1.94	0.1663	0.003	0.4453
0.02	0.06	0.92	0.42	0.21	0.37	1.99	0.1586	0.0046	0.4648
0.01	0.01	0.98	0.70	0.23	0.07	1.94	0.3036	0.1785	0.5985
0.01	0.04	0.95	0.52	0.23	0.25	1.72	0.1235	0.0884	0.5282
0.01	0.06	0.93	0.43	0.23	0.34	1.76	0.0516	0.0267	0.4632

- The potential drop in the depletion region of the source is negligible, and the potential in the source region is uniform.
- The source–channel and drain–channel depletion regions are free from mobile charge.
- Trap charges are taken as zero.

The analytical model for the proposed device structure is derived by solving the 2-D Poisson's equation

$$\frac{\delta^2\Psi(x,y)}{\partial x^2}+\frac{\delta^2\Psi(x,y)}{\partial y^2}=0. \tag{4}$$

The potential profile in the vertical direction is assumed to be a second-order polynomial [36]

$$\Psi(x,y)=a_O(x)+ya_1(x)+y^2a_2(x). \tag{5}$$

The boundary conditions in the channel region are:

(a) The electric flux at the front-oxide gate interface is continuous for the dual-material gate TFET, so

$$\frac{\mathrm{d}\Psi_1(x,y)}{\mathrm{d}y}=\varepsilon_{ox}\frac{\Psi_{S1}(x)-\varphi_{g1}}{\varepsilon_{Si}t_{ox}} \text{ under M1 at } y=0,$$

$$\frac{\mathrm{d}\Psi_2(x,y)}{\mathrm{d}y}=\varepsilon_{ox}\frac{\Psi_{S2}(x)-\varphi_{g2}}{\varepsilon_{Si}t_{ox}} \text{ under M2 at } y=0,$$

where $\varphi_{g1}=V_{gs}-\phi_{M1}+\chi+{}^{E_g}\!/_2$,

$\varphi_{g2}=V_{gs}-\phi_{M2}+\chi+{}^{E_g}\!/_2$.

(b) The electric flux at the back gate oxide and the back channel interface is continuous for both materials:

$$\frac{\mathrm{d}\Psi_1(x,y)}{\mathrm{d}y}=\varepsilon_{ox}\frac{\varphi_{g1}-\Psi_{S1}(x)}{\varepsilon_{Si}t_{ox}} \text{under M1 at } y=t_{Si},$$

$$\frac{\mathrm{d}\Psi_2(x,y)}{\mathrm{d}y}=\varepsilon_{ox}\frac{\varphi_{g2}-\Psi_{S2}(x)}{\varepsilon_{Si}t_{ox}} \text{ under M2 at } y=t_{Si}.$$

(c) The potential at the source and drain end is given as

$$\Psi_1(x,y)=\Psi_{S1}(0)=V_{bi}=\frac{-KT}{q}\ln\frac{N_{Source}}{N_i},$$

$$\Psi_2\left(l_1+l_2,0\right)=\Psi_{S2}\left(l_1+l_2\right)=V_{bi1}+V_{DS},$$

$$V_{bi1}=\frac{-KT}{q}\ln\frac{N_{Drain}}{N_i},$$

where V_{bi} is the built-in potential, ϕ_{M1} and ϕ_{M2} are the work functions of the gate metals, E_g is the bandgap energy, q is the elementary charge, V_{GS} is the gate–source voltage, V_{DS} is the drain–source voltage, ε_{Si} is the relative permittivity of GeSiSn, and ε_{ox} is the relative permittivity of HfO_2.

The 2-D potential under M1 and M2 can be obtained as

$$\Psi_1(x,y)=\Psi_{S1}(x)+a_{11}(x)y+a_{12}(x)y^2\ 0\le x\le l_1, \tag{6a}$$

$$\Psi_2(x,y)=\Psi_{S2}(x)+a_{21}(x)y+a_{22}(x)y^2\ l_1\le x\le l_1+l_2. \tag{6b}$$

The values of the above constants are given as follows:

$$a_{11}(x)=\varepsilon_{ox}\frac{\Psi_{S1}(x)-\varphi_{g1}}{\varepsilon_{Si}t_{ox}}, \tag{7a}$$

$$a_{12}(x)=\varepsilon_{ox}\frac{\varphi_{g1}-\Psi_{S1}(x)}{t_{Si}\varepsilon_{Si}t_{ox}}, \tag{7b}$$

$$a_{21}(x)=\varepsilon_{ox}\frac{\Psi_{S2}(x)-\varphi_{g2}}{\varepsilon_{Si}t_{ox}}, \tag{7c}$$

$$a_{22}(x)=\varepsilon_{ox}\frac{\varphi_{g2}-\Psi_{S2}(x)}{t_{Si}\varepsilon_{Si}t_{ox}}. \tag{7d}$$

Thus, we get

$$\Psi_1(x,y)=\Psi_{S1}(x)+\varepsilon_{ox}\frac{\Psi_{S1}(x)-\varphi_{g1}}{\varepsilon_{Si}t_{ox}}y+\varepsilon_{ox}\frac{\varphi_{g1}-\Psi_{S1}(x)}{t_{Si}\varepsilon_{Si}t_{ox}}y^2, \tag{8a}$$

$$\Psi_2(x,y) = \Psi_{S2}(x) + \varepsilon_{ox}\frac{\Psi_{S2}(x)-\varphi_{g2}}{\varepsilon_{Si}t_{ox}}y + \varepsilon_{ox}\frac{\varphi_{g2}-\Psi_{S2}(x)}{t_{Si}\varepsilon_{Si}t_{ox}}y^2. \tag{8b}$$

Solving the Poisson's equation, we obtain the surface potential under M1 and M2 as

$$\frac{d^2\Psi_{S1}(x)}{dx^2} - \frac{2\varepsilon_{ox}}{t_{Si}\varepsilon_{Si}t_{ox}}\Psi_{S1}(x) = \frac{2\varepsilon_{ox}}{t_{Si}\varepsilon_{Si}t_{ox}}\varphi_{g1}, \tag{9a}$$

$$\frac{d^2\Psi_{S2}(x)}{dx^2} - \frac{2\varepsilon_{ox}}{t_{Si}\varepsilon_{Si}t_{ox}}\Psi_{S2}(x) = \frac{2\varepsilon_{ox}}{t_{Si}\varepsilon_{Si}t_{ox}}\varphi_{g2}. \tag{9b}$$

Solving the above second-order differential equation yields

$$\Psi_{S1}(x) = B_1 e^{px} + C_1 e^{-px}\varphi_{g1}\,, \tag{10a}$$

$$\Psi_{S2}(x) = B_2 e^{px} + C_2 e^{-px}\varphi_{g2}, \tag{10b}$$

where $p^2 = \frac{2\varepsilon_{ox}}{t_{Si}\varepsilon_{Si}t_{ox}}$,

where χ is the electron affinity and p is the characteristic length.

The coefficients B_1, C_1, B_2, and C_2 are

$$B_1 = \frac{V_{bi1} + V_{DS} + \varphi_{g2} - (\varphi_{g2}-\varphi_{g1})\cos(pl_2) - e^{-p(l_1+l_2)} + (\varphi_{g1}+V_{bi})}{(2\sinh(p(l_1+l_2)))}, \tag{11a}$$

$$C_1 = V_{bi} + \varphi_{g1} - B_1, \tag{11b}$$

$$B_2 = B_1 - \left(\frac{\varphi_{g1}-\varphi_{g2}}{2e^{pl_1}}\right), \tag{11c}$$

$$C_2 = C_1 + \left(\frac{\varphi_{g2}-\varphi_{g1}}{2e^{-pl_1}}\right). \tag{11d}$$

Differentiating the surface potential along the channel length gives the electric field distribution.

The lateral electric field is

$$\Xi_{x1}(x) = -\frac{d}{dx}(\Psi_{S1}(x)) = B_1 p e^{px} + C_1 p e^{-px} \text{ where } 0 \le x \le l_1, \tag{12a}$$

$$\Xi_{x2}(x) = -\frac{d}{dx}(\Psi_{S2}(x)) = B_2 p e^{px} + C_2 p e^{-px} \text{ where } l_1 \le x \le l_1 + l_2. \tag{12b}$$

The vertical electric field is

$$\Xi_{y1}(x) = \frac{d}{dy}(\Psi_1(x,y)) = -(a_{11}(x) + 2a_{12}(x)y) \text{ where } 0 \le x \le l_1, \tag{13a}$$

$$\Xi_{y2}(x) = \frac{d}{dy}(\Psi_2(x,y)) = -(a_{21}(x) + 2a_{22}(x)y) \text{ where } l_1 \le x \le l_1 + l_2. \tag{13b}$$

The tunneling generation rate $G(\Xi)$ is calculated from Kane's model [32, 33] as

$$G(\Xi) = A_{Kane}|\Xi|^2 e^{\frac{-B_{Kane}}{|\Xi|}},$$

where $|\Xi| = \sqrt{\Xi_x^2 + \Xi_y^2}$ is the magnitude of the electric field and A_{Kane} and B_{Kane} are Kane's parameters.

The value of Kane's parameters, which are dependent on the reduced tunneling mass and bandgap, are taken as

$$A_{Kane} = 2.3334 \times 10^{22}\ \text{m}^{-1}\ \text{V}^{-2}\ \text{s}^{-1},$$

$$B_{Kane} = 2.9541 \times 10^{2}\ \text{MV/m}.$$

In a DG-TFET, electrons undergo BTBT from the valence band of the source to the conduction band of the channel region. The total drain current I_D per unit length can be obtained by integrating the band-to-band generation rate over the volume of the device [34]:

$$I_D = q\iint G(\Xi)dxdy, \tag{14}$$

where q is the electronic charge.

3 Results and discussion

The proposed analytical model is implemented for a device with a channel length of 20 nm. The device has a body thickness of 10 nm and an equivalent oxide thickness (EOT) of ~ 1 nm.

Figure 2 shows the band alignment at the strained $Ge_{1-x-y}Si_xSn_y/Ge_{1-a-b}Si_aSn_b$ interface.

The analytical model derived herein is first applied to an Si-based DG-TFET, and the results are compared with data previously reported by Garg et al. [39] by using the same parameter values as those of the Si-based DG-TFET studied by Garg et al. [39]. Figure 3 illustrates the transfer characteristic of the Si-based TFET. Good agreement is seen between the results obtained using the theoretical model described herein and the simulation results of Garg et al. [39]. The

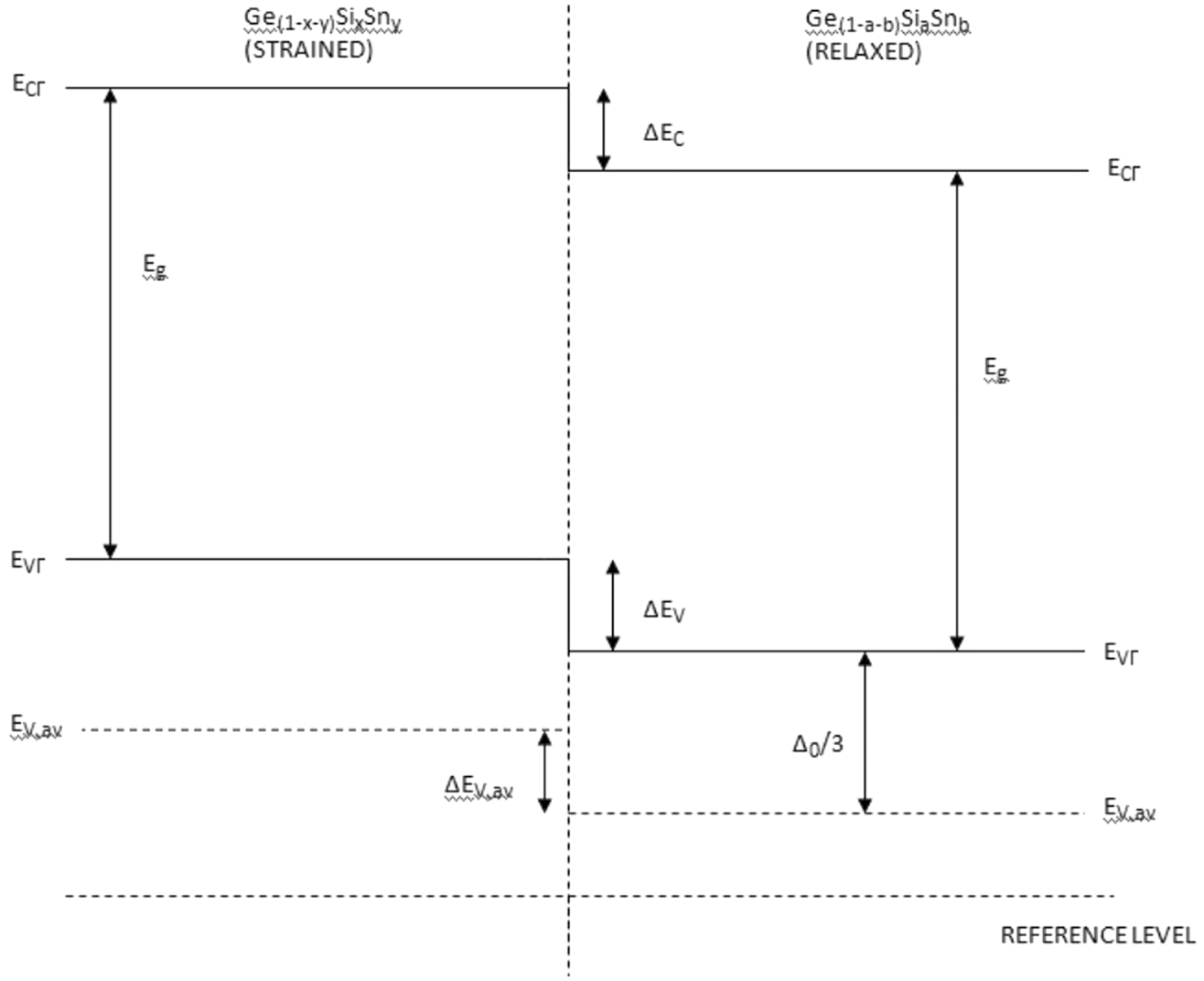

Fig. 2 Band alignments at the strained $Ge_{(1-x-y)}Si_xSn_y/Ge_{(1-a-b)}Si_aSn_b$ Interface

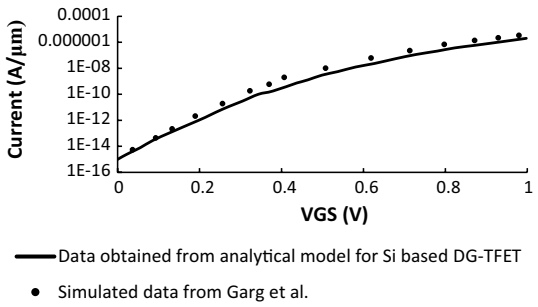

Fig. 3 The transfer characteristics for the Si-based DG-TFET

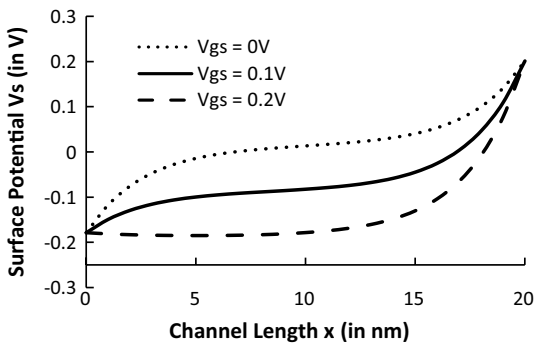

Fig. 4 The variation of the surface potential V_S for different V_{GS} values at $V_{DS} = 0.1$ V

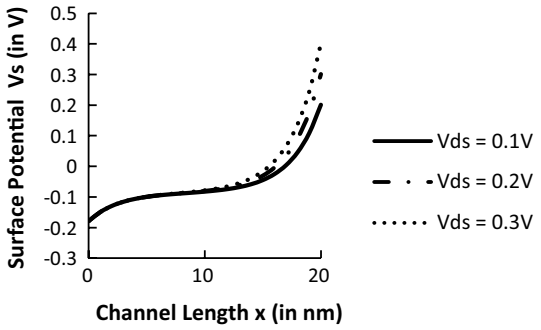

Fig. 5 The variation of the surface potential V_S for different V_{DS} values at $V_{GS}=0.1$ V

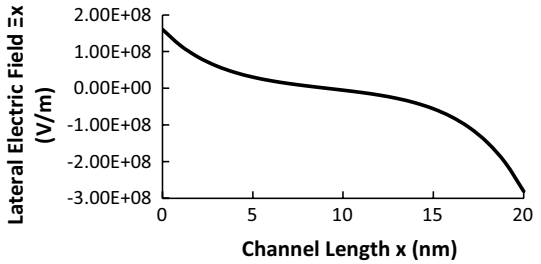

Fig. 6 The variation of the lateral electric field Ξ_x along the channel length

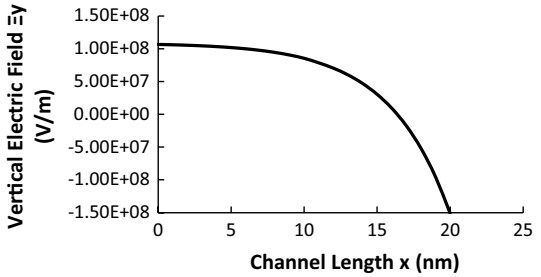

Fig. 7 The variation of the vertical electric field Ξ_y along the channel length

model is thus validated and is now implemented on the proposed device structure.

Figure 4 illustrates the variation of the surface potential along the channel length at different gate voltages with a constant drain–source voltage. The surface potential varies significantly with the gate–source voltage. There is a reduction in the surface potential in the channel region with increasing gate voltage. For a higher gate–source voltage, the slope of the surface potential is sharper, indicating a greater tunneling current on the source side.

Figure 5 illustrates the variation of the surface potential along the channel length for different drain voltages at a constant gate–source voltage. The surface potential at

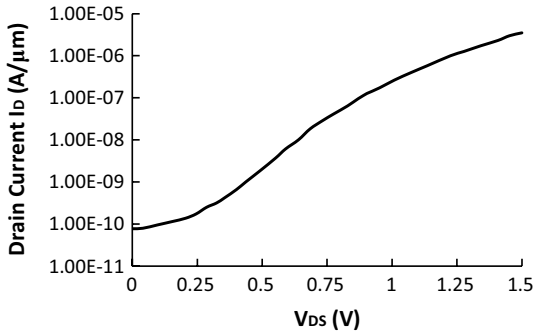

Fig. 8 The log I_D versus V_{DS} characteristic curve of the proposed device

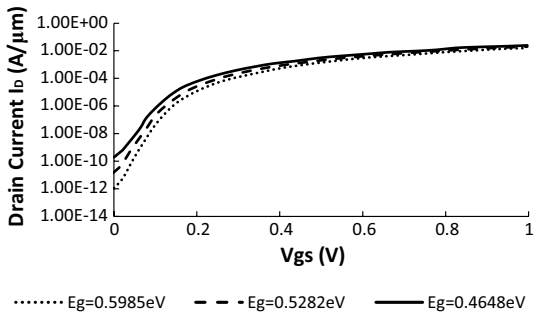

Fig. 9 The I_D versus V_{GS} transfer characteristics of the proposed device

the source side remains unaffected by the drain voltage. Also, the slope of the potential profile is unaffected when increasing the drain bias. Therefore, the drain-induced barrier lowering (DIBL) effect will be significantly reduced and the tunneling current will remain shielded from the drain bias.

The variation of the lateral electric field Ξ_x along the channel length at a constant drain voltage and constant gate voltage is shown in Fig. 6. The gradient of the field is high at the source and drain ends, but low in the middle of the channel. This gradient aids the diffusion of the carriers injected due to BTBT at the source junction to move to the drain end. The lateral electric field is crucial in calculating the tunneling generation rate.

Figure 7 plots the vertical electric field Ξ_y along the channel length at a constant drain voltage and constant gate voltage. The vertical electric field is maximum at the source end, which is the tunneling junction, but low at the drain end. Therefore, the chance of vertical tunneling from the gate is higher near the source than the drain. Therefore, bandgap or material engineering at the source side can reduce the leakage current. Also, the total electric field is maximum at the source–channel interface, i.e., the tunneling junction. This

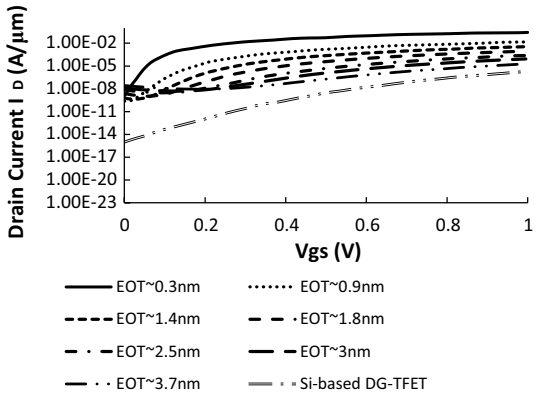

Fig. 10 The I_D versus V_{GS} characteristics for the proposed device at various t_{ox} values and for the Si-based DG-TFET

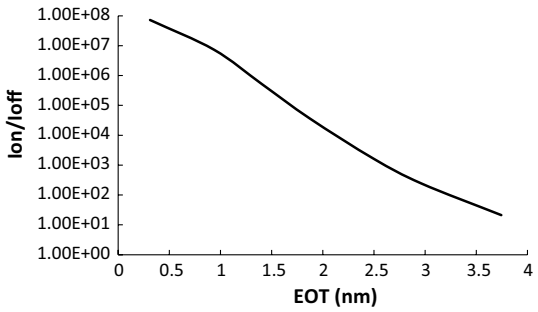

Fig. 11 The I_{on} to I_{off} ratio versus the EOT for the proposed device structure

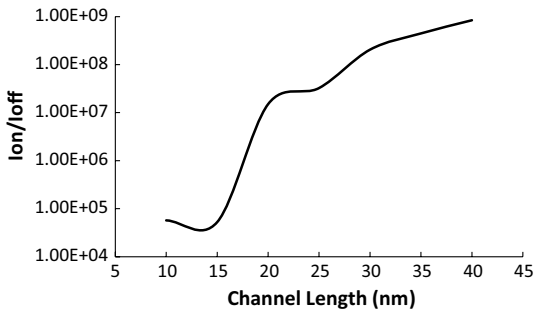

Fig. 12 The I_{ON}/I_{OFF} ratio versus the channel length (i.e., the scaling of the device dimension) for the proposed device structure

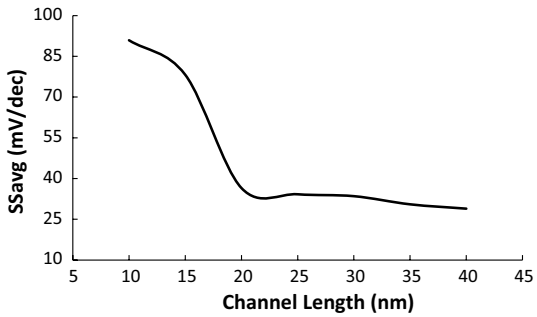

Fig. 13 The variation of SS_{avg} versus the channel length (scaling trend)

depicts the local band bending of the energy band leading to the BTBT.

Figure 8 illustrates the output characteristics of the device at constant gate–source voltage. The drain current I_D increases with the drain voltage, as desired.

Figure 9 shows the transfer characteristics of the device at constant drain–source voltage for different bandgaps taken from Table 2. An ON-current I_{ON} of ~ 25 mA/μm is achieved with an OFF-current of ~ 10^{-10} A/μm for a bandgap E_g of 0.4648 eV. The EOT of the proposed device is taken as ~ 1 nm. The OFF-current of the device varies when changing the bandgap of the heterostructure, while the ON-current shows very little change. It can thus be concluded that the device performance is dependent on the mole fraction values in the alloy and the tunneling barrier width is indirectly a function of the mole fraction values of the alloy. The application of the gate voltage reduces the tunneling gap, and a very high local electric field is created, which leads to tunneling. As the gate bias is increased, the tunneling current flows from the source to drain end in the lateral direction. The sharp potential profile strongly influences the tunneling current near the source–channel interface.

The variation of the transfer characteristics when changing the oxide thickness is illustrated in Fig. 10, which presents a comparative view of the I_D versus V_{GS} characteristics of an Si-based DG-TFET (EOT = 2 nm) and the proposed device for various values of t_{ox}. The ON-current increases with a decrease in the EOT. As t_{ox} decreases, the electric field increases, which in turn increases the tunneling probability. This increase in the band-to-band tunneling results in an increase of the ON-current of the device. It is observed that the proposed device offers a higher ON-current (~ 25 mA/μm) as compared with the Si-based DG-TFET (~ 2 μA/μm). The OFF-current of the proposed device is little affected when changing the EOT, showing a lower leakage current. A lower OFF-current is obtained for the Si-based DG-TFET. To overcome the disadvantage of the higher OFF-current, certain types of structural engineering can be incorporated, such as the addition of a drain pocket at the channel–drain interface. This not only reduces the OFF-current but also helps to eliminate the ambipolarity [39, 40]. The structure proposed herein overcomes the major disadvantage of the low ON-current of almost all types of TFET. The use of the SiGeSn heterostructure offers a great advance in this regard, and the proposed structure is clearly seen to provide a much higher ON-current than the Si-based DG-TFET when using comparable device parameters.

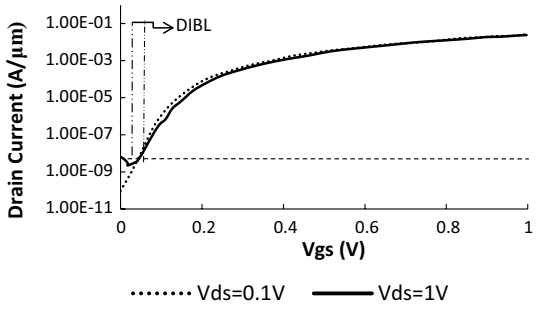

Fig. 14 The transfer characteristics of the proposed device, indicating the DIBL effect

Figure 11 illustrates the variation of the I_{ON}/I_{OFF} ratio over a range of EOT values for the proposed device structure. A smaller EOT values gives a higher ON-current, leading to a better I_{ON}/I_{OFF} ratio and complements the device scaling. As the EOT of the device is increased, a degradation is seen in the I_{ON}/I_{OFF} ratio. The incorporation of a high-K dielectric (HfO_2) helps to obtain a lower EOT, thereby improving the overall performance of the device.

Figure 12 shows the variation of the I_{ON}/I_{OFF} ratio when changing the channel length. At shorter channel lengths, the SCEs emerge, thereby reducing the I_{ON}/I_{OFF} ratio. Around a channel length of 20 nm, there is a large increase in the I_{ON}/I_{OFF} ratio, thus proving that this channel length can provide the optimum device characteristics while allowing device scaling. A I_{ON}/I_{OFF} ratio on the order $\sim 10^7$ is observed at the channel length of 20 nm.

Figure 13 depicts the SS_{avg} of the proposed device structure versus the channel length. As the device dimensions are increased, a lower SS_{avg} is obtained. For a shorter channel length, i.e., 10 nm, an SS_{avg} value of 90 mV/dec is obtained. Meanwhile, at a channel length of 20 nm, an SS_{avg} value of 36.5 mV/dec is obtained, being much lower than that obtained from conventional MOSFET and TFET devices.

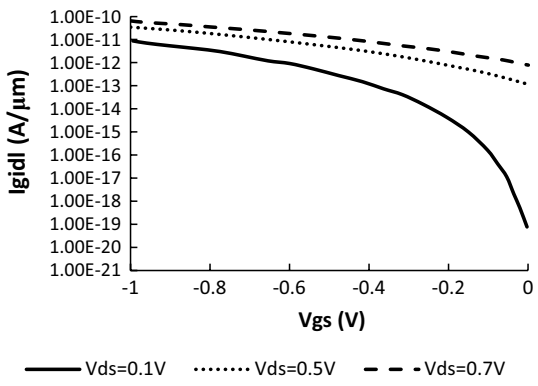

Fig. 15 The $I_{GIDL} - V_{GS}$ transfer characteristics for different drain voltages

Table 3 A comparison of the proposed device structure with the Si-based TFET

Device	I_{ON}/I_{OFF}	SS_{avg} (mV/dec)	DIBL (mV/V)
Si-based TFET	10^9 [39]	104 [12]	121 [12]
Proposed GeSiSn-based heterojunction device ($L_G = 20$ nm)	10^7	36.5	44.4

Figure 14 illustrates the transfer characteristics of the proposed device at $V_{DS} = 0.1$ V and 1 V. The DIBL is calculated as the ratio of the difference of the gate voltages at which the drain current is equal to the DIBL current of 10^{-9}A/μm at different V_{DS} values to the difference of the drain voltages [12]. The DIBL of the proposed device extracted from the graph is 44.4 mV/V, being much lower than for conventional TFETs (~ 121 mV/V) [12]. Thus, the DIBL is reduced by almost 63%.

Figure 15 illustrates the gate-induced drain leakage (GIDL) current of the device [41–43] obtained for different V_{GS} values at fixed drain voltages. The GIDL current can be reduced by increasing the EOT and introducing structural engineering into the device, which eventually improves the overall device performance.

Table 3 presents a comparison of the various performance characteristics of the Si-based TFET and the proposed device structure. The advantages of the current structure are clearly observed in the context of the low I_{ON}/I_{OFF} ratio of the proposed device, and it can be concluded that the source of this problem is the higher I_{OFF} of the proposed device compared with the Si-based TFET. Further studies are necessary to address this problem, along with that of the ambipolarity. It can be conjectured that optimization of the device structure, and hence the nature of the strain in the material, could be employed for such work. Another important unresolved issue is related to the presence of interface trap states that may play a role, typically via the generation of hot electrons. However, at this point, there is little experimental data available on SiGeSn to reach any conclusion on this matter.

4 Conclusions

A strained $Ge_{1-x-y}Si_xSn_y/Ge_{1-a-b}Si_aSn_b$ direct type II staggered heterojunction n-channel tunneling FET with a dual-material double gate is designed and an analytical model proposed for the same. Analytical expressions for the electric field and surface potential are derived. Using the electric field components, the tunneling generation rate is calculated and thus the drain current is obtained using Kane's model. The two major disadvantages of the TFET include a low

ON-current and ambipolarity, restricting use in low-power applications. The device proposed herein improves the ON-current drastically. It is thus concluded that the proposed GeSiSn-based TFET achieves better ON-current I_D as compared with the Si-based DG-TFET.

Acknowledgements The authors thank Prof. Sudakshina Kundu, Ex-Professor, Maulana Abul Kalam Azad University of Technology, West Bengal and Dr. Anirban Bhattacharyya, Assistant Professor, Institute of Radio Physics and Electronics, University of Calcutta for providing insight and expertise that greatly helped in the research.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflicts of interest.

References

1. Arun Samuel, T.S., Balamurugan, N.B.: An analytical modeling and simulation of dual material double gate tunnel field effect transistor for low power applications. J. Electr. Eng. Technol. **8**, 742–748 (2013)
2. Taur, Y., Ning, T.H.: Fundamentals of modern VLSI devices. Cambridge University Press, Cambridge (1998)
3. Anvarifard, M.K., Ramezani, Z., Amiri, I.S., Nejad, A.M.: A nanoscale-modified band energy junctionless transistor with considerable progress on the electrical and frequency issue. Mater. Sci. Semicond Process **107**, 104849 (2020)
4. Shoormasti, A.S., Orouji, A.A., Anvarifard, M.K.: Performance improvement of SiGe based silicon-on-insulator transistor using vertically graded channel approach. Silicon **11**, 3021–3030 (2019)
5. Choi, W.Y., Park, B.-G., Lee, J.D., Liu, T.-J.K.: Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett. **28**(8), 743–745 (2007). https://doi.org/10.1109/LED.2007.901273
6. Gandhi, R., Chen, Z., Singh, N., Banerjee, K.: Vertical Si-Nanowire n-type tunneling FETs with low subthreshold swing (~50 mV/decade) at room temperature. IEEE Electron Device Lett. **32**(4), 437–439 (2011). https://doi.org/10.1109/led.2011.2106757
7. Zhang, Qin, Zhao, Wei, Seabaugh, Alan: Low subthreshold-swing tunnel transistors. IEEE Electron Device Lett. **27**(4), 297–300 (2006). https://doi.org/10.1109/LED.2006.871855
8. Pal, A., Sachid, A.B., Gossner, H., Rao, V.R.: Insights into the design and optimization of tunnel-FET devices and circuits. IEEE Trans. Electron Devices **58**(4), 1045–1053 (2011)
9. Upasana, Narang, R., Saxena, M., Gupta, M.: "Modeling and TCAD assessment for gate material and gate dielectric engineered TFET architectures: circuit-level investigation for digital applications. IEEE Trans. Electron Devices **62**(10), 3348–3356 (2015)
10. Anvarifard, M.K., Orouji, A.A.: Enhancement of a nanoscale novel Esaki tunneling diode source TFET (ETDS-TFET) for low-voltage operations. Silicon **11**, 2547–2556 (2019)
11. Uddin Shaikh, M.R., Loan, S.A.: Drain-engineered TFET with fully suppressed ambipolarity for high-frequency application. IEEE Trans. Electron Devices **66**(4), 1628–1634 (2019)
12. Garg, S., Saurabh, S.: Improving the scalability of SOI-based tunnel FETs using ground plane in buried oxide. J. Electron Devices Soc. IEEE **7**, 435–443 (2019)
13. Lu, H., Lu, B., Zhang, Y., Zhang, Y., Lv, Z.: Drain current model for double gate tunnel-FETs with in As/Si heterojunction and source-pocket architecture. Nanomaterials **9**, 181 (2019)
14. Ferhati, H., Djeffal, F., Bentrcia, T.: The role of the Ge mole fraction in improving the performance of a nanoscale junctionless tunneling FET: concept and scaling capability. Beilstein J Nanotechnol. **9**, 1856–1862 (2018)
15. Boucart, K., Ionescu, A.M.: Double-gate tunnel FET with high-k gate dielectric. IEEE Trans. Electron Devices **54**(7), 1725–1733 (2007)
16. Saurabh, S., Jagadesh Kumar, M.: Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. IEEE Trans. Electron Devices **58**(2), 404–410 (2011)
17. Nayfeh, O.M., Chleirigh, C.N., Hennessy, J., Gomez, L., Hoyt, J.L., Antoniadis, D.A.: Design of tunneling field-effect transistors using strained-silicon/strained-germanium type-II staggered heterojunctions. IEEE Electron Device Lett. **29**(9), 1074–1077 (2008)
18. Vimala, P., Arun Samuel, T.S., Nirmal, D., Panda, A.K.: Performance enhancement of triple material double gate TFET with heterojunction and heterodielectric. Solid State Electron. Lett. **1**(2), 64–72 (2019)
19. Bhuwalka, K.K., Schulze, J., Eisele, I.: Scaling the vertical tunnel FET with tunnel band gap modulation and gate work function engineering. IEEE Trans. Electron Devices **52**(5), 909–917 (2005)
20. He, G., Atwater, H.A.: Interband transitions in SnxGe$_{1-x}$ alloys. Phys. Rev. Lett. **79**, 1937–1940 (1997)
21. Bauer, M., Taraci, J., Tolle, J., Chizmeshya, A.V.G., Zollner, S., Smith, D.J., Menendez, J., Hu, C., Kouvetakis, J.: Ge–Sn semiconductors for band-gap and lattice engineering. Appl. Phys. Lett. **81**(1–3), 2992 (2002)
22. D'Costa, V.R., Cook, C.S., Birdwell, A.G., Littler, C.L., Canonico, M., Zollner, S., Kouvetakis, J., Menendez, J.: Optical critical points of thin-film Ge$_{1-y}$Sn$_y$ alloys: a comparative Ge$_{1-y}$Sn$_y$/Ge$_{1-x}$Si$_x$ study. Phys. Rev. B. **73**(1–16), 125207 (2006)
23. Roucka, R., Xie, J., Kouvetakis, J., Mathews, J., D'Costa, V., Menendez, J., Tolle, J., Yu, S.Q.: Ge$_{1-y}$Sny photoconductor structures at 1.55 μm: from advanced materials to prototype devices. J. Vac. Sci. Technol. B **26**, 1952–1959 (2008)
24. Chizmeshy, A.V.G., Ritter, C., Tolle, J., Cook, C., Menendez, J., Kouvetakis, J.: Fundamental studies of P(GeH$_3$)$_3$, As(GeH$_3$)$_3$, and Sb(GeH$_3$)$_3$: practical *n*-dopants for new group IV semiconductors. Chem. Mater. **18**, 6266–6277 (2006)
25. Menendez, J., Kouvetakis, J.: Type-I Ge/GeSiSn strained layer heterostructures with a direct Ge band gap. Appl. Phys. Lett. **85**, 175–1178 (2004)
26. Basu, P.K., Mukhopadhyay, B., Basu, R.: Semiconductor laser theory. CRC Press, Boca Raton (2015)
27. Jiang, L., Gallagher, J.D., Senaratne, C.L., Aoki, T., Mathews, J., Kouvetakis, J., Menendez, J.: Compositional dependence of the direct and indirect band gaps in Ge1_ySny alloys from room temperature photoluminescence: implications for the indirect to direct gap crossover in intrinsic and n-type materials. Semicond. Sci. Technol. **29**, 115028 (2014)
28. Dutt, B., Lin, H., Sukhdeo, D.S., Vulovic, B.M., Gupta, S., Nam, D., Saraswat, K.C., Harris Jr., J.S.: Theoretical analysis of GeSn alloys as a gain medium for a Si-compatible laser. IEEE J. Sel. Top. Quant. Electron. **19**, 1502706 (2013)
29. Dey, S., Mukhopadhyay, B., Sen, G., Basu, P.K.: Type II band alignment in Ge$_{1-x-y}$Si$_x$Sn$_y$/Ge$_{1-\alpha-\beta}$Si$_\alpha$Sn$_\beta$ heterojunctions. Solid State Commun. **270**, 155–159 (2018)
30. Wang, L., Yu, E., Taur, Y., Asbeck, P.: Design of tunneling field effect transistors based on staggered heterojunctions for ultra-low power applications. IEEE Electron Device Lett. **31**(5), 431–433 (2010)
31. Wang, H., Han, G., Liu, Y., Hu, S., Zhang, C., Zhang, J., Hao, Y.: Theoretical investigation of performance enhancement in GeSn/SiGeSn type-II staggered heterojunction tunneling FET. IEEE Trans. Electron Devices **63**(1), 303–310 (2016)

32. Kane, E.O.: Zener tunneling in semiconductors. J. Phys. Chem. Solids **12**(2), 181–188 (1960)
33. Kane, E.O.: Theory of tunneling. J. Appl. Phys. **32**(1), 83–91 (1961)
34. Bardon, M.G., Neves, H.P., Puers, R., Hoof, C.V.: Pseudo-two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions. IEEE Trans. Electron Devices **57**(4), 827–834 (2010)
35. Chuang, S.L.: Physics of photonic devices. Wiley, Hoboken (2009)
36. Chang, G.-E., Chang, S.-W., Chuang, S.L.: Strain-balanced $Ge_zSn_{1-z-x}Si_x/Ge_ySn_{1-x-y}$ multiple-quantum-well lasers. IEEE J Quantum Electron **46**(12), 1813–1820 (2010)
37. Chandrasekhar, M., Pollak, F.H.: Phys. Rev. B **15**, 2127 (1977)
38. Van de Walle, C.G.: Band lineups and deformation potentials in the model-solid theory. Phys. Rev. B **39**, 1871 (1989)
39. Garg, Shelly, Saurabh, Sneh: Suppression of ambipolar current in tunnel FETs using drain pocket: proposal and analysis, superlattices and microstructures. Elsevier, Amsterdam (2017)
40. Shaw, N., Sen, G., Mukhopadhyay, B.: An analytical approach of elimination of ambipolarity of DPDG- TFET using strained type II staggered SiGeSn heterostructure. Superlattices Microstruct. **141**, 106488 (2020). https://doi.org/10.1016/j.spmi.2020.106488
41. Wan, J., Le Royer, C., Zaslavsky, A., Cristoloveanu, S.: Gate-induced drain leakage in FD-SOI devices: what the TFET teaches us about the MOSFET. Microelectron. Eng. **88**(7), 1301–1304 (2011)
42. Liu, X., Hu, H., Wang, M., Miao, Y., Han, G., Wang, B.: Design and theoretical calculation of novel GeSn fully-depleted n-tunneling FET with quantum confinement model for suppression on GIDL effect. Superlattices Microstruct. **118**, 266–274 (2018)
43. Bouhdada, A., Bakkalli, S., Touhami, A.: Modeling of gate induced drain leakage in relation to technological parameters and temperature. Microelectron. Reliabil. **37**, 649–652 (1997)