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A variation-aware design for storage cells using Schottky-barrier-type GNRFETs

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Abstract

Graphene nanoribbons (GNRs) are a good replacement material for silicon to overcome short-channel effects in nanoscale devices. However, with continuous technology scaling, the variability of device parameters also increases. Indeed, process, voltage, and temperature (PVT) variations affect the performance of GNR devices because of their small size. Moreover, the bandgap of GNRs is strongly affected by the number of carbon atoms across the channel width. This paper accurately evaluates the impact of such PVT variations on the performance of circuits based on Schottky barrier (SB)-type GNR field-effect transistors (SB-GNRFETs) in terms of their timing parameters, power, and energy–delay product (EDP). Extensive simulations and stability analysis are performed on both flip-flop and conventional six-transistor static random-access memory (6T SRAM) cells made using SB-GNRFETs under these variations. A statistical analysis of the impact of the PVT variations on the SB-GNRFET-based flip-flop is also performed using Monte Carlo simulations, considering the variation of one or all of the parameters, with or without line-edge roughness effects.

Keywords Schottky-barrier-type graphene nanoribbon field-effect transistors (SB-GNRFETs) · Flip-flop · Process, voltage, and temperature (PVT) variations · Monte Carlo (MC) simulation · Static random-access memory (SRAM)

1 Introduction

As the channel length of Si complementary metal–oxide–semiconductor (CMOS)-based transistors approaches the sub-10-nm domain, various short-channel effects such as subthreshold leakage and drain-induced barrier lowering (DIBL) degrade the device performance [1]. One of the solutions to such Si CMOS scaling issues is the application of emerging materials to replace silicon [2]. Graphene, a sheet of carbon atoms in a two-dimensional (2-D) honeycomb lattice [3], is a good candidate in this regard because of its impressive properties such as high charge carrier mobility, high optical transparency, low Johnson noise, excellent mechanical strength, nanometer-scale electron mean free path, atomically thin planar geometry, and high electrical and thermal conductivities [4–10]. However, it cannot be used directly for the device channel because of its zero bandgap energy. To open up the bandgap, it can be patterned into one-dimensional (1-D) graphene nanoribbons (GNRs) with widths of less than 10 nm [11].

GNR field-effect transistors (GNRFETs) represent a better alternative to silicon transistors due to their high charge carrier velocity, faster switching, and lower energy–delay product (EDP) [12]. However, the impact of process, voltage, and temperature (PVT) variations on GNRFETs is very large due to their small dimensions [13]. Some limited studies have been carried out to evaluate the impact of such variations on these transistors in both analog and digital applications. In Ref. [12], a Schottky barrier (SB)-type GNRFET (SB-GNRFET)-based *LC*-tuned voltage-controlled oscillator (LC-VCO) was designed and simulated but only considering variations in the manufacturing process such as the oxide thickness, the number of dimer lines, and the channel length. In Refs. [11, 14, 15], various SB-GNRFET-based digital logic circuits including INV, NAND, NOR, and XOR were simulated under PVT variations in terms of their delay and power. SB- and metal–oxide–semiconductor (MOS)-type GNRFET (MOS-GNRFET)-based standard ternary INV,

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NAND, NOR, and static random-access memory (SRAM) circuits were designed and simulated without consideration of PVT variations in Ref. [16]. In Ref. [17], a GNRFET-based eight-bit arithmetic logic unit (ALU) was simulated and compared with a Si CMOS design in terms of their delay and power, revealing that the SB-GNRFET design offered better performance. The results in Ref. [18] show that the write ability of GNRFET-based SRAM is better than that of a Si-CMOS design due to its lower write trip power, whereas the Si CMOS-based SRAM is more stable because of its large static power noise margin. In Ref. [19], MOS-GNRFET, MOS-carbon nanotube (CNT)FET, and Si CMOS-based conventional six-transistor (6T) SRAM circuits were simulated and the N-curve method was employed to analyze their stability under supply voltage variations. The results indicated nearly equivalent stability of the GNRFET- and CNTFET-based SRAM circuits, being better than that of the Si CMOS design.

In this paper, a conventional static flip-flop is designed using SB-GNRFETs, then extensive HSPICE simulations are performed to evaluate and analyze the impact of PVT variations in terms of its timing parameters, leakage and dynamic powers, and EDP. Monte Carlo (MC) simulations are performed to statistically analyze the impact of these variations. Moreover, stability analysis of the SB-GNRFET-based SRAM circuit under PVT variations is performed.

The remainder of this manuscript is organized as follows: Section 2 provides an overview on the variability and its various sources for graphene nanoribbons and GNR-based field-effect transistors. In Sect. 3, the SB-GNRFET-based flip-flop and its timing parameters are described. The SB-GNRFET-based 6T SRAM and its noise margin measurement using the N-curve and butterfly curve methods are also explained in this section. The simulation results as well as the effects of PVT variations and the stability analysis are presented in Sect. 4. Finally, the conclusions are drawn in Sect. 5.

2 Background

2.1 Variability

Variability is the deviation of a device parameter from its nominal value [20]. The scaling down of process technology increases the variability of the device parameters, strongly affecting the performance, yield, power consumption, and energy characteristics [21]. There are several methods, including statistical models, for the precise evaluation of this effect of variability [22]. Generally, there are three types of source of such variation, viz. process variations, environmental variations, and aging variations or reliability issues [23]. The process variations, also known as spatial variations [20], correspond to changes during the device manufacturing process [24], which affect parameters such as the channel length and width, the gate oxide thickness, and the threshold voltage [25]. Meanwhile, environmental, or dynamic, variations arise during the operation of a circuit and include changes in the supply voltage or temperature [26]. As the fabrication technology for GNRFET-based devices is still in an early phase [13], the effects of such variability on them are greater. Moreover, the bandgap of GNRs depend on their width, increasing their propensity towards process variations. Therefore, studying the effects of PVT variations on transistor performance is important to verify GNRFETs as a potential replacement for silicon-based transistors.

2.2 Graphene nanoribbon field-effect transistors (GNRFETs)

Graphene is one of the allotropes of carbon, comprising a single atomic layer of graphite, which is structurally similar to a 2-D honeycomb lattice but is not a Bravais lattice [27]. Graphene acts as a metal because the bandgap between its conduction and valence bands is zero [28]. Hence, this material is unsuitable for application as a transistor channel. However, conversion of graphene into a 1-D GNR with sub-10-nm width opens up the bandgap [11]. The energy gap of a GNR is inversely proportional to its width [29]. GNRs can be categorized into two types: zigzag GNRs (ZGNRs) and armchair GNRs (AGNRs) [30], as shown in Fig. 1, differing in the type of edge or chiral angle or their orientation along the GNR lattice. ZGNRs are always metallic, while AGNRs are metallic or semiconductor depending on their width [31].

GNR-based transistors can be classified into two main types depending on their structure. MOS-GNRFETs have an *n*–i–*n* or *p*–i–*p* structure consisting of a GNR channel plus doped source and drain regions. SB-GNRFETs, on the other hand, have an m–i–m structure, consisting of a GNR channel plus a metallic source and drain [32]. MOS-GNRFETs exhibit monotonic *I*–*V* curves, as opposed to the ambipolar curve observed for SB-GNRFETs, which occurs due to the SB at the graphene–metal junctions. As a result, MOS-GNRFETs offer larger I_{ON}/I_{OFF} ratios than SB-GNRFETs. Some of the benefits of SB-GNRFETs are as follows [11, 15]:

- The lack of doping in the metallic drain and source regions, meaning that they are not very sensitive to process variations
- The absence of contacts with high electrical resistance in vias within the drain and source
- The lack of extra graphene–metal vias due to the metal-based interconnects and terminals

Figure 2 shows the schematic structure of a SB-GNRFET. Parallel AGNRs are used in this structure to increase the

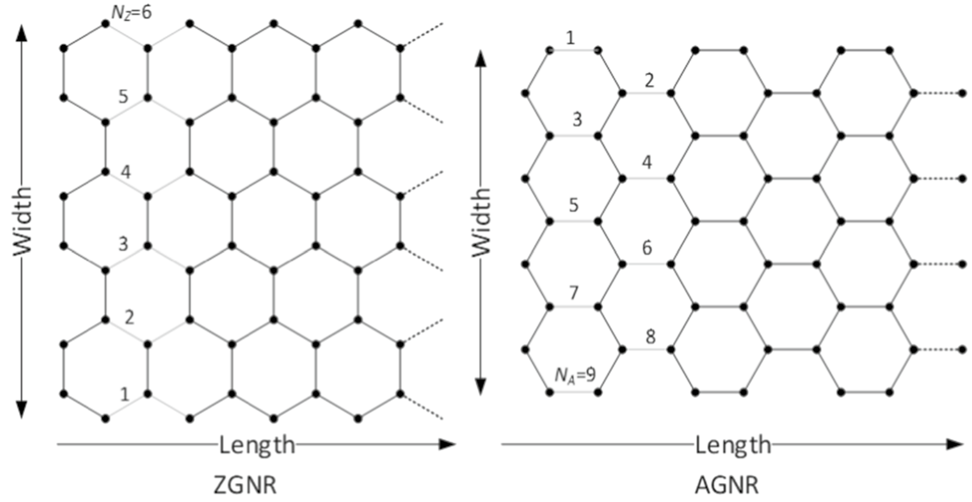


Fig. 1 The structure of ZGNRs and AGNRs

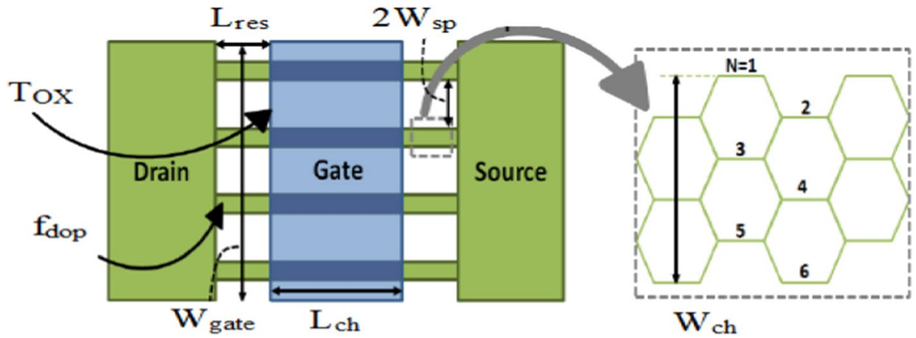


Fig. 2 The structure of a SB-GNRFET with four parallel armchair-type GNRs [14]

driving strength of the transistor [11]. The parameters L_{ch}, W_{gate}, L_{res}, $2W_{\mathrm{sp}}$, and f_{dop} denote the channel length, the gate width, the length of the reservoirs, the distance between two adjacent GNRs in the same device, and the doping level of the drain and source, respectively. W_{ch} denotes the width of each GNR, which can be determined from the number of dimer lines N as follows:

$$W_{\mathrm{CH}} = \sqrt{3}d_{\mathrm{cc}}\frac{\left(N_A - 1\right)}{2}, \tag{1}$$

$$W_{\mathrm{GATE}} = \left(W_{\mathrm{CH}} + 2W_{\mathrm{sp}}\right) \times N_{\mathrm{ribb}}, \tag{2}$$

where $d_{\mathrm{cc}} = 1.42\,\mathrm{nm}$ is the carbon–carbon bond distance and N_{ribb} is the number of ribbons. The index A in N_A represents the number of dimer lines of AGNRs.

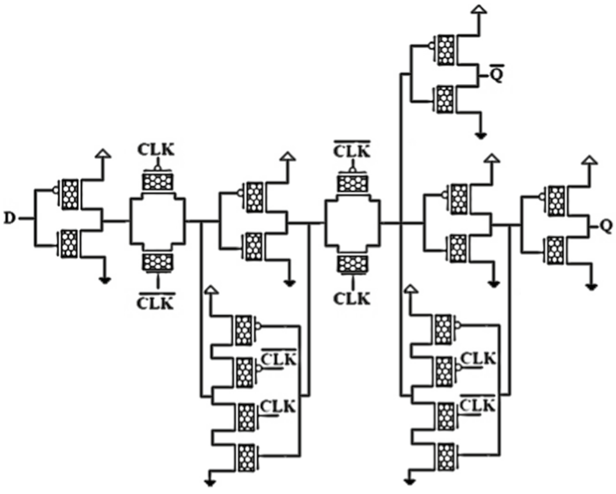


Fig. 3 The transistor-level structure of the SB-GNRFET-based FF

3 Circuit design and specifications

3.1 The SB-GNRFET-based flip-flip and its timing parameters

Flip-flops (FFs) are one of the main building blocks used in digital system design, allowing the storage of data [33]. Figure 3 shows the transistor-level structure of the SB-GNRFET-based rising-edge-triggered FF. Most standard cell libraries employ this design due to its attributes of simplicity, compactness, robustness, and energy efficiency [34].

A FF operates correctly when its data and clock inputs satisfy basic timing limitations, e.g., on the setup and hold times. Thus, the input data should be held steady before and after the clock edge as long as the setup time and hold time, respectively [35]. Figure 4 qualitatively exhibits plots of the clock to output delay (t_{CQ}) and the data to output delay (t_{DQ}) versus the time from the arrival of the rising data to the rising edge of the clock (t_{DC}).

According to Fig. 4, t_{CQ} has a constant minimum value [called the contamination delay (t_{ccq})] and also t_{DQ}, which is the sum of t_{DQ} and t_{CQ} ($t_{\mathrm{DQ}} = t_{\mathrm{DQ}} + t_{\mathrm{CQ}}$), has a slope equal to -1 when t_{DC} is very large. On the other hand, as t_{DC} decreases, t_{CQ} increases until reaching an asymptote, after which the FF cannot correctly capture the data while t_{DQ} reaches a minimum ($t_{\mathrm{DQ,min}}$) at the point where t_{CQ} has a slope of -1. The setup time (t_{setup}) and propagation delay (t_{pcq}) are defined at $t_{\mathrm{DQ,min}}$ [36]. The hold time (t_{hold}) is the minimum delay from the clock to data changing, such that $t_{\mathrm{CQ}} \leq t_{\mathrm{pcq}}$ [34]. The sum of t_{setup} and t_{hold} is defined as the possible minimum width of a data pulse. The setup time and the hold time can be both positive and negative, depending on the supply voltage, the circuit topology, and the simulation setup [37].

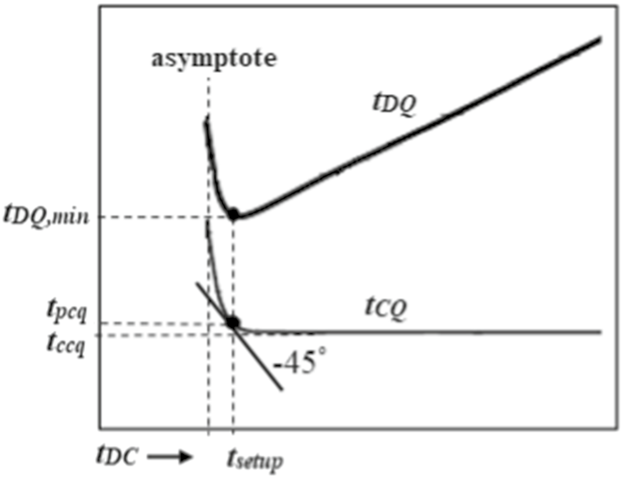


Fig. 4 Plots of t_{DQ} and t_{CQ} versus the time from the arrival of the rising data to the rising edge of the clock t_{DC} [36]

3.2 The SB-GNRFET-based 6T SRAM

The variations in the device parameters increase for deep-submicron technologies, which can seriously affect the stability of SRAM cells [38]. In the structure of the SB-GNRFET-based 6T SRAM shown in Fig. 5a, the pull-down transistors NM1 and NM2 and the pull-up transistors PM1 and PM2 form two back-to-back inverters. The output nodes of the inverters (Q and QB) are coupled with the bit lines (BL and BLB) by the access transistors NM3 and NM4. In standby mode, the word line (WL) has a logical value of "0" hence NM3 and NM4 turn off and only two inverters remain. In this mode, the static noise margin (SNM) can be determined by plotting the butterfly voltage transfer curve (VTC) for the input and output nodes of the two inverters. The SNM is the length of the side of the largest square that can be inscribed between these curves, called the hold margin (Fig. 5b). In read mode, the BL and BLB are initially precharged to V_{DD}. The WL is high (V_{DD}), and the output value of the two inverters is transferred to the bit lines (Q to BL and QB to BLB). The SNM obtained in this mode is called the read margin and is smaller than the SNM (Fig. 5c). In write mode, the WL is high while the BL can be high or low. The write margin is the size of the smallest square that can be drawn between the two VTCs (Fig. 5d) [34, 39, 40].

To perform the stability analysis of the SRAM cell, three butterfly curves must be drawn in conjunction with the I_q–V_q N-curve. This plot is drawn for the following conditions: BL and BLB are precharged to V_{DD}, the initial value of the nodes Q and QB is "1" and "0", respectively, and the WL is high. Then, a voltage source V_{in} is swept from 0 V to V_{DD} at the node Q and the current I_{in} is measured (Fig. 6a). This plot gives the static voltage noise margin (SVNM), the static current noise margin (SINM), the write trip voltage (WTV), and the write trip current (WTI), as shown in Fig. 6b. The N-curve crosses the horizontal axis at two stable points A and C, and a metastable point B. The SVNM is the maximum direct-current (DC) voltage that can be tolerated at the input of the 6T SRAM cell without changing its state, being defined as the voltage difference between the points A and B. The SINM is the maximum DC current that can be injected into the input of the SRAM before changing its state, being defined as the maximum current between points A and B. The WTV is the voltage that can be applied before varying the content of the internal node, being measured as the voltage difference between points B and C. The WTI is the minimum current between the points B and C that has to be applied to write into the cell [19, 41, 42].

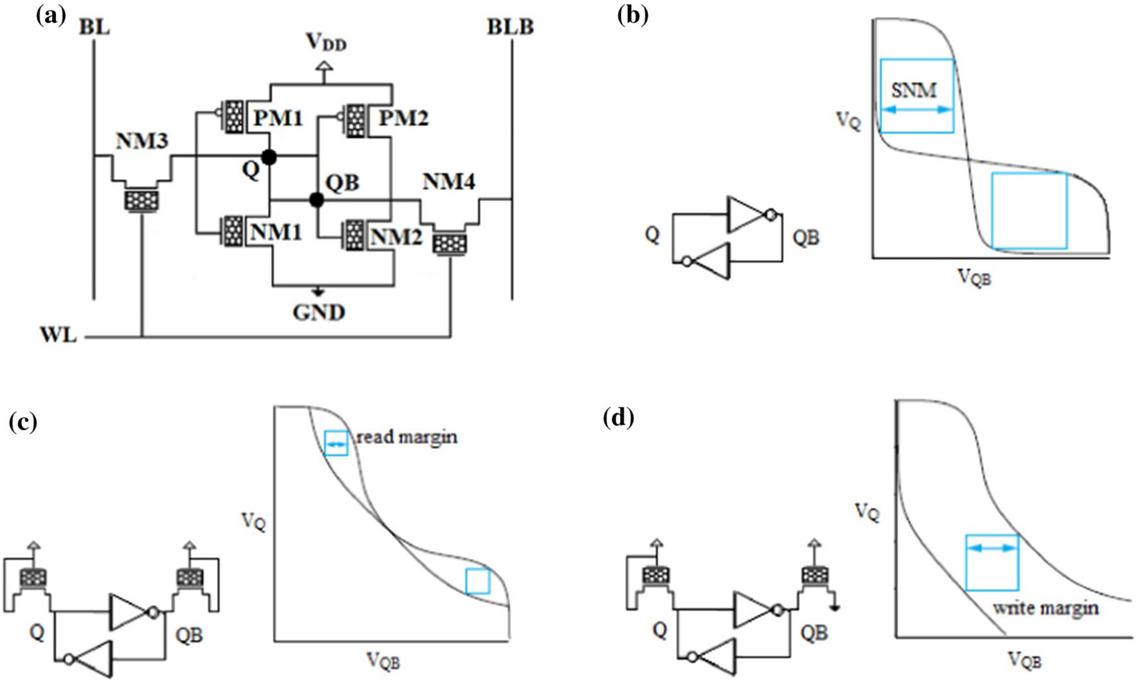


Fig. 5 **a** The SB-GNRFET-based 6T SRAM and its **b** hold circuit and hold margin, **c** read margin circuit and read margin, and **d** write margin circuit and write margin

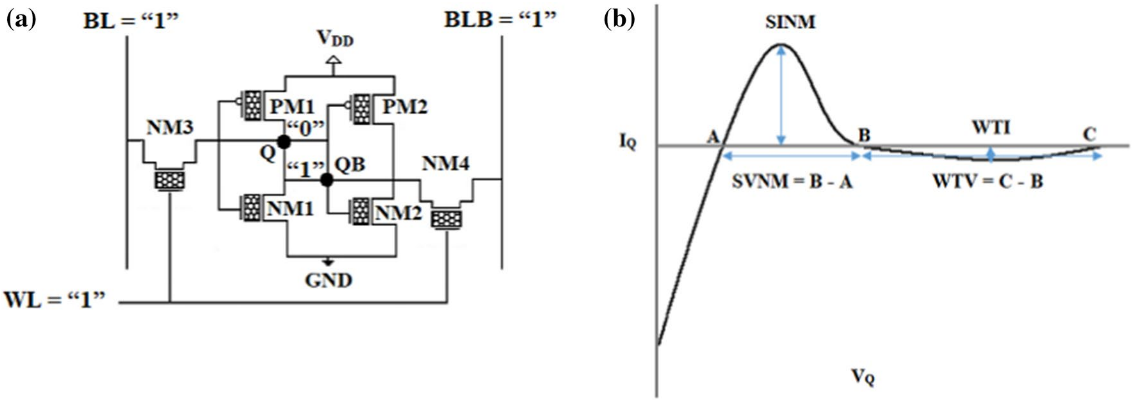


Fig. 6 **a** The experimental setup for the N-curve of the 6T SRAM cell and **b** the N-curve

4 The Simulation Results

This section presents the simulation setup and results. The simulations are performed in HSPICE utilizing the SB-GNRFET model presented in Ref. [11] at 25 °C.

4.1 The SB-GNRFET-based flip-flop

The FF circuit shown in Fig. 3 is designed using the SB-GNRFET device parameters presented in Table 1. Using Eq. (2), the gate width of the SB-GNRFET is obtained as

Table 1 The design parameters of the SB-GNRFET device

SB-GNRFET parameter	Value
Channel length (L_{ch})	16 nm
Number of dimer lines (N)	12
Space between two adjacent GNRs ($2 \times sp$)	2 nm
Number of GNRs (N_{ribb})	6
Oxide thickness (T_{OX})	0.95 nm
Line-edge roughness percentage (P_r)	0
Doping fraction	0.001
Supply voltage	0.5 V
Temperature	25 °C

Table 2 The timing parameters, power consumption, PDP, and EDP for the SB-GNRFET and Si-CMOS-based FFs

Parameter	CMOS design	SB-GNRFET design	Change
t_{setup} (ps)	12.92	2.39	−81.5%
t_{hold} (ps)	8.40	5.43	−35.3%
t_{pcq} (ps)	21.76	4.91	−77.4%
t_{ccq} (ps)	19.66	4.57	−76.7%
P_{avg} (μW)	0.19	3.71	×19.53
PDP (aW s)	4.13	18.22	×4.41
EDP (W s^2)	9×10^{-29}	8.94×10^{-29}	−0.67%

21.59 nm. The data and clock inputs are passed through a buffer (two SB-GNRFET-based inverters in series) to produce realistic input signals. The FF is connected to a fanout-of-4 circuit as its load. To compare the results of the SB-GNRFET-based FF with a Si CMOS design, the Si CMOS transistor parameters are considered to be $L_{ch} = 16$ nm and $w_{ch} = 21.59$ nm with $V_{DD} = 0.7$ V. Figure 5 shows the plots of t_{CQ} and t_{DQ} versus the time from the arrival of the rising data to the rising edge of the clock t_{DC} for both the SB-GNRFET and Si-CMOS-based FF. Their timing parameters, power consumption, power–delay product (PDP), and EDP are presented in Table 2. As can be inferred from this table, the minimum possible width of the data pulse, which is the sum of the setup and hold times, is obtained as 7.82 ps and 21.32 ps for the SB-GNRFET and Si-CMOS design, respectively. The power reported in Table 2 is the average power dissipated in the FF circuit during four operating cycles. The following equations are used to obtain the PDP and EDP values (Fig. 7):

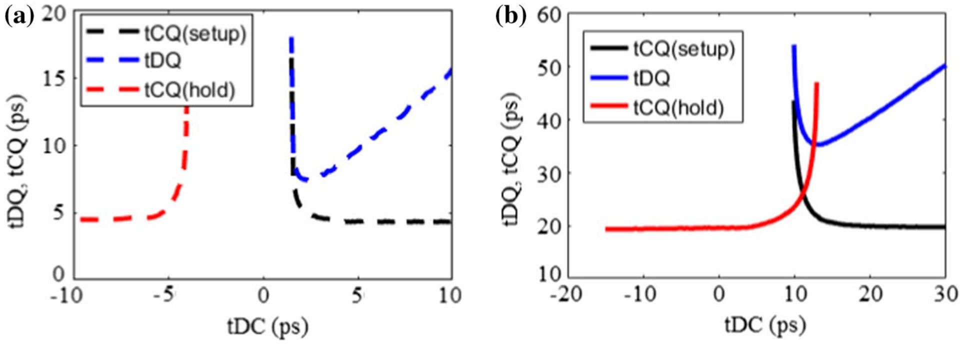
$$\mathrm{PDP} = P_{avg} \times t_{pcq}, \tag{3}$$

$$\mathrm{EDP} = \mathrm{PDP} \times t_{pcq}. \tag{4}$$

4.2 The effects of PVT variations

To study the performance of the SB-GNRFETs under PVT variations, the sensitivity of the main characteristics of the FF such as the timing parameters, power (leakage, dynamic, and total), and EDP to these variations is evaluated and analyzed. Here, the PVT variations include changes in the channel length, gate oxide thickness, number of dimer lines, line-edge roughness, supply voltage, and operating temperature. Figures 8,9,10,11,12,13, and 14 show the effect of the PVT variations on the selected FF characteristics. The impact of channel length (L_{ch}) variations is shown in Fig. 8. L_{ch} has a first-order influence on the delay and performance. The gate capacitance is directly dependent on L_{ch}, which results in a longer delay for longer channel lengths. As the channel

Fig. 7 The plots of t_{DQ} and t_{CQ} versus t_{DC} for the **a** SB-GNRFET-based FF and **b** Si-CMOS-based FF



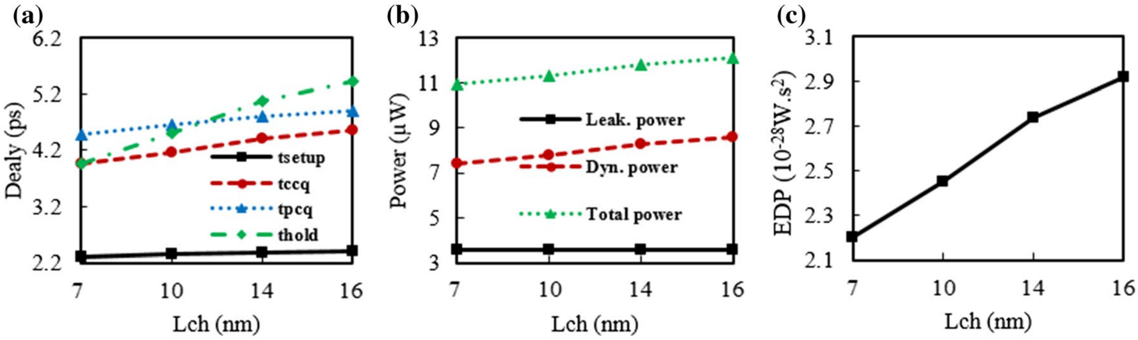


Fig. 8 The effect of the channel length L_{ch} on the **a** timing parameters, **b** powers, and **c** EDP of the SB-GNRFET-based FF

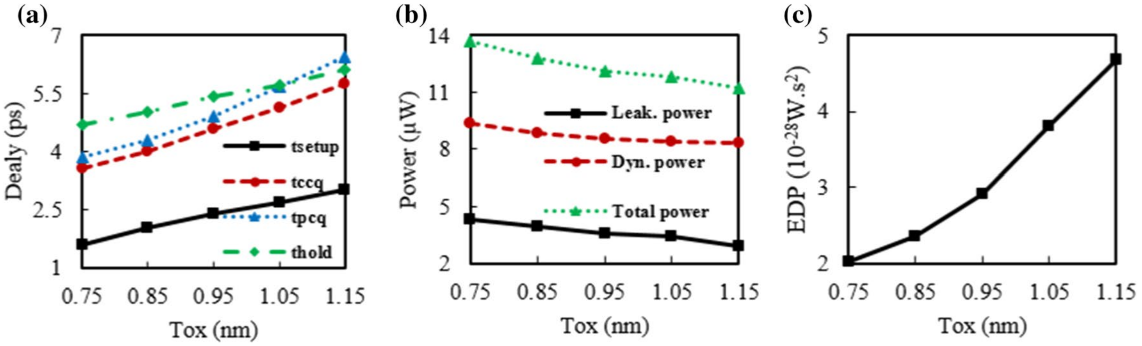


Fig. 9 The effect of the gate oxide thickness T_{ox} on the **a** timing parameters, **b** powers, and **c** EDP of the SB-GNRFET-based FF

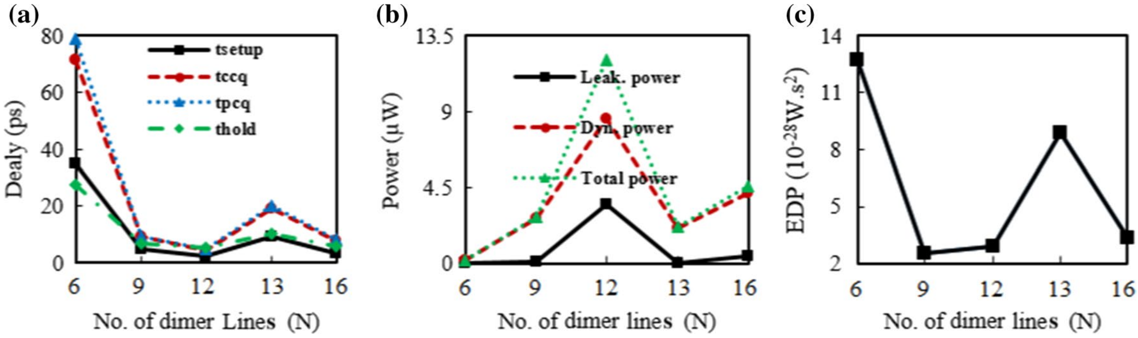


Fig. 10 The effect of the number of dimer lines N on the **a** timing parameters, **b** powers, and **c** EDP of the SB-GNRFET-based FF

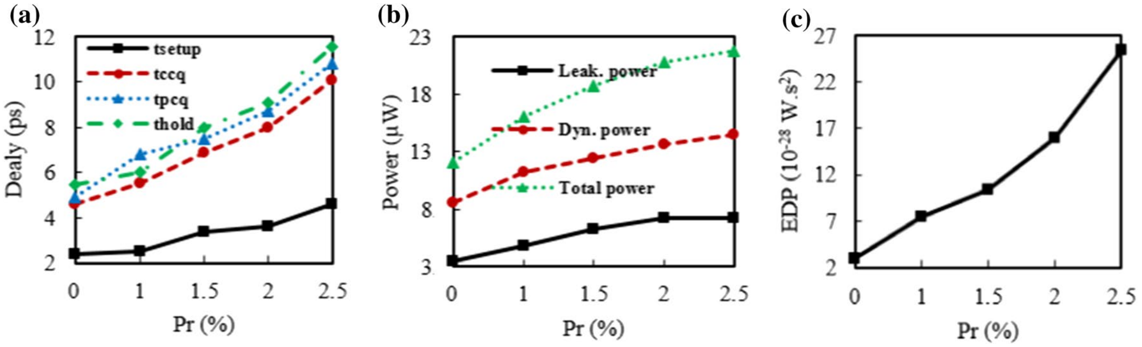


Fig. 11 The effect of the line-edge roughness P_r on the **a** timing parameters, **b** powers, and **c** EDP of the SB-GNRFET-based FF

length is increased, the dynamic power also increases while the leakage power does not change considerably. Figure 9 shows the effect of gate oxide thickness (T_{ox}) variations. T_{ox} has a first-order effect on the delay, power, EDP, and performance. Increasing T_{ox} causes a reduction of the power and delay due to a drop in the ON-current.

As can be seen from Fig. 10, the number of dimer lines (N) has a periodic effect on the bandgap. The widest bandgap and highest I_{ON}/I_{OFF} current ratio are obtained when the number of dimer lines satisfies $N = 3p + 1$ (e.g., 7, 10, and 13). The results for $N = 3p + 2$ (e.g., 8, 11, and 14) are not shown in Fig. 10 because of their very small bandgap and I_{ON}/I_{OFF} ratio. Indeed, these GNRs are not suitable for digital circuit applications. For $N = 3p$ (e.g., 6, 9, and 12), the bandgap is moderate. Simulations are performed for $N = 6, 9, 12, 13, 16$ dimer lines, which can be ordered based on decreasing energy bandgap as 6, 13, 9, 16, and 12. The delay and power show a direct and inverse relation with the bandgap, respectively. As a result, the N corresponding to the longest delay will have the least power consumption, and vice versa.

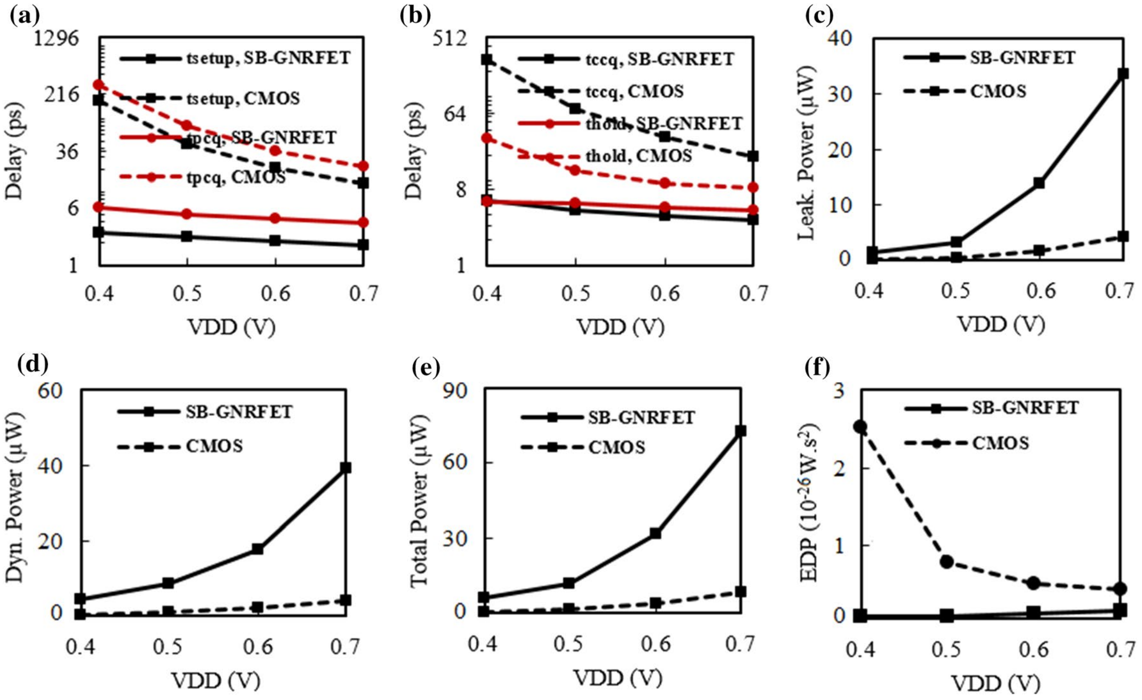


Fig. 12 The effect of the supply voltage V_{DD} on the **a** t_{setup} and t_{pcq}, **b** t_{ccq} and t_{hold}, **c** leakage power, **d** dynamic power, **e** total power, and **f** EDP of the SB-GNRFET and Si-CMOS-based FFs

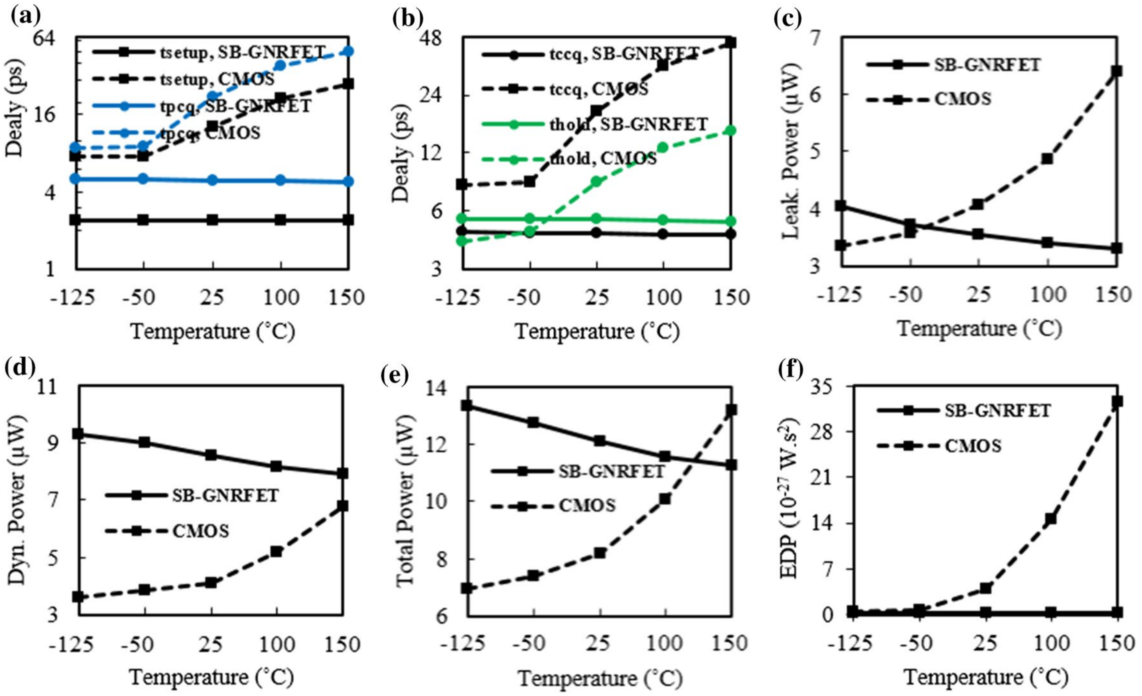


Fig. 13 The effect of the temperature on the **a** t_{setup} and t_{pcq}, **b** t_{ccq} and t_{hold}, **c** leakage power, **d** dynamic power, **e** total power, and **f** EDP of the SB-GNRFET and Si-CMOS-based FFs

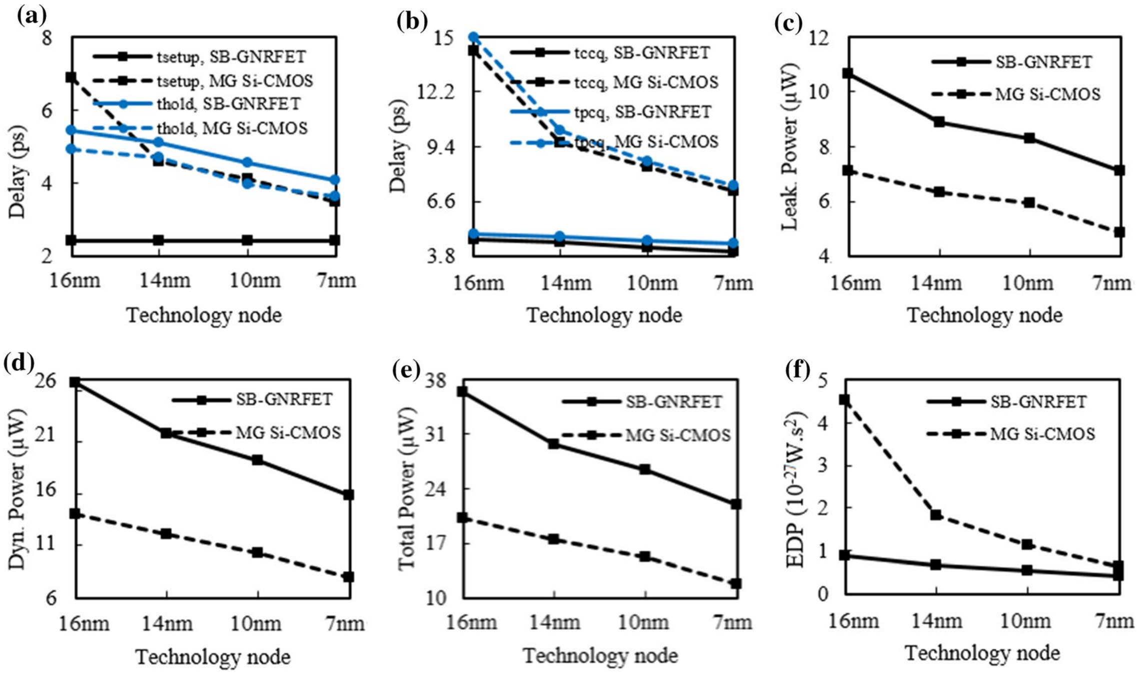


Fig. 14 The effect of the transistor sizes on the **a** t_{setup} and t_{pcq}, **b** t_{ccq} and t_{hold}, **c** leakage power, **d** dynamic power, **e** total power, and **f** EDP of the SB-GNRFET and MG Si-CMOS-based FFs

Figure 11 shows the impact of the line-edge roughness using the parameter P_r. With increasing line-edge roughness, I_{ON} reduces while I_{OFF} first increases then decreases [11]. However, the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio decreases. As shown in Fig. 11, the delay and power rise with increasing line-edge roughness. The effect of the supply voltage (V_{DD}) on the SB-GNRFET and Si-CMOS-based FFs is shown in Fig. 12. The delay decreases with increasing supply voltage, while the power increases. The SB-GNRFET design consumes more power compared with the Si CMOS design, but it has a shorter delay. In the supply voltage range from 0.4 to 0.6 V, the SB-GNRFET design shows better performance than the Si CMOS design, since its EDP is lower. Figure 13 shows the influence of temperature on the SB-GNRFET and Si-CMOS-based FFs. The effect of temperature variations on these designs is quite different. For the Si CMOS design, increasing the temperature results in a longer delay and higher power, while for the SB-GNRFET design, it reduces both the power and delay. Moreover, variation of the temperature has only a small effect on the delay of the SB-GNRFET-based FF. Generally, the SB-GNRFET-based FF shows better performance than the Si-CMOS design due to its lower EDP.

4.3 The simulations at different technology nodes

To compare the performance of the SB-GNRFET-based FF versus conventional Si CMOS technology, different simulations are performed using a multigate Si CMOS predictive technology model (MG Si-CMOS PTM) [43] at the 7-, 10-, 14-, and 16-nm technology nodes, at nominal supply voltages of 0.7, 0.75, 0.8, and 0.85 V, respectively. The equivalent width of a MG Si-CMOS with n fins is defined by $n \times \left(T_{\mathrm{fin}} + 2 \times H_{\mathrm{fin}}\right)$, where H_{fin} is the fin height of the transistor and T_{fin} is the fin thickness [44]. The number of dimer lines, the number of ribbons, and the spacing between two adjacent ribbons are chosen such that the gate width of the SB-GNRFET becomes equal to the effective width of the MG Si-CMOS device. Values of $N = 12$ and $2W_{\mathrm{sp}} = 2\mathrm{nm}$ are chosen, thus determining the number of ribbons (N_{ribb}). The transistor sizes in the different technology nodes are presented in Table 3. Figure 14 shows the timing, power, and EDP characteristics of both the SB-GNRFET and MG Si-CMOS FF designs. A reduction in the transistor size leads to a shorter delay and reduced power. As seen in Fig. 14f, the SB-GNRFET-based FF is better than the MG Si-CMOS

Table 3 The transistor sizes at the different technology nodes

Node (nm)	SB-GNRFET		MG Si-CMOS		
	N_{ribb} (nm)	W_{gate} (nm)	T_{fin} (nm)	H_{fin} (nm)	W_{MG} (nm)
7	12	43.18	6.5	18	42.5
10	14	50.38	9	21	51
14	15	53.98	10	23	54
16	18	64.78	12	26	64

design at the different technology nodes, since it has a lower EDP.

4.4 Monte Carlo simulations

The effect of varying each parameter one at a time is evaluated and analyzed in the previous section. However, more than one parameter may vary from its nominal value [13]. MC simulations are performed for statistical analysis of the sensitivity to the parameters, changing the supply voltage, number of dimer lines, gate oxide thickness, and channel length. The simulations are performed in two different cases, with and without the line-edge roughness effect. A uniform distribution function is used for the supply voltage. For the other parameters, a Gaussian distribution function with 3σ variation is applied. Since the number of dimer lines is an integer, the generated random value is converted to an integer. Each parameter is changed by ±10% around its nominal value

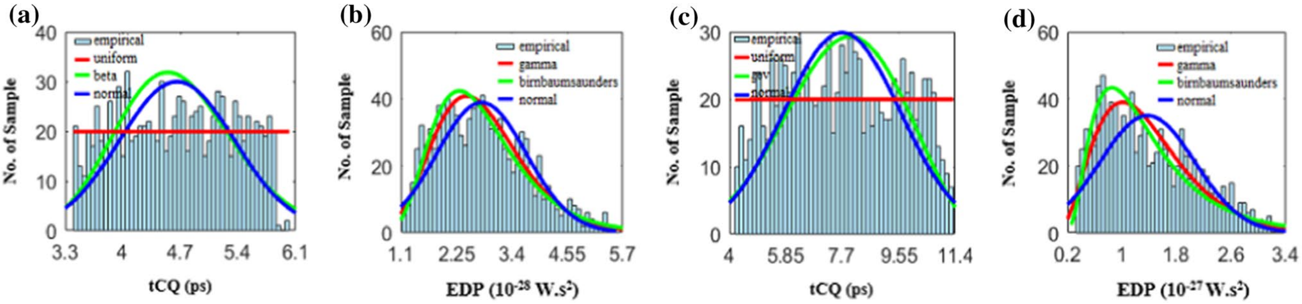


Fig. 15 The histograms of (**a**, **c**) t_{CQ} and (**b**, **d**) the EDP obtained from the MC simulations with a uniform distribution of $V_{\mathrm{DD}} \pm 10\%$ and (**a**, **b** $P_{\mathrm{r}} = 0$) or (**c**, **d**) $P_{\mathrm{r}} = 2.5\%$

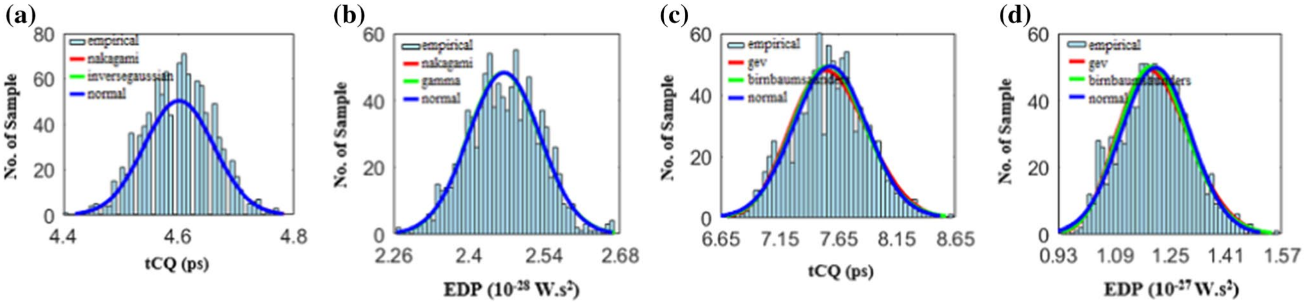


Fig. 16 The histograms of (**a**, **c**) t_{CQ} and (**b**, **d**) the EDP obtained from the MC simulations with a Gaussian distribution of $N \pm 10\%$ and (**a**, **b**) $P_{\mathrm{r}} = 0$ or (**c**, **d**) $P_{\mathrm{r}} = 2.5\%$

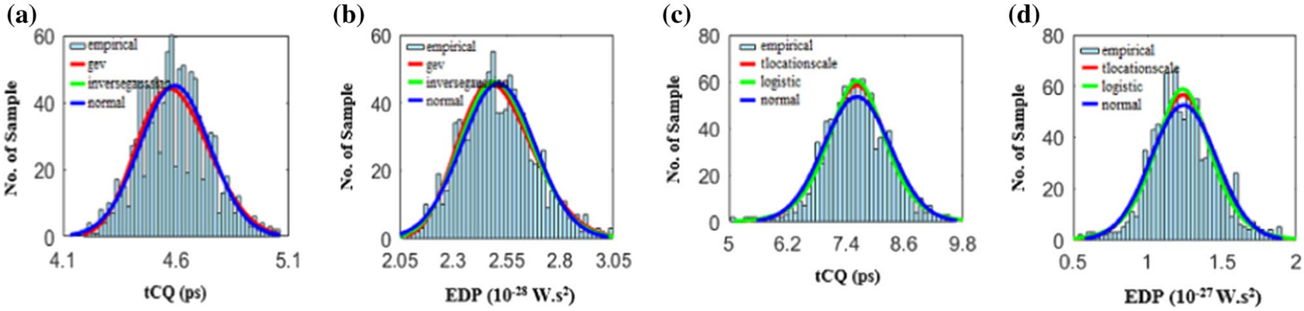


Fig. 17 The histograms of (**a**, **c**) t_{CQ} and (**b**, **d**) the EDP obtained from the MC simulations with a Gaussian distribution of $T_{\mathrm{ox}} \pm 10\%$ and (**a**, **b**) $P_{\mathrm{r}} = 0$ or (**c**, **d**) $P_{\mathrm{r}} = 2.5\%$

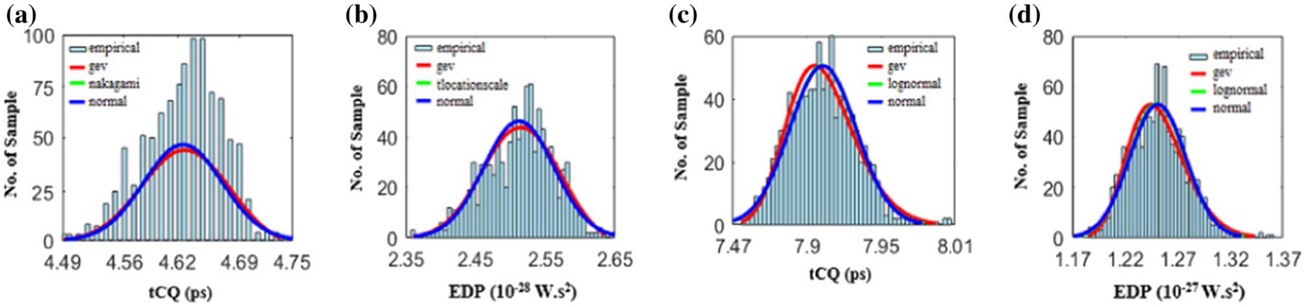


Fig. 18 The histograms of (**a**, **c**) t_{CQ} and (**b**, **d**) the EDP obtained from the MC simulations with a Gaussian distribution of L_{ch} ± 10% and (**a**, **b**) $P_r = 0$ or (**c**, **d**) $P_r = 2.5\%$

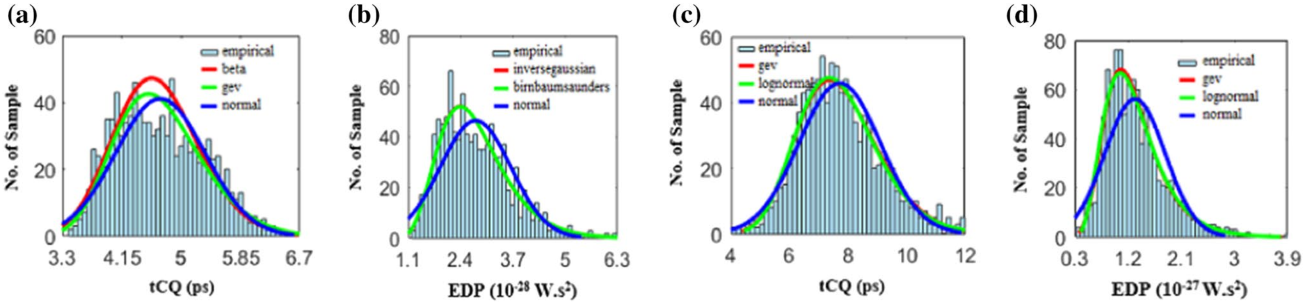


Fig. 19 The histograms of (**a**, **c**) t_{CQ} and (**b**, **d**) the EDP obtained from the MC simulations with the variation of all parameters and (**a**, **b**) $P_r = 0$ or (**c**, **d**) $P_r = 2.5\%$

reported in Table 1 using $N_m = 1000$ samples in the MC simulations. Figures 15,16,17,18, and 19 show the results for the distribution of the t_{CQ} delay and EDP of the SB-GNRFET-based FF as histograms. Each of these figures also shows several distribution functions that best fit the results. The mean (μ) and standard deviation (std) of the data based on a normal distribution function are presented in Table 4. For example, the results for both the ideal ($P_r = 0$) and nonideal ($P_r = 2.5\%$) transistors indicate that varying V_{DD} and N has the greatest and least effect on the total power. The effect of varying V_{DD} and N is about +6.47% and −0.77% for $P_r = 0$ and +2.80% and −0.33% for $P_r = 2.5\%$, respectively. The results also show that the mean value of each of the powers does not change much with variation of the channel length. The last row of the table presents the results obtained under simultaneous variations of the target parameters.

4.5 The SB-GNRFET-based 6T SRAM

In this section, the SB-GNRFET-based 6T SRAM cell depicted in Fig. 5a is simulated and compared with the Si CMOS design in terms of their stability. The transistor sizes of the 6T SRAM cell are obtained by satisfying the following two conditions: (1) ratio restrictions and (2) optimal layout density [34]. To satisfy these two conditions, the size of the pull-down transistors NM1 and NM2 should be greater than that of the pull-up transistors PM1 and PM2, while the size of the access transistors NM3 and NM4 should lie in between. Table 5 presents the transistor sizing for both the SB-GNRFET and Si-CMOS-based 6T SRAM cells. The simulations are performed at 25 °C with a nominal supply voltage of 0.5 V and 0.7 V for the SB-GNRFET and Si-CMOS design, respectively. The butterfly curve and N-curve of the 6T SRAM cells are shown in Fig. 20. All the noise margins are specified in these plots and are also presented in Table 6. The static power noise margin (SPNM) and the write trip power (WTP) are obtained using Eqs. (5) and (6). The SPNM and WTP are measures of the read stability and write-ability, respectively. A design with a high SPNM is more stable, while a design with a low WTP has better write-ability [19]. The SB-GNRFET-based 6T SRAM cell has better write-ability than the Si-CMOS design, but its stability is lower.

Table 4 The mean (μ) and standard derivation (std) of the results obtained using the normal distribution function

Parameter(s) varied	t_{CQ} (ps)				Leakage power (μW)				Dynamic power (μW)				Total power (μW)				EDP (10^{-27} W s^2)			
	$P_r = 0$		$P_r = 2.5\%$		$P_r = 0$		$P_r = 2.5\%$		$P_r = 0$		$P_r = 2.5\%$		$P_r = 0$		$P_r = 2.5\%$		$P_r = 0$		$P_r = 2.5\%$	
	$t_{CQ\text{-nom}}=4.65$		$t_{CQ\text{-nom}}=7.68$		$LP_{nom}=3.17$		$LP_{nom}=6.57$		$DP_{nom}=8.57$		$DP_{nom}=14.49$		$TP_{nom}=11.74$		$TP_{nom}=21.06$		EDP-$_{nom}=2.53$		EDP-$_{nom}=12.42$	
	μ	Std	μ	Std	μ	Std	μ	Std	μ	Std	μ	Std	μ	Std	μ	Std	μ	Std	μ	Std
V_{DD}	4.66	0.70	7.70	1.91	3.53	0.63	6.92	1.03	8.97	1.79	14.72	2.20	12.50	1.91	21.65	2.52	2.77	0.93	13.71	6.95
T_{ox}	4.60	0.15	7.62	0.68	3.25	0.04	6.74	0.10	8.63	0.13	14.55	0.18	11.88	0.13	21.29	0.21	2.51	0.17	12.47	2.22
N	4.60	0.60	7.58	0.31	3.13	0.01	6.61	0.06	8.52	0.08	14.38	0.12	11.65	0.08	20.99	0.14	2.47	0.07	12.09	1.00
L_{ch}	4.63	0.05	7.69	0.08	3.17	0.00	6.57	0.00	8.57	0.06	14.49	0.07	11.74	0.06	21.16	0.07	2.51	0.05	12.51	0.27
All	4.71	0.64	7.72	1.39	3.41	6.90	6.83	0.99	8.88	1.73	14.57	2.17	12.30	1.87	21.40	2.42	2.77	0.88	13.16	5.09

Table 5 The transistor sizing for the 6T SRAM cells

	SB-GNRFET			Si-CMOS
Transistor type	N_{ribb}	$2W_{sp}$ (nm)	W_G (nm)	W_G (nm)
Pull up	3	9.068	32	32
Pull down	6	13.401	90	90
Access	3	13.401	45	45

$$\mathrm{SPNM} = \mathrm{SVNM} \times \mathrm{SINM}, \tag{5}$$

$$\mathrm{WTP} = \mathrm{WTV} \times \mathrm{WTI}. \tag{6}$$

The effect of varying V_{DD} on the stability of the SB-GNRFET- and Si-CMOS-based 6T SRAM cells is shown in Fig. 21. The voltage margins (SVNM and WTV), the magnitude of the current margins (SINM and WTI), and the (hold, read, and write) noise margins increase with V_{DD}. These margins decrease when the line-edge roughness P_r is increased, as shown in Fig. 22.

5 Conclusions

The impact of PVT variations such as changes in the channel length, gate oxide thickness, number of dimer lines, and line-edge roughness on the timing parameters, power, and EDP of an SB-GNRFET-based FF is evaluated and analyzed. MC simulations are performed for statistical analysis of these variations. The results show that changing the number of dimer lines N from the nominal value of 12 to 13 has the greatest effect on the propagation delay (about +315.48%), while changing the operating temperature from its nominal value of 25 to 100 °C has the least effect. This variation affects the propagation delay and the total power by about −1.43% and −4.38%, respectively. With an increase of the supply voltage by 0.1 V above its nominal value, the total power changes by about 206.03% while the propagation delay decreases by about 13.44%. With scaling down of the technology node from 16 to 14 nm, the propagation delay and the total power decrease by nearly 2.25% and 18.52%, respectively. Moreover, the SB-GNRFET-based FF is better than the Si-CMOS and MG Si-CMOS designs in terms of the EDP. SB-GNRFETs have immense potential for use in digital circuit design. However, variations have a greater effect on SB-GNRFET circuits in the presence of line-edge roughness (LER); For example, the EDP increases by about 394.94%, 396.81%, 389.47%, 398.41%, and 375.09% when

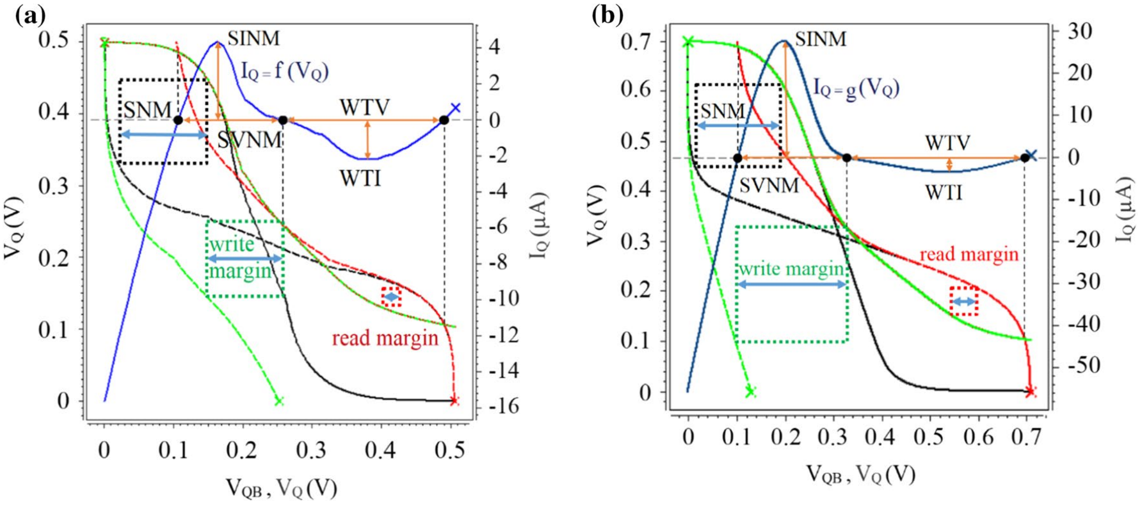


Fig. 20 The butterfly curve and N-curve of the 6T SRAM based on **a** SB-GNRFETs and **b** Si CMOS

Table 6 The noise margin values for both 6T SRAM designs

Noise margin type	CMOS design	SB-GNRFET design	Change
Hold (V)	0.17	0.12	×0.7
Read (V)	0.05	0.03	×0.60
Write (V)	0.23	0.10	×0.43
SVNM (V)	0.22	0.15	×0.68
SINM (μA)	27.58	4.31	×0.16
WTV (V)	0.36	0.24	×0.67
WTI (μA)	−3.51	−2.21	×0.63
SPNM (μW)	6.07	0.65	−89.29%
WTP (μW)	−1.26	−0.53	−57.94%

varying V_{DD}, T_{ox}, N, and L_{ch} or all these parameters simultaneously, respectively.

The stability of the SB-GNRFET-based SRAM cell is evaluated under variations of parameters such as the supply voltage and line-edge roughness; For instance, a +20% change of the supply voltage from its nominal value of 0.5 V results in an increase of about 19.67% and 47.80% in the static noise margin and the static current noise margin, while these parameters decrease by about 22.25% and 65.66%, respectively, when the line-edge roughness is 2.5%. Based on these results, the SB-GNRFET-based 6T SRAM exhibits better write-ability than the Si CMOS design.

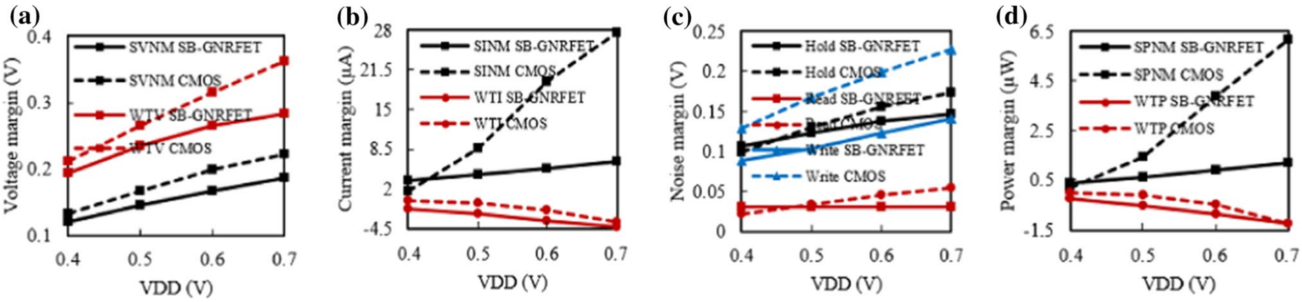


Fig. 21 The impact of V_{DD} on the stability of the SB-GNRFET- and Si-CMOS-based 6T SRAM cells in terms of the **a** voltage margins, **b** current margins, **c** noise margins, and **d** power margins

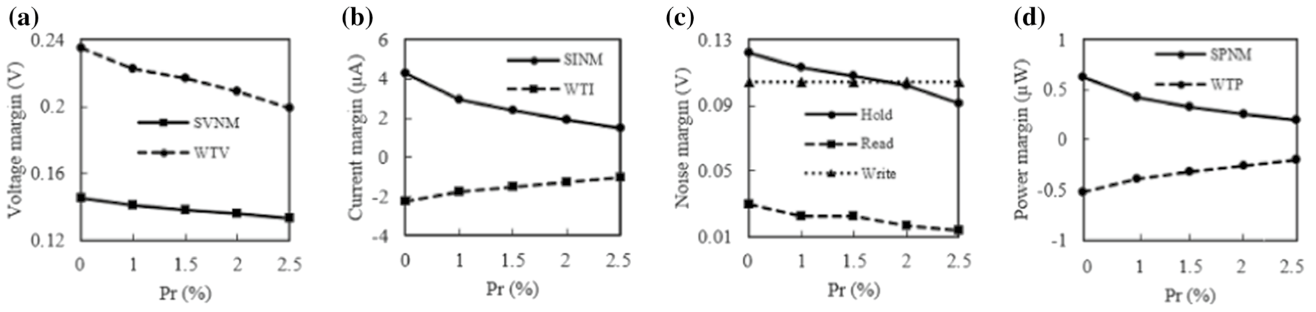


Fig. 22 The effect of P_r on the stability of the SB-GNRFET-based 6T SRAM cell in terms of the **a** voltage margins, **b** current margins, **c** noise margins, and **d** power margins

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References

1. Plummer, J.D., Griffin, P.B.: Material and process limits in silicon VLSI technology. Proc. IEEE **89**(3), 240–258 (2001). https://doi.org/10.1109/5.915373
2. Schwierz, F.: Two-dimensional electronics—prospects and challenges. J. Electron. (2016). https://doi.org/10.3390/electronics5020030
3. Novoselov, K.S., Fal, V., Colombo, L., Gellert, P., Schwab, M., Kim, K.: A roadmap for graphene. Nature **490**(7419), 192–200 (2012). https://doi.org/10.1038/nature11458
4. Geim, A.K., Novoselov, K.S.: The rise of graphene. Nat. Mater. **6**(3), 183–191 (2007). https://doi.org/10.1038/nmat1849
5. Castro Neto, A.H., Guinea, F., Peres, N.M.R., Novoselov, K.S., Geim, A.K.: The electronic properties of graphene. Rev. Mod. Phys. (2009). https://doi.org/10.1103/RevModPhys.81.109
6. Du, X., Skachko, I., Barker, A., Andrei, E.Y.: Approaching ballistic transport in suspended graphene. Nat. Nanotechnol. **3**(8), 491–495 (2008). https://doi.org/10.1038/nnano.2008.199
7. Balandin, A.A., Ghosh, S., Bao, W., Calizo, I., Teweldebrhan, D., Miao, F., et al.: Superior thermal conductivity of single-layer graphene. Nano Lett. **8**(3), 902–907 (2008). https://doi.org/10.1021/nl0731872
8. Park, S., Ruoff, R.S.: Chemical methods for the production of graphenes. Nat. Nanotechnol. **4**(4), 217–224 (2009). https://doi.org/10.1038/nnano.2009.58
9. Banadaki, Y., Mohsin, K., Srivastava, A.: A graphene field effect transistor for high temperature sensing applications. Proc. (SPICE Smart Structure/NDE: Nano-, Bio-, and Info-Tech Sens Syst SSN06) (2014). https://doi.org/10.1117/12.2044611
10. Heer, De, Walt, A., Berger, C., Wu, X., First, P.N., Conard, E.H., Li, A., Li, T., Sprinkle, M., Hass, J., Sadowski, M.L., Potemski, M., Martinez, G.: Epitaxial graphene. Solid State Commun. (2007). https://doi.org/10.1016/j.ssc.2007.04.023
11. Gholipour, M., Chen, Y.-Y., Sangai, A., Masoumi, N., Chen, D.: Analytical SPICE-compatible model of Schottky-barrier-type GNRFETs with performance analysis. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. (2016). https://doi.org/10.1109/TVLSI.2015.2406734
12. Joshi, S., Albalawi, U.: Statistical process variation analysis of Schottky-barrier type GNRFET for RF application. Int. Conf. Current Trends Comput., Electr., Electron. Commun. (CTCEEC) (2017). https://doi.org/10.1109/CTCEEC.2017.8455156
13. Chen, Y.-Y., Sangai, A., Rogachev, A., Gholipour, M., Iannaccone, G., Fiori, G., et al.: A SPICE-compatible model of MOS-type graphene nano-ribbon field-effect transistors enabling gate-and circuit-level delay and power analysis under process variation. IEEE Trans. Nanotechnol. (2015). https://doi.org/10.1109/TNANO.2015.2469647
14. Gholipour, M., Chen, Y.-Y., Sangai, A., Chen, D.: Highly accurate SPICE-compatible modeling for single-and double-gate GNRFETs with studies on technology scaling. Proc. Conf. Design, Autom. Test Europe (2014). https://doi.org/10.7873/DATE.2014.133
15. Chen, Y.-Y., Rogachev, A., Sangai, A., Iannaccone, G., Fiori, G., Chen, D.: A SPICE-compatible model of graphene nano-ribbon field-effect transistors enabling circuit-level delay and power analysis under process variation. Design, Autom. Test Europe Conf. Exhib. (DATE) (2013). https://doi.org/10.7873/DATE.2013.359
16. Anil, D.G., Bai, Y., Choi, Y.: Performance evaluation of ternary computation in SRAM design using graphene nanoribbon field effect transistors. IEEE 8th Ann. Comput. Commun. Workshop Conf. (CCWC) (2018). https://doi.org/10.1109/CCWC.2018.8301723
17. Aradhya, H.R., Madan, H., Megaraj, T., Suraj, M., Karthik, R., Muniraj, R.: GNRFET based 8-bit ALU. Int. J. Electron. Commun. Eng. (IJECE) **5**(1), 45–54 (2016)
18. Joshi, S., Mohanty, S.P., Kougianos, E., Yanambaka, V.P.: Graphene nanoribbon field effect transistor based ultra-low energy SRAM design. IEEE Int. Symp. Nanoelectron. Inform. Syst. (iNIS) (2016). https://doi.org/10.1109/iNIS.2016.028
19. Singh, P., Chandel, R., Sharma, N.: Stability analysis of SRAM cell using CNT and GNR field effect transistors. Int. Conf. Contemp. Comput. (IC3) (2017). https://doi.org/10.1109/IC3.2017.8284335
20. Forzan, C., Pandini, D.: Statistical static timing analysis: a survey. Integration **42**(3), 409–435 (2009). https://doi.org/10.1016/j.vlsi.2008.10.002
21. Mittal, S.: A survey of architectural techniques for managing process variation. ACM Comput. Surv. (CSUR) **48**(4), 54 (2016). https://doi.org/10.1145/2871167
22. Liu, J.J.-H., Zeng, J.-K., Hong, A.-S., Chen, L., Chen, C.C.P.: Process-variation statistical modeling for VLSI timing analysis. Int. Symp. Qual. Electron. Design. (isqed 2008) (2008). https://doi.org/10.1109/ISQED.2008.4479828
23. Sapatnekar, S.S.: Overcoming variations in nanometer-scale technologies. IEEE J. Emerg. Sel. Top. Circuits Syst. **1**(1), 5–18 (2011). https://doi.org/10.1109/JETCAS.2011.2138250

24. Pandit, S., Mandal, C., Patra, A.: Nano-scale CMOS analog circuits: models and CAD techniques for high-level design, 1st edn. CRC Press, London (2014). https://doi.org/10.1201/9781315216102
25. Cheng, L.: Statistical analysis and optimization for timing and power of VLSI circuits. University of California, Los Angeles (2010)
26. Bhunia, S., Mukhopadhyay, S.: Low-power variation-tolerant design in nanometer silicon. Springer Science & Business Media, Berlin (2010). https://doi.org/10.1007/978-1-4419-7418-1
27. Mohsin, A.: Graphene synthesis and characterization on copper. https://doi.org/10.17077/etd.xkpszqo8 (2012)
28. Chilstedt, S., Dong, C., Chen, D.: Carbon nanomaterial transistors and circuits. In: Transistors: types, materials and applications, pp. 1–34. Nova Sience Pub., New York (2010)
29. Son, Y.-W., Cohen, M.L., Louie, S.G.: Energy gaps in graphene nanoribbons. Phys. Rev. Lett. **97**(21), 216803 (2006). https://doi.org/10.1103/PhysRevLett.97.216803
30. Singh, V., Joung, D., Zhai, L., Das, S., Khondaker, S.I., Seal, S.: Graphene based materials: past, present and future. Prog. Mater Sci. **56**(8), 1178–1271 (2011). https://doi.org/10.1016/j.pmatsci.2011.03.003
31. Marmolejo-Tejada, J.M., Velasco-Medina, J.: Review on graphene nanoribbon devices for logic applications. Microelectron. J. **48**, 18–38 (2016). https://doi.org/10.1016/j.mejo.2015.11.006
32. Chen, Y.-Y., Sangai, A., Gholipour, M., Chen, D.: Graphene nanoribbon field-effect transistors as future low-power devices. Int. Symp. Low Power Electron. Design (ISLPED) (2013). https://doi.org/10.1109/islped.2013.6629286
33. Lin, J.-F., Sheu, M.-H., Hwang, Y.-T., Wong, C.-S., Tsai, M.-Y.: Low-power 19-transistor true single-phase clocking flip-flop design based on logic structure reduction schemes. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **25**(11), 3033–3044 (2017). https://doi.org/10.1109/TVLSI.2017.2729884
34. Weste, N. H., Harris, D.: CMOS VLSI design: a circuits and systems perspective, 4th edn. Pearson (2011)
35. Phyu, M.W., Goh, W.L., Yeo, K.S.: A low-power static dual edge-triggered flip-flop using an output-controlled discharge configuration. IEEE Int. Symp. Circuits Syst. (2015). https://doi.org/10.1109/ISCAS.2005.1465116
36. Harris, D.M.: Sequential element timing parameter definition considering clock uncertainty. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **23**(11), 2705–2708 (2014). https://doi.org/10.1109/TVLSI.2014.2364991
37. Phyu, M. W.: Low-voltage low-power CMOS flip-flops. PhD Thesis, Nanyang Technological University 2009. https://doi.org/10.32657/10356/46774
38. Liu, Z., Kursun, V.: Characterization of a novel nine-transistor SRAM cell. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. (2008). https://doi.org/10.1109/TVLSI.2007.915499
39. Prasad, G., Anand, A.: Statistical analysis of low-power SRAM cell structure. Analog Integr. Circ. Sig. Process **82**(1), 349–358 (2015). https://doi.org/10.1007/s10470-014-0463-1
40. Almeida, R.B., Butzen, P.F., Meinhardt, C.: 16NM 6T and 8T CMOS SRAM cell robustness against process variability and aging effects. Symp. Integr. Circuits Syst. Design (SBCCI) (2018). https://doi.org/10.1109/sbcci.2018.8533253
41. Grossar, E., Stucchi, M., Maex, K., Dehaene, W.: Read stability and write-ability analysis of SRAM cells for nanometer technologies. IEEE J. Solid-State Circuits **41**(11), 2577–2588 (2006). https://doi.org/10.1109/JSSC.2006.883344
42. Nayak, D., Acharya, D., Rout, P.K., Mahapatra, K.: Design of low-leakage and high stable proposed SRAM cell structure. Int. Conf. Electron Commun. Syst. (2014). https://doi.org/10.1109/ECS.2014.6892682
43. Predictive Technology Model. [Online]. Available: https://ptm.asu.edu/
44. Lim, W., Chin, H.C., Lim, C.S., Tan, M.L.P.: Performance evaluation of 14 nm FinFET-based 6T SRAM cell functionality for DC and transient circuit analysis. J. Nanomater. **2014**, 105 (2014). https://doi.org/10.1155/2014/820763

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