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A novel 2-D analytical model for the electrical characteristics of a gate-all-around heterojunction tunnel field-effect transistor including depletion regions

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Abstract
A new two-dimensional analytical model is proposed for the electrical attributes of a gate-all-around heterojunction tunnel field-effect transistor, including the potential distribution, lateral and vertical electric fields, drain current, subthreshold swing, and threshold voltage. The potential distribution in the device is obtained by using the two-dimensional (2-D) Poisson equation, including the depletion regions across the source–channel, channel, and drain–channel regions. The drain current of the proposed device is derived by combining parameters such as the band-to-band generation rate, lateral electric field, and channel thickness as well as the shortest tunneling path in Kane's model. The threshold voltage is obtained from the second derivative of the drain current. The effects of the depletion regions are also included in the model to obtain accurate results. The results are validated against ATLAS technology computer-aided design (TCAD) simulations with the SILVACO tool, revealing excellent agreement.

Keywords Analytical modeling · Gate-all-around · Heterojunction device · Tunnel field-effect transistor · Potential distribution · Electric field · Drain current · Poisson's equation

1 Introduction

In complementary metal–oxide–semiconductor (CMOS) technology, the tunneling field-effect transistor has attracted enormous attention from researchers due to its excellent electrical characteristics such as low subthreshold swing (i.e., less than 60 mV/dec) and high ON/OFF current ratio with low OFF leakage current [1–7]. Due to their low OFF leakage current, tunnel FETs are excellent devices for use in low-power very large-scale integration (VLSI) applications [8]. However, two-dimensional tunnel FETs provide a low ON current due to the poor efficiency of the band-to-band tunneling (BTBT) mechanism, because of the wide bandgap in the device. In current semiconductor technology, gate-all-around nanowire (GAANW) tunnel FETs are considered as alternate devices to improve the ON current and reduce the subthreshold swing (SS). The greatest advantage of nanowire tunnel FETs is their excellent gate control over the channel, due to which short-channel effects are greatly reduced. Recently, many studies related to fabrication methods and process technology for nanowire tunnel FETs have been published [9–14].

An analytical model to obtain the drain current of a gate-all-around nanowire tunnel FET was proposed by Lu and Seabaugh [14]. However, that model did not include the differences caused in the drain current when the drain-to-source voltage applied to the device is varied. Various analytical models for homojunction tunnel FETs with different structures have also been proposed by researchers with the aim of enhancing the drain current characteristics. Vishnoi and Kumar proposed an analytical model for a gate-all-around nanowire tunnel FET by segregating two regions across the source and channel. However, the variations of the drain region are not account for in their model [15]. Reza et al. suggested an analytical model for a homojunction cylindrical gate-all-around tunnel FET using the superposition principle, but their work did not include the threshold voltage of the device [16]. Bagga and Dasgupta introduced an analytical model to study the surface potential and drain current of a gate-all-around (GAA) triple-metal tunnel FET by solving the

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Poisson equation using a parabolic approximation and applying Kane's model for the drain current. Again in this model, only the surface potential, electric field, and drain current are obtained, whereas other important factors that determine the performance of a tunnel FET such as the subthreshold swing and threshold voltage are not explored [17, 18].

Very few studies discussing the schematic cross section of and simulation methods for heterojunction tunnel FETs are available in literature. Kumar et al. proposed a model for schematic double-gate heterojunction TFETs with germanium in the source and silicon in the drain in both the accumulation/inversion and depletion modes [19]. The forward gain is high while the reverse gain is low for heterojunction devices in comparison with homojunction transistors, which enables them to offer high-frequency performance. Moreover, the bandgap in a heterojunction device can be adjusted depending on the application, indicating that SiGe junctions enable more bandgap tuning than silicon-only technology.

A heterojunction (HJ) is formed in a GAA-HJTFET when two semiconductors (germanium and silicon) with dissimilar bandgaps are placed in conjunction or layered together. The conduction-band energy and valence-band energy change abruptly at the heterojunction. The magnitude of these changes determines the band alignment and the effective bandgap in the semiconductor heterojunction. Due to this, the ON-state current performance improves, short-channel effects are reduced, and a subthreshold swing below 45 mV/dec can be obtained.

In the Si–Ge heterojunction, the energy band of the device moves downwards to the intrinsic region, which improves the I_{ON} current and also suppresses the ambipolar behavior, thereby reducing the subthreshold swing. Researchers have demonstrated that increasing the Ge concentration in such devices from 7% to 25% can increase the drain current by 15-fold at a constant subthreshold slope and also decrease the I_{OFF} current.

An analytical model for a heterojunction gate-all-around tunnel FET is presented herein. The surface potential is modeled across the three regions of the proposed device, viz. the source–channel depletion region, channel depletion region and channel–drain depletion region. Differentiation of the surface potential results in the electric field. The drain current is modeled using Kane's model. The results of the model are validated against ATLAS-based TCAD simulations.

2 Device structure

Figure 1a shows a three-dimensional (3-D) structural view of the GAA-HJTFET. The assumptions of the model include a source length of 20 nm with germanium material having a doping concentration of $N_1 = 1 \times 10^{20}$ cm^{-3}, a channel length of 50 nm with a doping concentration of $N_2 = 1 \times 10^{16}$ cm^{-3}, and a drain length of 20 nm with silicon material having a doping concentration of $N_3 = 5 \times 10^{18}$ cm^{-3}. Figure 1b shows a cross-sectional schematic view of the GAA-HJTFET device. The potential distribution along the radius is similar to that in the y-direction for a double-gate (DG)-TFET. Thus, this cross-sectional schematic view is considered in the analytical model, considering the source–channel (R_1), channel (R_2), and drain–channel (R_3) depletion regions with lengths of L_1, L_2, and L_3, respectively.

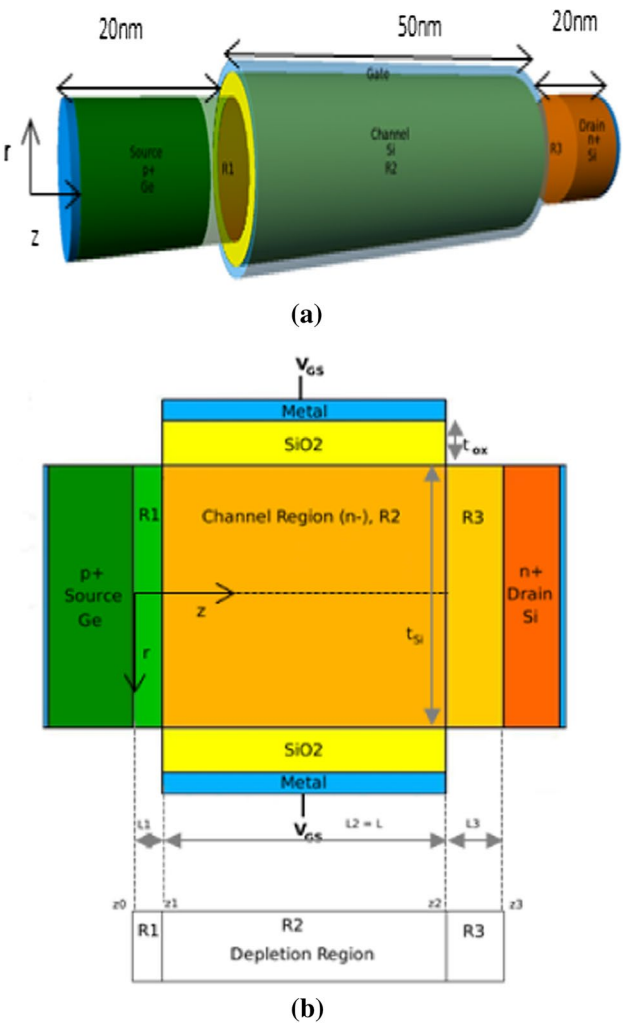

Fig. 1 **a** The 3-D structure of the GAA-HJTFET. **b** A cross-sectional schematic diagram of the GAA-HJTFET

3 Model formulation

The cross-sectional schematic view of the GAA-HJTFET shown in Fig. 1b is considered for the analytical modeling. The z- and r-axes represent the coordinates of the device, with

the following parameters: silicon thickness (t_{Si}) and channel oxide thickness (t_{ox}). ψ_0, ψ_1, ψ_2, and ψ_3 are the junction potentials at $z = 0$, $z_1 = L_1$,$z_2 = L_1 + L_2$, and $z_3 = L_1 + L_2 + L_3$, respectively.

3.1 The analytical modeling of the surface potential

Let $\psi_i(r, z)$ be the surface potential distribution function along channel region R_i, where $i = 1$, 2, or 3. The two-dimensional (2-D) Poisson's equation is given as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_i(r,z)}{\partial r}\right) + \frac{\partial^2 \psi_i(r,z)}{\partial z^2} = -\frac{qN_i}{\varepsilon_{Si}} \quad i = 1,\ 2,\ 3, \tag{1}$$

where q is the electron charge and N_i is the doping concentration of each region. The doping concentration of the source region is assumed to be $N_1 = 1 \times 10^{20}\,\mathrm{cm}^{-3}$, that of the channel region to be $N_2 = 1 \times 10^{16}\,\mathrm{cm}^{-3}$, and that of the drain region to be $N_3 = 5 \times 10^{18}\,\mathrm{cm}^{-3}$. Using a parabolic approximation, the 2-D channel potential $\psi_i(r, z)$ in region R_i can be expressed as

$$\psi_i(r,z) = a_{0i}(z) + a_{1i}(z)r + a_{2i}(z)r^2 \quad \text{where} \quad i = 1, 2, 3, \tag{2}$$

where $a_{0i}(z)$, $a_{1i}(z)$ and $a_{3i}(z)$ are arbitrary functions of z, defined by the boundary conditions [15]

$$(1)\ \psi_i(r,z)\big|_{r=R} = \psi_s(z). \tag{3}$$

The potential for regions R_1, R_2, and R_3 at $r = R$ equals the surface potential. The electric field at the center of the channel region is zero:

$$(2)\ \left.\frac{\partial \psi_i(r,z)}{\partial r}\right|_{r=0} = 0. \tag{4}$$

The electric field distribution at $r = R$ is equal across the boundary between the silicon substrate and SiO_2 oxide, being given by

$$(3)\ \left.\frac{\partial \psi_i(r,z)}{\partial r}\right|_{r=R} = \frac{C'_{ox}}{\varepsilon_{Si}R}\left[\frac{\psi_G - \psi_s(z)}{\ln(1+\frac{t_{ox}}{R})}\right], \tag{5}$$

where $\psi_G = V_{GS} - \varphi_m + \chi + \frac{E_g}{2}$ and $i = 1$, 2, 3 for the three different depletion regions, the gate work function φ_m is 4 eV, the electron affinity of silicon is given by $\chi = 4.05$ eV, the oxide capacitance is $C'_{ox} = \varepsilon_{ox}/t$, V_{GS} is the gate-to-source voltage, $t = t_{ox}$ is for region R_2, and $t = \left(\pi/2\right)t_{ox}$ for regions R_1 and R_3. The radius of the channel is $R = t_{Si}$.

Using Eqs. (3)–(5) to solve Eq. (2) yields

$$a_{0i} = \psi_s(z) - \frac{C'_{ox}}{2\varepsilon_{Si}}\left[\frac{\psi_G - \psi_s(z)}{\ln(1+\frac{t_{ox}}{R})}\right], \tag{6}$$

$$a_{1i} = 0, \tag{7}$$

$$a_{2i} = \frac{\varepsilon_{ox}}{2\varepsilon_{Si}R^2}\left[\frac{\psi_G - \psi_s(z)}{\ln(1+\frac{t_{ox}}{R})}\right]. \tag{8}$$

The relationship between the surface potential and channel potential $\psi_i(r, z)$ is defined by $\psi_{s,i}(z) = \psi_i\left(\pm t_{Si}/2, z\right)$.

From Eqs. (6)–(8), it can be deduced that

$$\psi_i(r,z) = \psi_{0i}(z) + \left(\frac{r^2}{\lambda^2 R^2} - \frac{1}{\lambda^2}\right)\left(\psi_G - \psi_{0i}(z)\right), \tag{9}$$

$$\psi_{s,i}(z) = \psi_{0i}(z) + \left(\frac{t_{Si}^2}{4\lambda^2 R^2} - \frac{1}{\lambda^2}\right)\left(\psi_G - \psi_{0i}(z)\right), \tag{10}$$

where

$$\psi_{0i}(z) = \psi_i(0,z) \quad \text{i.e when radius } r = 0$$
$$\lambda^2 = \frac{2\varepsilon_{Si}}{\varepsilon_{ox}}\left(\ln\left(1+\frac{t_{ox}}{R}\right)\right).$$

At $r = 0$, the 2-D Poisson Eq. (1) can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_i(r,z)}{\partial r}\right)\bigg|_{r=0} + \left.\frac{\partial^2 \psi_i(r,z)}{\partial z^2}\right|_{r=0} = -\left.\frac{qN_i}{\varepsilon_{Si}}\right|_{r=0}. \tag{11}$$

Substituting Eq. (2) into Eq. (11) yields the following differential equation in terms of the center potential:

$$\frac{\partial^2 \psi_{0i}(z)}{\partial^2 z} - \eta_i^2 \psi_{0i}(z) = -\eta_i^2 P_i, \tag{12}$$

where $P_i = \frac{qN_i}{\eta_i^2 \varepsilon_{Si}} + \psi_G$ and $\eta_i^2 = \frac{4}{\lambda^2 R^2}$..

The general solution of Eq. (12) is

$$\psi_{0i}(z) = A_i \exp(\eta_i(z - z_{i-1})) + B_i \exp(-\eta_i(z - z_{i-1})) + P_i, \tag{13}$$

where

$$A_i = \frac{-1}{2\sinh\eta_i L_i}[\psi_{i-1}(z)\exp(-\eta_i L_i) - \psi_i(z) - P_i(\exp(-\eta_i L_i) + 1)], \tag{14}$$

$$B_i = \frac{1}{2\sinh\eta_i L_i}[\psi_{i-1}(z)\exp(\eta_i L_i) - \psi_i(z) - P_i(\exp(\eta_i L_i) + 1)]. \tag{15}$$

The length of region R_i is $L_i = z_i - z_{i-1}$ $(i = 1, 2, 3)$ and the surface potential at $z = z_i$ is $\psi_i = \psi_{s,i}(z_i)$ as shown in Fig. 1b.

The surface potential across the regions can be obtained by using the following boundary conditions [18, 20]:

$$\psi_0 = \psi_1(r,0) = V_{\text{bis}}, \tag{16}$$

$$\psi_1 = \psi_2(r,L_1), \tag{17}$$

$$\psi_2 = \psi_2(r,L_1+L_2), \tag{18}$$

$$\psi_3 = \psi_3(r,L_1+L_2+L_3) = V_{\text{bis}} + V_{\text{DS}}, \tag{19}$$

where

$$V_{\text{bis}} = -\frac{1}{q}\left[(\chi_1-\chi_2)+0.5(E_{\text{g1}}-E_{\text{g2}}) + qV_{\text{T}}(\ln(N_1/n_i)\right]$$

is the built-in potential. The electron charge is q, V_{T} is the thermal voltage, and n_i is the electron concentration.

ψ_1 and ψ_2 are intermediate surface potentials obtained by using the continuity property of the lateral electric field thus [18]:

$$\psi_{\text{s},i}(z)\big|_{z=z_i} = \psi_{\text{s},i+1}(z)\big|_{z=z_i}, \tag{20}$$

$$\varepsilon\frac{\partial\psi_{\text{s},i}(z)}{\partial z}\bigg|_{z=z_i} = \varepsilon\frac{\partial\psi_{\text{s},i+1}(z)}{\partial z}\bigg|_{z=z_i}. \tag{21}$$

Using Eqs. (20)–(21) in (10) along with Eqs. (13)–(15) yields the intermediate potentials as

$$\psi_1 = \frac{1}{y_1}\left[\frac{(x-1)}{\sinh\eta_1 L_1}\{\eta_1\psi_0+\eta_1 P_1(1+\cosh\eta_1 L_1) - P_2\sinh\eta_1 L_1\}+x\psi_{\text{G}}\right], \tag{22}$$

$$\psi_2 = \frac{1}{y_2}\left[\frac{(x-1)}{\sinh\eta_2 L_2}\{\eta_2\psi_1+\eta_2 P_2(1+\cosh\eta_2 L_2) - P_3\sinh\eta_2 L_2\}+x\psi_{\text{G}}\right], \tag{23}$$

where

$$x = \left(\frac{t_{\text{Si}}^2}{4\lambda^2R^2}-\frac{1}{\lambda^2}\right)$$

$$y_i = \left[1-\eta_i(x-1)\coth\eta_i L_i\right] \quad i=1,2,$$

3.2 The modeling of the electric field

The vertical and lateral electric fields $E_{ri}(r,z)$ and $E_{zi}(r,z)$ are obtained by differentiation of the potential in Eqs. (2) and (13) thus:

$$E_{ri}(r,z) = 2r\frac{C'_{\text{ox}}}{2\varepsilon_{\text{Ge}}R^2}\left[\frac{\psi_{\text{G}}-\psi_{\text{s}}(z)}{\ln(1+\frac{t_{\text{ox}}}{R})}\right], \tag{24}$$

$$E_{zi}(r,z) = -\frac{\partial\psi_i(r,z)}{\partial z} = \eta_i[-A_i\exp(\eta_i(z-z_{i-1})) + B_i\exp(-\eta_i(z-z_{i-1})]. \tag{25}$$

3.3 The lengths of the depletion regions

L_1 and L_3 are determined as the lengths of the regions R_1 and R_3 that occur due to the source and drain charge depletion regions. A TFET can be considered to be a gate diode whose potential can be regulated by its gate voltage [4]. To consider the impact of the two terminals on each other, L_1 and L_3 should be calculated by applying $E_r = 0$ at $r = r_0$ and $r = r_2$ before deriving the potentials ψ_2 and ψ_3. To avoid the complexity of this calculation, a simple approximation is made by considering the source–channel and drain–channel regions separately using Refs. [18, 21] as follows:

$$L_1 = \sqrt{2\varepsilon_{\text{Si}}(P_2-\psi_0)/(qN_1)}, \tag{26}$$

$$L_3 = \sqrt{2\varepsilon_{\text{Si}}(\psi_3-P_2)/(qN_3)}. \tag{27}$$

Since P_2 is dependent on V_{GS}, the L_1 and L_3 values are smaller than for the DG-TFET. Because of these smaller depletion lengths, the conduction of the device improves while the drain current is simultaneously increased.

3.4 The modeling of the drain current

Based on Kane's model [21], the drain current of the device is determined from the band-to-band generation rate in the device volume [18] as

$$I_{\text{d}} = q\int_{\text{Volume}} A_{\text{Kane}}E_{z2}(r,z) \times E_{\text{avg}}^{\alpha-1}\exp\left(-\frac{B_{\text{Kane}}}{E_{\text{avg}}}\right)\text{d}V), \tag{28}$$

where $A_{\text{Kane}} = 4\times10^{14}\,\text{cm}^{1/2}\,\text{V}^{-5/2}\,\text{s}^{-1}$ and $B_{\text{Kane}} = 1.9\times10^7\,\text{V/cm}$ are Kane's constant parameters. $E_{\text{avg}} = E_{\text{g}}/ql_{\text{path}}$ is the average electric field [18]. l_{path} is the tunneling path distance, from the shortest tunneling path distance L_{min} to the largest tunneling path distance L_{max}, $E_{z2}(r,z)$ is the lateral electric field in channel region R_2. For indirect-bandgap materials, the material constant α is 2.5, while for direct-bandgap materials the value tends to be 2. The surface potential changes by E_{g}/q (unit bandgap

potential) [22] when the charges tunnel over the tunneling distance from $z=0$ to $z=L_{\min}$ in the channel region, which is denoted as the shortest tunneling path distance $L_{\min}$. This equation can thus [18] be written as

$$\psi_{s,2}(L_{\min}) - \psi_0 = \frac{E_g}{q}. \tag{29}$$

Equation (10) then yields

$$A_2 \exp(\eta_2 L_{\min}) + B_2 \exp(-\eta_2 L_{\min}) = X, \tag{30}$$

where

$$X = \frac{1}{1-k}\left[\psi_0 + \frac{E_g}{q} - k\psi_G - (1-k)P_2\right]$$
$$k = \frac{1}{\lambda^2}\left(\frac{t_{Si}^2}{4R^2} - 1\right),$$

$$I_d = q \int_{-t_{Si}/2}^{t_{Si}/2} \left(\int_{L_{\min}}^{L_{\max}} A_{Kane} E_{z2}(r,z) E_{avg}^{\alpha-1} \times \exp\left(-\frac{B_{Kane}}{E_{avg}}\right) dz \right) dr. \tag{31}$$

Substituting Eq. (23) with $i=2$ into Eq. (30), the drain current after integration is given by

$$I_d = I_0 \left[\int_{L_{\min}}^{L_{\max}} \left(\frac{A_2 \exp(-\mu_1 z)}{z^{\alpha-1}} - \frac{B_2 \exp(-\mu_2 z)}{z^{\alpha-1}} \right) dz \right], \tag{32}$$

where

$$I_0 = A_{Kane} E_g^{\alpha-1} q^{2-\alpha} \eta_2 t_{Si} \tag{33}$$

is the direct-current (DC) component

$$\mu_1 = \left((qB_{Kane}/E_g) - \eta_2 \right),$$
$$\mu_2 = \left((qB_{Kane}/E_g) + \eta_2 \right). \tag{34}$$

The variation of $1/z^{\alpha-1}$ within the interval $L_{\min} \le z \le L_{\max}$ is negligible compared with the exponential term [22]. Since the drain current cannot be expressed in closed form, Eq. (32) can be approximated as [18, 22]

$$I_d \approx I_0 \left[-\frac{A_2}{\mu_1}\left(M_{L_{\max}} - M_{L_{\min}}\right) + \frac{B_2}{\mu_2}\left(N_{L_{\max}} - N_{L_{\min}}\right) \right], \tag{35}$$

where M_z and N_z are expressed as

$$M_z = \frac{\exp(-\mu_1 z)}{z^{\alpha-1}}, \quad N_z = \frac{\exp(-\mu_2 z)}{z^{\alpha-1}}. \tag{36}$$

Note that $M_{L_{\max}} \ll M_{L_{\min}}$ and $N_{L_{\max}} \ll N_{L_{\min}}$, since $L_{\max} > L_{\min}$. Thus, the drain current can be further approximated as [18]

$$I_d \approx I_0 \left[\frac{A_2 M_{L_{\min}}}{\mu_1} - \frac{B_2 N_{L_{\max}}}{\mu_2} \right]. \tag{37}$$

3.5 The threshold voltage using the SD method

Among the various methods available for extracting the threshold voltage, the transconductance extrapolation method (GMLE) and second-derivative (SD) method have been proved to provide accurate and more practical results [23]. The gate voltage applied to the device at which its transconductance g_m' reaches the maximum value is defined as the threshold voltage (V_{th}) [22, 23]:

$$g_m' = \frac{\partial g_m}{\partial V_{GS}}, \tag{38}$$

where g_m is the transconductance, obtained as

$$g_m = \frac{\partial I_d}{\partial V_{GS}}. \tag{39}$$

3.6 The threshold voltage using the minimum channel potential method

The minimum surface potential distribution along the channel region can be obtained as

$$\psi_{s,\min} = 2\sqrt{A_2 B_2} + \frac{qN_s}{\eta_2 \varepsilon_{Si}} + \psi_G. \tag{40}$$

For the threshold condition [24], this gives

$$\psi_{s,\min} = 2\varphi_F \tag{41}$$

and

$$V_{GS} = V_{th}. \tag{42}$$

Using Eqs. (40) and (41), a quadratic approximation for the threshold voltage can be obtained as [21]

$$AV_{\text{th}}^2 + BV_{\text{th}} + C = 0. \tag{43}$$

4 Results and discussion

In this section, the results obtained using the proposed analytical model for the GAA-HJTFET are validated against ATLAS TCAD-based simulation data. Germanium (Ge) is employed at the source. Aluminum with a work function of $\varphi_{\text{m}} = 4.05$ eV is used as the gate metal, and the results are compared with a homojunction GAA TFET. The variation of the surface potential across the three regions, viz. the source–channel, channel, and drain–channel regions, for different ramping gate voltages is shown in Fig. 2. The sharp changes at the source–channel are due to the high band-tuning property of the heterojunction Si–Ge material, which remains constant across the entire channel region. As the gate-to-source voltage is increased, the potential across the entire channel region (including the source and drain junctions) also shoots up. For a considerable increase in the gate-to-source voltage, the source depletion region R_1 extends out towards the source, whereas the drain depletion region R_3 is shortened due to the variations on the higher and lower sides of the reverse-bias voltages at the source–channel and drain–channel junctions.

Figure 3 shows the variation of the surface potential for diverse drain-to-source voltages V_{DS}, in which the channel potential is the same and the device is found to vary little, barring the drain depletion region R_3. This variation across the drain implies a reduced drain-induced barrier lowering (DIBL) effect, as it is nearly independent of V_{DS}. The variation of the lateral (E_z) and vertical (E_r) electric field in the channel region compared with that of the homojunction GAA TFET is shown in Fig. 4.

Due to the smaller values of L_1 and L_3, a higher lateral electric field is obtained in the tunneling region. It is observed that the homojunction GAA TFET shows a peak magnitude variation at both the source–channel and drain–channel junctions, while the GAA-HJTFET shows a magnitude variation at only the source–channel junction and is nearly zero in the entire channel region. The variation of the drain current compared with the homojunction GAA TFET is shown in Fig. 5, clearly indicating that the threshold voltage is lower while the ON current increases

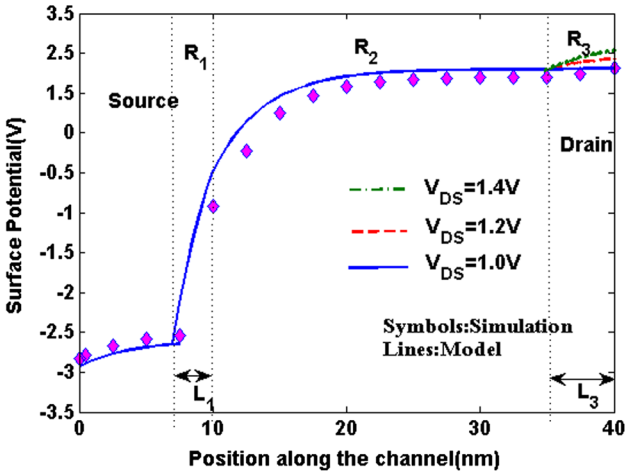

Fig. 3 The surface potential along the channel for different V_{DS} values of 1, 1.2, and 1.4 V with $L_2 = 50$ nm, $t_{\text{Si}} = 12$ nm, and $V_{\text{GS}} = 1$ V

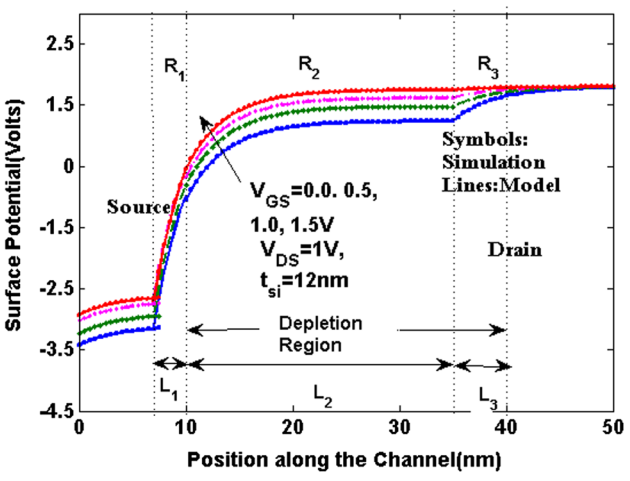

Fig. 2 The surface potential distribution along the channel for different V_{GS} values of 0, 0.5, 1, and 1.5 V with $L_2 = 50$ nm, $t_{\text{Si}} = 12$ nm, and $V_{\text{DS}} = 1$ V

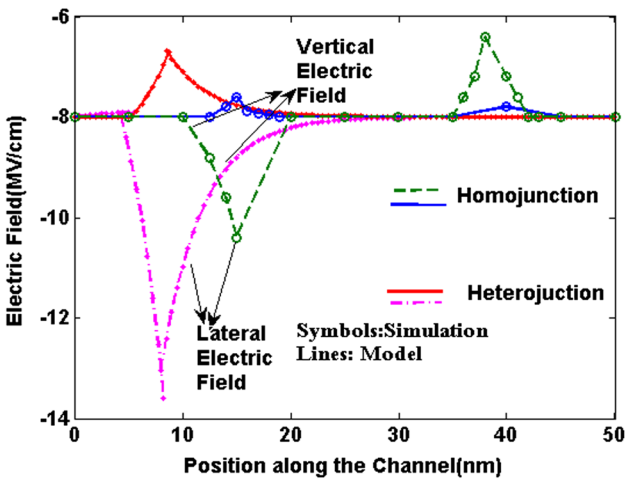

Fig. 4 The variation of the lateral and vertical electric fields along the channel for the homojunction GAA TFET and GAA-HJTFET

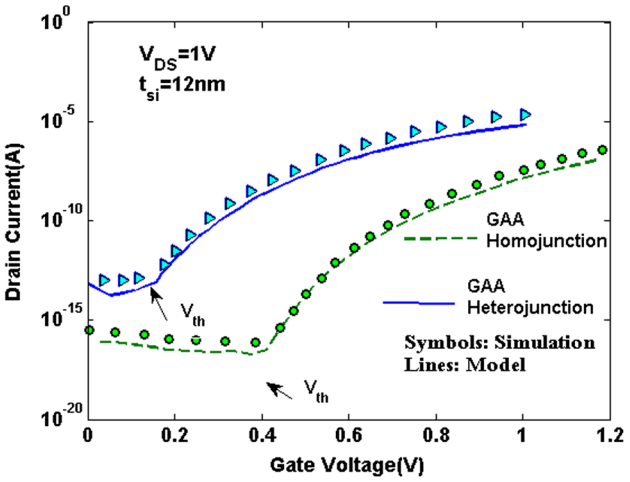

Fig. 5 The variation of the drain current with the gate-to-source voltage (V_{GS})

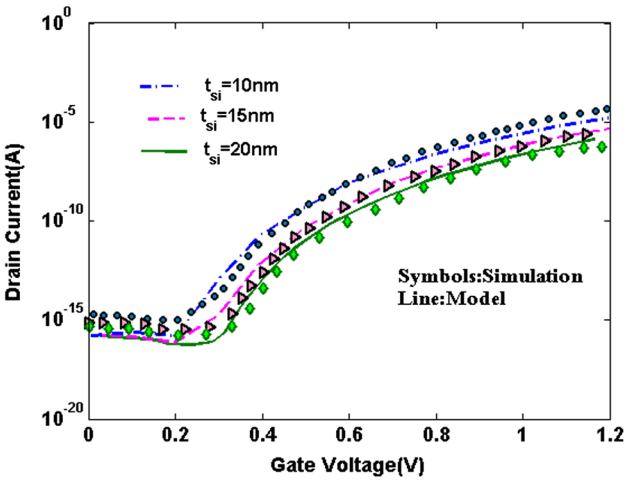

Fig. 6 The I_d–V_{GS} characteristics for different channel thicknesses t_{Si} of 10 nm, 15 nm, and 20 nm

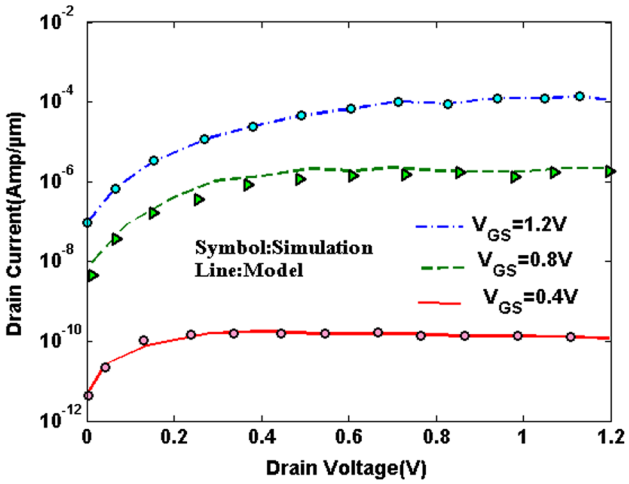

Fig. 7 The I_d–V_{DS} characteristics for different gate-to-source voltages V_{GS} of 0.8 V, 1 V, and 1.2 V with t_{Si} = 15 nm

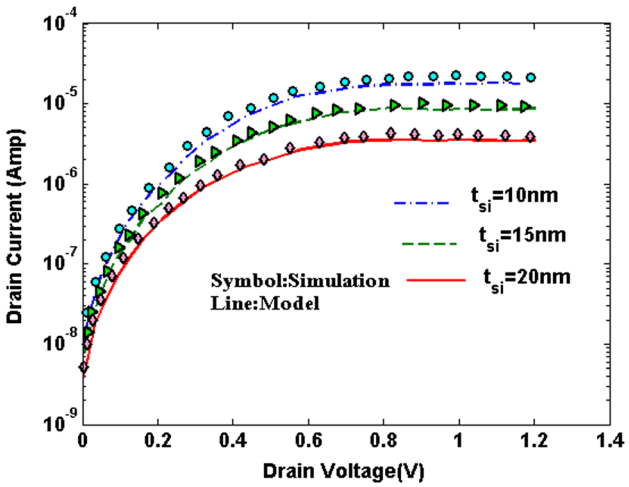

Fig. 8 The I_d–V_{DS} characteristics for different silicon thicknesses of t_{Si} = 15 nm and 20 nm with V_{GS} = 1 V

along with the OFF current in the GAA-HJTFET. Figure 6 shows the resulting drain current variation as a function of the gate voltage for different t_{Si} values, revealing an increase in the drain current I_d with a decrease in t_{Si} due to the significant band-to-band tunneling of electrons from the valance to conduction band of the channel; the decrease in the drain current with an increase in t_{Si} reduces the shortest tunneling path length L_{min}.

The variation of the drain current I_d as a function of the drain-to-source voltage V_{DS} is shown in Fig. 7 for different V_{GS} values, clearly indicating that an increase in the gate voltage will increase the drain current I_d as a result of the decreasing barrier height, which further increases the movement of added electrons from the source to channel.

Figure 8 shows the resulting variation of the drain current as a function of the drain-to-source voltage V_{DS} for different channel thicknesses. An increase in t_{Si} decreases the drain current I_d due to the reduced tunneling volume. Figure 9 shows the transconductance plot for different channel thicknesses with V_{GS} = 1 V and L = 50 nm. The peak value at the drain junction can be attributed to the increase in the shortest tunneling path L_{min}. Figure 10 shows a comparison of the drain current, the transconductance, and the first derivative of the transconductance with L = 50 nm, V_{DS} = 1 V, and t_{Si} = 15 nm. The dependence of the current on the gate bias changes from quasi-exponential to linear with an increase in the gate bias. It is observed that the peak is high for the first derivative of

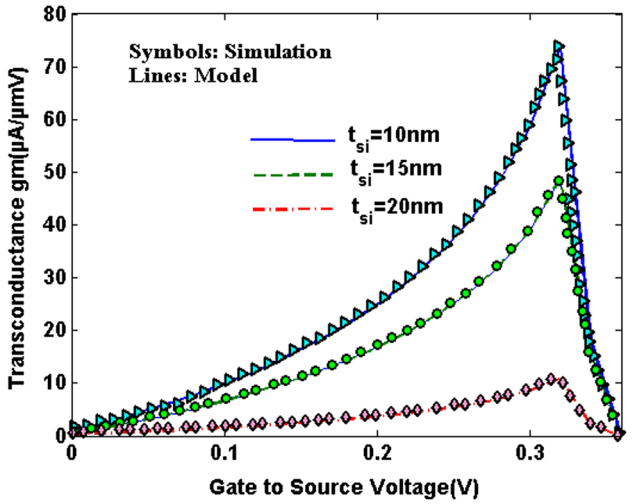

Fig. 9 The g_m–V_{GS} plots for different channel thicknesses t_{Si} of 10 nm, 15 nm, and 20 nm

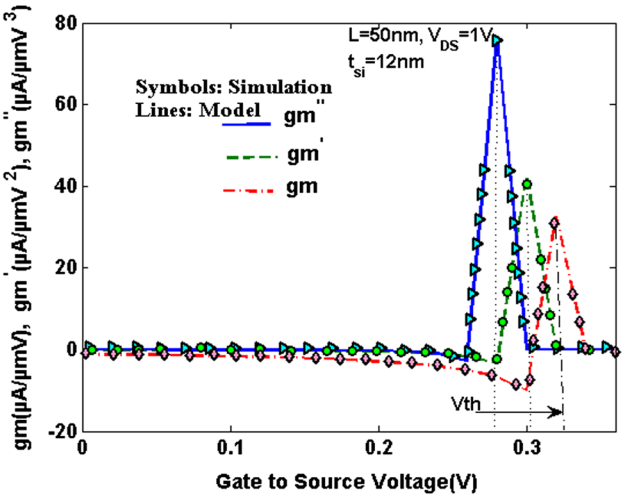

Fig. 11 The extraction of the threshold voltage V_{th}

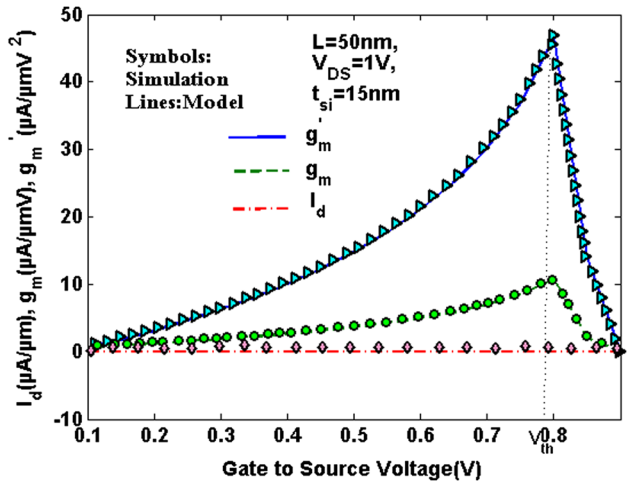

Fig. 10 A comparison of the plots of I_d, g_m, and g_m' with $L=50$ nm

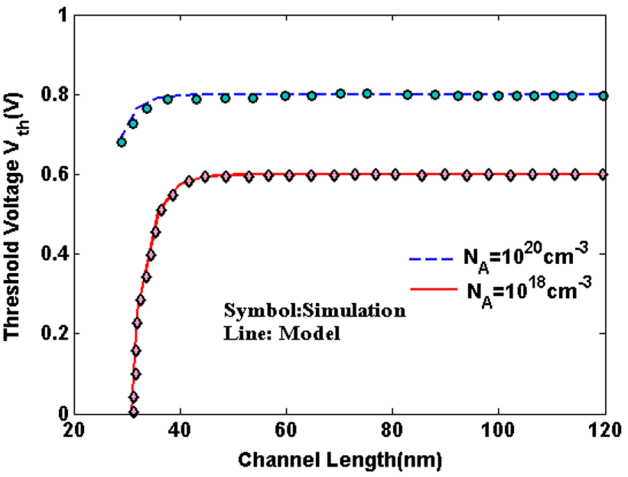

Fig. 12 The threshold voltage along the channel for $V_{DS}=0.5$ V and $V_{GS}=0.8$ V

the transconductance due to the decrease in the tunneling volume, which indicates the threshold voltage. Figure 11 demonstrates the extraction of the threshold voltage, where the peak transition at the drain–channel junction is due to the quasiexponential and linear dependence of the drain current I_d with the gate voltage V_{GS}. When using the second derivative method for extraction of the threshold voltage, the device in the linear region is sensitive to measurement error and noise. Figure 12 shows the threshold voltage plot along the channel length using the minimum channel potential method, revealing that the threshold voltage increases linearly from the source to channel region until it saturates due to the maximum electric field at the junction. The threshold voltage remains constant along the channel region due to the independence from the gate length for positive voltage. The threshold voltage shift is high for high doping concentration. Figures 11 and 12 show that the threshold voltage obtained by the second derivative method is low compared with that extracted using the minimum channel potential method.

Figure 13 shows the subthreshold swing for different oxide thicknesses; for the proposed device, it is limited to 48 mV/dec, which is less than for a MOSFET device. This

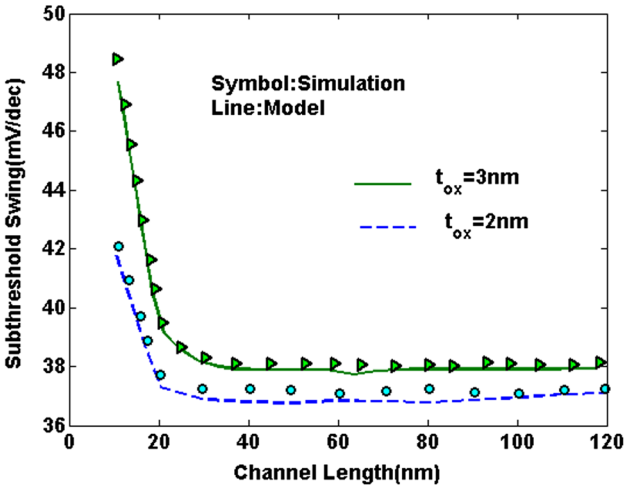

Fig. 13 The subthreshold swing across the channel length for different oxide thicknesses

plot reveals that the subthreshold swing is constant across the channel length, thus decreasing the DIBT in this device.

5 Conclusions

A 2-D analytical model for the surface potential, electric field, drain current, transconductance, and threshold voltage of a GAA-HJTFET is developed, including the source–channel, channel, and drain–channel depletion regions. The lateral electric field corresponding to the channel depletion is used to calculate the BTBT generation rate analytically and thus extract the drain current. Based on the drain current, the transconductance and threshold voltage are derived, then the threshold voltage is obtained using the quasiexponential and linear dependence of the drain current I_d on the gate voltage V_{GS}. The proposed model predicts the characteristics of the GAA-HJTFET for different parameter values to provide insight into the device physics. Validation of the results against simulations reveals good agreement.

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