



# A simulation study of the influence of a high- $k$ insulator and source stack on the performance of a double-gate tunnel FET

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## Abstract

The influence of incorporating  $\text{HfO}_2$  as a dielectric at the drain side and a silicon stack at the source side on the electrical performance of a double-gate tunnel field-effect transistor (TFET) is investigated by comparing a conventional TFET structure with four other structures in which the gate dielectric material is either homogeneous or heterogeneous while the insulator on the drain side is either  $\text{SiO}_2$  or  $\text{HfO}_2$ . Moreover, a structure with a silicon source stack is proposed and the figures of merit of the resulting device are compared with other counterparts. The results of the simulations reveal that the presence of an  $\text{HfO}_2$  insulator on the drain side reduces the ambipolar conduction while the heterogeneous gate dielectric enhances the drive current and transconductance. However, the use of  $\text{HfO}_2$  slightly deteriorates the source–gate and drain–gate capacitances in comparison with the conventional TFET. Furthermore, the incorporation of a silicon source stack along with a heterogeneous gate dielectric and  $\text{HfO}_2$  insulator on the drain side leads to a higher  $I_{\text{ON}}/I_{\text{OFF}}$  ratio, lower subthreshold slope ( $S$ ), and lower ambipolar conduction in the studied TFET with channel length of 50 nm.

**Keywords** Double-gate TFET · Heterogeneous gate dielectric · Ambipolar conduction · Drive current · Parasitic capacitance

## 1 Introduction

The ongoing downscaling of semiconductor devices and the requirement to reduce the power consumption density of integrated circuits (ICs) have led to the proposition of many innovative technologies for “More Moore” and “More than Moore” electronics applications [1, 2]. Because of their low power dissipation, TFETs have thus attracted much attention recently and even become serious candidates for use in ultralow-power applications [3, 4]. The carrier injection mechanism in TFETs is based on band to band tunneling (BTBT), resulting in their low energy dissipation and the expectation of a significant reduction in the off-state current in such devices [5, 6]. Furthermore, the subthreshold

slope of TFETs can be reduced below 60 mV/dec, which has been proved to be the theoretical limit for conventional metal–oxide–semiconductor field-effect transistors (MOSFETs) [7, 8]. Therefore, TFETs are very energy efficient and can be incorporated into circuits for operation at very low supply voltage targets [9–12]. However, TFET devices also suffer from low on-state current ( $I_{\text{ON}}$ ) and ambipolar current conduction ( $I_{\text{amb}}$ ) when used in circuits [12–14]. The low  $I_{\text{ON}}$  of TFETs is due to the BTBT carrier injection mechanism itself, according to which electrons tunnel from the valence band of the source region to the conduction band of the channel region, or from the valence band of the channel region to the conduction band of the drain region, with the band bending in the energy gap being controlled by the gate bias [15, 16]. The ambipolar conduction in TFETs occurs due to the large BTBT at the source–channel junction as well as the drain–channel junction at different polarities of the gate voltage applied to obtain the drive current. This can prevent the device from turning off completely. As a result, a TFET can show  $n$ -type behavior with electrons as the majority carriers as well as  $p$ -type behavior with holes as the majority carriers at the same drain voltage [15, 16].

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Many ideas have been proposed in literature to boost the drive current of TFETs, including approaches based on the insertion of source pocket (SP) doping [17–19], tunneling-area engineering using high- $k$  dielectrics [6, 20, 21], double-gate (DG) architectures [22], gate-to-source overlap [23], gate-to-drain underlap [24], dual-material gates [25], and the use of strained silicon [26]. Meanwhile, the problem of ambipolar conduction can be addressed by adopting various techniques such as a gate–drain underlap [23, 27], Gaussian or nonuniform drain doping [6, 28], work-function engineering of the gate electrodes [29], and spacer and gate material engineering [30, 31].

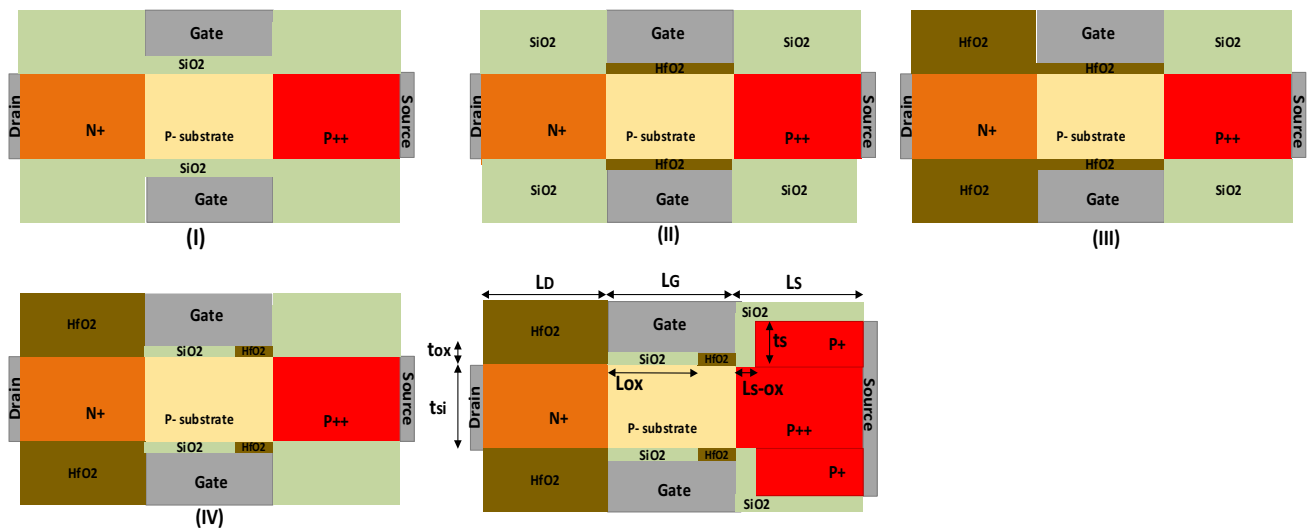
Several supplementary structures are analyzed stepwise herein to study how the use of a heterogeneous gate dielectric, an  $\text{HfO}_2$  insulator on the drain side of the gate, and a silicon source stack on the source side can both enhance the drive current and reduce the ambipolar current conduction in comparison with the conventional DG-TFET. Furthermore, the transconductance ( $g_m$ ), gate–drain capacitance ( $C_{gd}$ ), gate–source capacitance ( $C_{gs}$ ), subthreshold slope ( $S$ ), and  $I_{ON}/I_{OFF}$  ratio are also analyzed for the studied structures with a fixed channel length of 50 nm.

The remainder of this manuscript is organized as follows: In Sect. II, the proposed device structures and simulation models are discussed. Section III addresses the electrical characteristics of the devices under study. Finally, the principal findings and conclusions of this paper are presented in Sect. IV.

## 2 The device structures and simulation parameters

Figure 1 shows a schematic cross-sectional view of the five devices under study. Structure (I) is a conventional DG-TFET with a  $\text{SiO}_2$  gate dielectric. Structure (II) is similar to the conventional DG-TFET but with an  $\text{HfO}_2$  gate dielectric. In structure (III), both the gate dielectric and the drain-side insulator are made of  $\text{HfO}_2$ . In structure (IV), a heterogeneous gate dielectric and an  $\text{HfO}_2$  insulator are applied on the drain side of the gate, while in structure V, a silicon source stack is added to structure (IV). The simulation results are evaluated in comparison with the conventional TFET with structure (I), and the other structures are studied in a stepwise fashion to reveal the effect of applying each modification to the structure on their electrical performance. All the simulation parameters related to the studied structures are presented in Table 1.

All the simulations are carried out using the SILVACO ATLAS version 5.22.1.R technology computer-aided design (TCAD) simulator, applying the nonlocal band-to-band tunneling (BTBT) model to compute the tunneling current in the lateral direction. The bandgap narrowing (BGN) model is utilized to account for the highly doped regions in the devices. The Shockley–Read–Hall (SRH) and Auger models are used to consider the generation/recombination in the simulations. Furthermore, the drift–diffusion carrier transport model and Fermi–Dirac distribution function model are used in the simulations. Tunneling through the gate oxide is ignored, as in Refs. [32–35]. Since the silicon film thickness



**Fig. 1** A schematic representation of the studied double-gate TFETs: (I) the conventional DG-TFET, (II) the conventional DG-TFET with an  $\text{HfO}_2$  gate dielectric, (III) the DG-TFET with an  $\text{HfO}_2$  dielectric on the gate and drain sides, (IV) the DG-TFET with a heterogeneous

gate dielectric and an  $\text{HfO}_2$  insulator on the drain side, and (V) the DG-TFET with a heterogeneous gate dielectric, an  $\text{HfO}_2$  insulator on the drain side, and a silicon stack on the source side

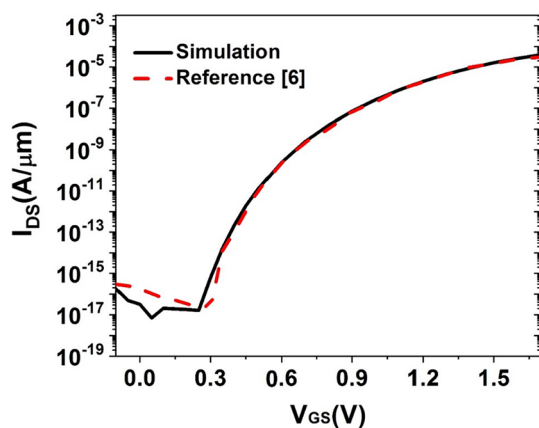
**Table 1** The parameter values for the structures under study

Parameter	Value
Oxide thickness ( $t_{ox}$ )	1 nm
Silicon channel thickness ( $t_{Si}$ )	10 nm
Channel length ( $L_G$ )	50 nm
SiO <sub>2</sub> length in the gate ( $L_{OX}$ )	45 nm
Source/drain extended length ( $L_S/L_D$ )	100 nm
Source stack oxide length ( $L_{S-ox}$ )	4 nm
Stack thickness ( $t_S$ )	7 nm
Gate work function	4.3 eV
HfO <sub>2</sub> permittivity	22 [37]
Channel doping ( $P$ )	$1 \times 10^{17} \text{ cm}^{-3}$
Source doping ( $p^{++}$ )	$1 \times 10^{20} \text{ cm}^{-3}$
Drain doping ( $N^+$ )	$5 \times 10^{18} \text{ cm}^{-3}$
Source stack doping ( $p^+$ )	$5 \times 10^{19} \text{ cm}^{-3}$

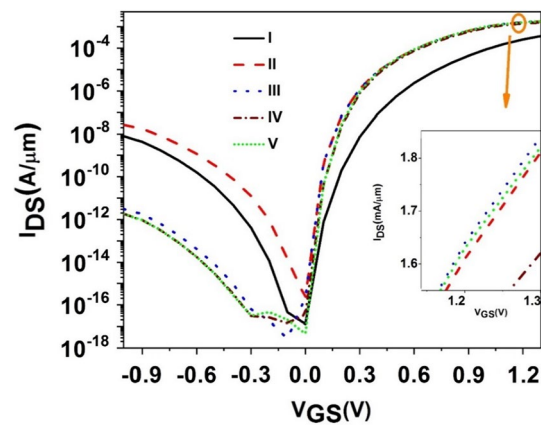
is 10 nm, quantum confinement effects arising due to the thin silicon-on-insulator (SOI) body are not considered [36]. The simulation setup is calibrated against the work of Boucart [6], shown in Fig. 2, by considering electron and hole tunneling masses of  $m_e = 0.07m_0$  and  $m_h = 0.71m_0$ , respectively. The primary objective of this work is to consider the combined relative effects of a heterogeneous gate dielectric, an HfO<sub>2</sub> insulator on the drain side of the gate and a source stack on the drive current and ambipolar current with respect to the conventional structure by studying the qualitative trends.

### 3 Results and Discussion

Figure 3 depicts the transfer characteristics of the five TFETs at  $V_{DS} = 1.0 \text{ V}$ . It is observed from this figure that the conventional TFET (I) as well as structure TFET (II) exhibit



**Fig. 2** The calibration of the simulation results against those presented in Ref. [6] at  $V_{DS} = 1.0 \text{ V}$

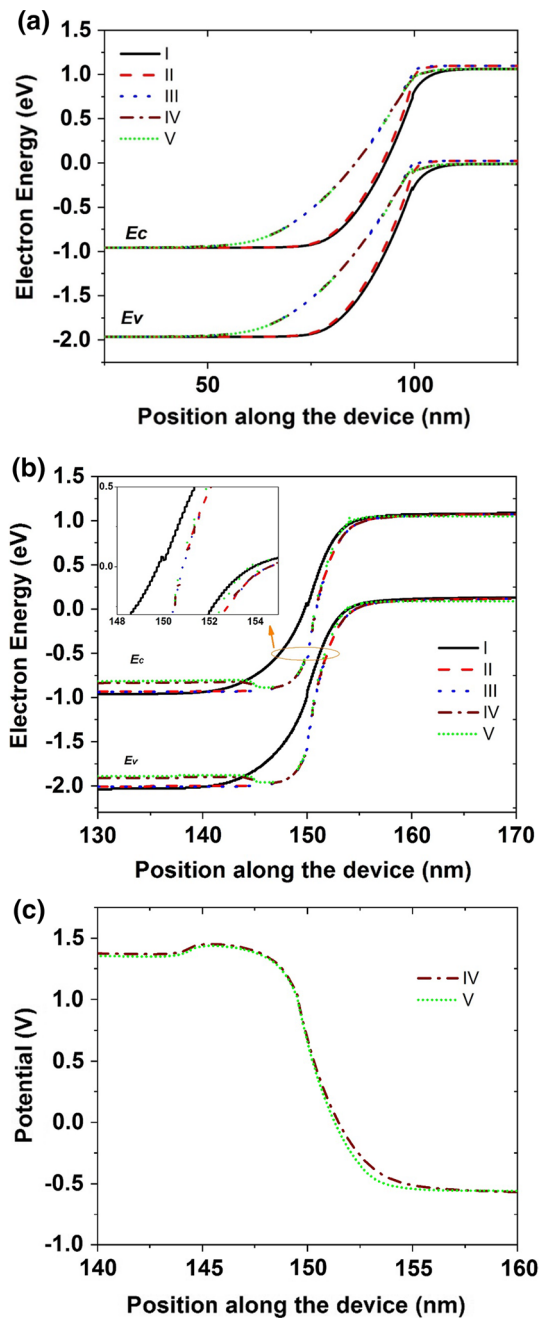


**Fig. 3** The transfer characteristics ( $I_D$ - $V_{GS}$ ) of the five TFETs under study at  $V_{DS} = 1 \text{ V}$

higher ambipolar conduction compared with the other TFETs in this figure at negative gate voltages. At positive gate voltages, it can be seen that TFETs (II), (III), and (V) show the highest drive currents. The behavior of the transfer characteristics of the devices under study can be explained based on their energy band diagram profiles obtained at a cut line placed at 1 nm below the Si-oxide interface, through the silicon active region of the devices, as shown in Fig. 4a, b. According to the Wentzel–Kramers–Brillouin (WKB) approximation, the tunneling probability,  $T(E)$ , is calculated as [37]:

$$T(E) = \exp \left[ -2 \int_{x_{start}}^{x_{end}} K(x) dx \right], \tag{1}$$

where  $K$  is the evanescent wavevector and  $x_{start}$  and  $x_{end}$  indicate the start and end points of the tunneling path. Ideally, the start and end points of the tunneling path should be considered in the flat-band (neutral) regions at either side of the junction, where their influence can be calibrated using the carrier effective mass. Then, the calculated tunneling probability for each energy level can be used to calculate the current density [37]. For a thinner tunneling width, the tunneling probability increases [38]. Based on the above theorem and Fig. 4a, it is observed that TFETs (I) and (II) show greater band bending, thus the tunneling width is shorter in their profiles. Therefore, the ambipolar conduction is greater in these devices compared with TFETs (III), (IV), and (V). According to the results shown in this figure, incorporating the HfO<sub>2</sub> insulator on the drain side of the gate causes the conduction band (or valence band) slope to decrease. This slope is proportional to the electric field intensity, so this leads to reduced band bending and ambipolar conduction in the devices with an HfO<sub>2</sub> insulator on the drain side. On



**Fig. 4** The energy band diagrams of the five TFETs at **a**  $V_{GS} = -1$  V and **b**  $V_{GS} = 1.3$  V; **c** the potential profiles of structures (IV) and (V) at  $V_{GS} = 1.3$  V. For all cases, the drain bias is  $V_{DS} = 1$  V

the other hand, Fig. 4b shows that the energy band diagrams of all the TFETs except TFET (I) exhibits an overlap in the tunneling region, so it is expected that they will exhibit the same order of drive current.

Based on Figs. 3 and 4, the role of utilizing  $\text{HfO}_2$  above the drain side or underneath the gate, a heterogeneous dielectric, and a source stack in the structures can be explained. The results show that the presence of  $\text{HfO}_2$  dielectric in the

whole gate region of TFETs (II) and (III) enables the electrostatic control over the channel by the gate to be strongly increased and thus the drive current to be enhanced, while embedding  $\text{HfO}_2$  above the drain in TFET (III) leads to a reduction of the ambipolar conduction in this device by about four orders of magnitude compared with the similar structure in TFET (II). As mentioned above, this improvement is due to the formation of a greater tunneling width (Fig. 4a) in the drain–channel junction of TFET (III) compared with TFET (II) due to the incorporation of  $\text{HfO}_2$  above the drain side. The structural difference between TFETs (III) and (IV) is the embedding of a heterogeneous dielectric in TFET (IV), whose role is revealed by the difference between their  $I_D$ – $V_G$  characteristics. As is obvious from Fig. 3, embedding the heterogeneous dielectric reduces both the drive and ambipolar currents. In fact, utilizing  $\text{HfO}_2$  on the source side of the gate oxide reduces the tunneling width by increase in the band bending in the channel–source junction, which in turn leads to an enhancement of the drive current. However, the use of a low- $k$  dielectric ( $\text{SiO}_2$ ) on the drain side of the gate insulator increases the tunneling width in the channel–drain junction, which reduces the ambipolar conduction in comparison with the conventional structure. The structure of TFET (V) is similar to TFET (IV) but with an additional source stack on the source side. The results shown in Fig. 4b reveal that such incorporation of a silicon source stack reduces the effective tunneling width in the source–channel junction of TFET (V). In fact, as shown by Fig. 4c, the introduction of a source stack leads to the formation of a sharper potential profile in the source–channel junction of structure (V) compared with (IV). This increases the electric field and reduces the tunneling width in the source–channel junction. Therefore, the drive current in TFET (V) is enhanced. It is also obvious that the ambipolar current is comparable to TFET (IV) and the source stack has no effect on it.

The amplification can be used as a figure of merit for analog devices, being proportional to the transconductance  $g_m$ , which is defined as  $g_m = dI_D/dV_{GS}$  [39]. A higher  $g_m$  in a device indicates that the gate has better control over the variation of the device current. Figure 5 shows that this parameter is comparable for TFETs (II), (III), and (V) and much higher than for the conventional TFET (I). Indeed, these improvements are due to the incorporation of the heterogeneous gate dielectric, the  $\text{HfO}_2$  insulator on the drain side, and the source stack in the mentioned TFET structures. This is due to the fact that these modifications enhance the gate control over the channel, as explained above.

The effect of incorporating a high- $k$  material (such as  $\text{HfO}_2$ ) on the drain side on two important capacitances, viz. the gate–drain ( $C_{gd}$ ) and gate–source ( $C_{gs}$ ) components, is now investigated, since it may deteriorate these parasitic capacitances [19]. Figure 6 shows that  $C_{gd}$  increases

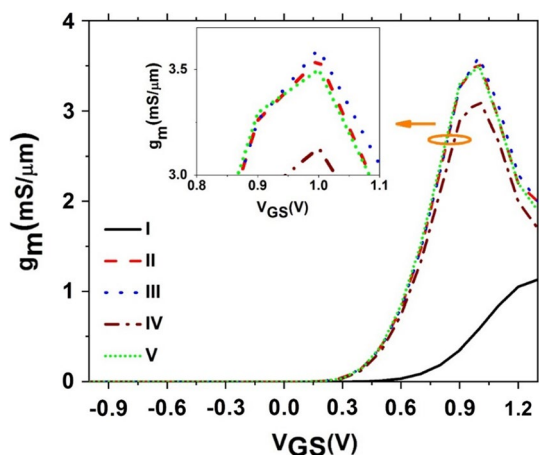


Fig. 5 The transconductance of the different TFETs under study at  $V_{DS}=1\text{ V}$

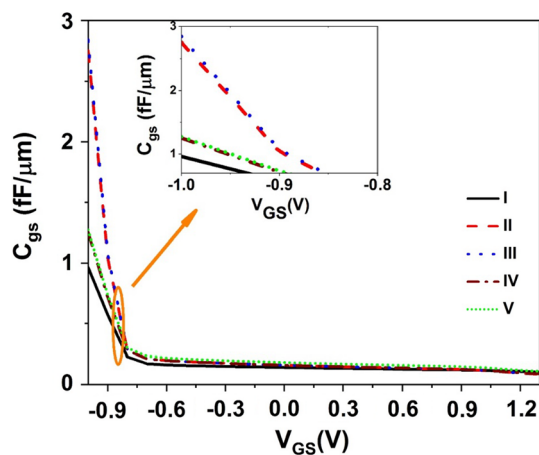


Fig. 7 The gate–source capacitance versus the gate voltage for the different TFETs at  $V_{DS}=1\text{ V}$  and a frequency of 1 MHz

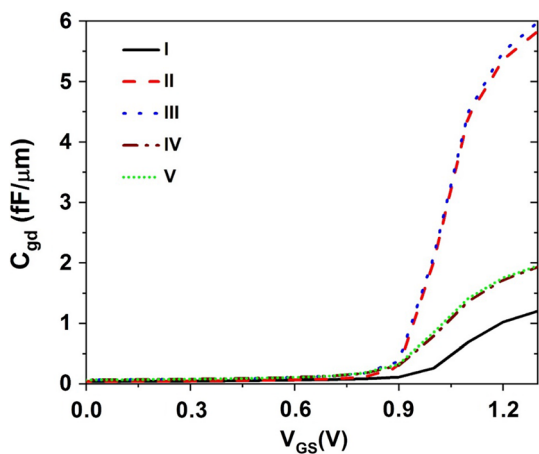


Fig. 6 The gate–drain capacitance versus the gate voltage for the different TFETs at  $V_{DS}=1\text{ V}$  and a frequency of 1 MHz

with increasing  $V_{GS}$  for all the devices. This is due to the enhanced coupling between the gate and drain charges at higher gate voltages. It is observed from this figure that TFETs (II) and (III) show the highest parasitic components, while for TFETs (IV) and (V), these parasitic components are more comparable to those of the conventional TFET (I). The latter effect is due to the fact that they have a heterogeneous gate dielectric with lower permittivity ( $\epsilon_{SiO_2}=3.9$ ) on the drain side of their structure, which reduces the coupling between the two terminals. Figure 7 shows that  $C_{gs}$  decreases with increasing  $V_{GS}$  for all the devices. This occurs due to the reduced coupling between the gate and source terminals at higher gate voltages, as indicated in Ref. [19]. Since the gate dielectric in TFETs (II) and (III) is uniform  $HfO_2$ , the parasitic capacitance  $C_{gs}$  is highest for these devices in comparison with all the other devices. In addition, the  $C_{gs}$  of TFETs (IV) and (V) is closer to that of the conventional

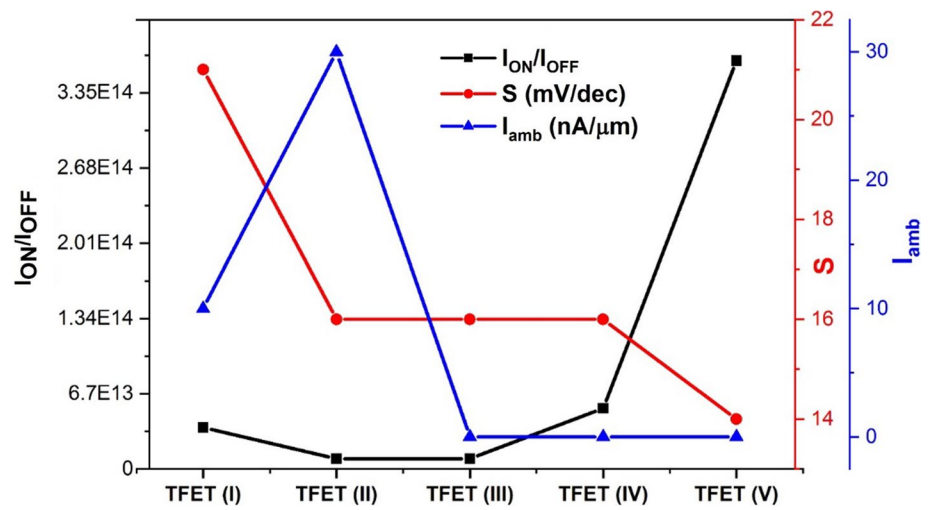
TFET (I). This result emphasizes the fact that the heterogeneous gate dielectric can cause this parasitic capacitance to become comparable to that in the conventional counterpart. The results shown in Figs. 6 and 7 also reveal that the source stack has no significant effect on the parasitic components  $C_{gd}$  and  $C_{gs}$ .

Figure 8 illustrates the  $I_{ON}/I_{OFF}$  ratio, the subthreshold slope ( $S$ ), and the ambipolar conduction ( $I_{amb}$ ) for the five DG-TFETs under study. It is observed that the incorporation of a heterogeneous gate dielectric ( $SiO_2$  and  $HfO_2$ ) along with the source stack can enhance the  $I_{ON}/I_{OFF}$  ratio and decrease the  $S$  parameter. It can also be seen that, for the devices with the  $HfO_2$  insulator on the drain side,  $I_{amb}$  is reduced; these results show that TFET (V) offers the best performance in terms of the mentioned parameters due to its supplementary specific structure compared with its counterparts.

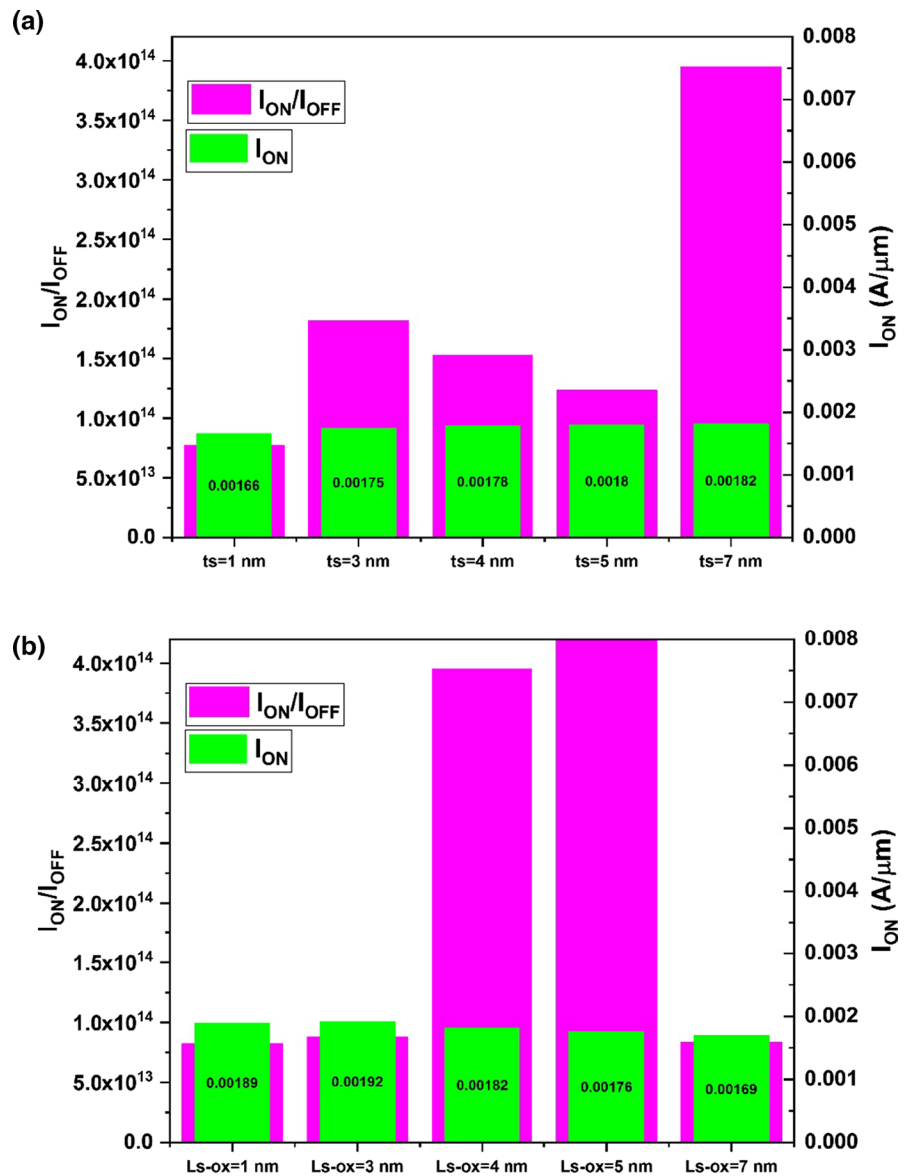
The influence of the source stack parameters ( $t_s$  and  $L_{s-ox}$ ) and its doping value on the performance of TFET (V) is noteworthy. As depicted in Fig. 9, there is a nonlinear relation between the device current and the source stack thickness ( $t_s$ ) or stack oxide length ( $L_{s-ox}$ ). Based on the results shown in this figure,  $I_{ON}$  and the  $I_{ON}/I_{OFF}$  current ratio will be close to optimum at  $t_s=7\text{ nm}$  and  $L_{s-ox}=4\text{ nm}$ , compared with other source stack thicknesses and stack oxide lengths. It is also clear from Fig. 10 that, when the silicon source stack doping value is set to  $5 \times 10^{19}\text{ cm}^{-3}$ , the  $I_{ON}/I_{OFF}$  current ratio becomes one order of magnitude higher than for the other two doping values. Moreover, the subthreshold swing ( $S$ ) parameter for the selected doping of  $5 \times 10^{19}\text{ cm}^{-3}$  is slightly lower (14 mV/dec) compared with the other cases. The  $S$  parameter for the source stack doping values of  $1 \times 10^{19}$  and  $1 \times 10^{20}\text{ cm}^{-3}$  is equal to 16 and 17 mV/dec, respectively. As a result,  $5 \times 10^{19}\text{ cm}^{-3}$  is chosen as the optimum source stack doping value.

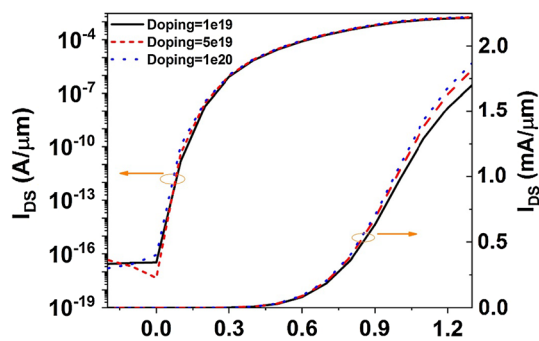


**Fig. 8** The  $I_{ON}/I_{OFF}$  ratio (black), subthreshold slope (red), and ambipolar drain current (blue) for the five devices under study.  $I_{OFF}$  is measured at a bias of  $V_{DS}=1$  V and  $V_{GS}=0$  V, while the ambipolar conduction ( $I_{amb}$ ) is measured at a bias of  $V_{DS}=1$  V and  $V_{GS}=-1$  V (Color figure online)



**Fig. 9** The  $I_{ON}/I_{OFF}$  current ratio along with the  $I_{ON}$  value obtained for structure (V) when varying **a** the stack thickness,  $t_s$  and **b** the source stack oxide length,  $L_{s-ox}$ . The measurements are all taken at a bias of  $V_{DS}=1$  V and  $V_{GS}=1.3$  V





**Fig. 10** The transfer characteristics of structure (V) obtained for different source stack doping values at  $V_{DS} = 1$  V

## 4 Conclusions

The effects of incorporating a heterogeneous gate dielectric, a  $\text{HfO}_2$  insulator on the drain side of the gate, and a silicon source stack on the electrical characteristics of a double-gate TFET are studied. The results reveal that the incorporation of a heterogeneous gate dielectric along with the  $\text{HfO}_2$  insulator on the drain side can reduce the ambipolar conduction while retaining low gate–drain and gate–source parasitic capacitances with respect to the conventional double-gate TFET, by forming strong barriers in the drain–channel and channel–source junctions. Embedding the silicon source stack can further enhance the drive current along with the  $I_{ON}/I_{OFF}$  ratio and reduce the  $S$  parameter, while having no strong effect on the mentioned parasitic capacitances. Thus, it seems that TFET (V) exhibits promising electrical behavior for use in low-power applications.

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## References

- Bai, P., Auth, C., Balakrishnan, S., Bost, M., Brain, R., Chikarmane, V., Heussner, R., Hussein, M., Hwang, J., Ingerly, D., James, R., Jeong, J., Kenyon, C., Lee, E., Lee, S.-H., Lindert, N., Liu, M., Ma, Z., Marieb, T., Murthy, A., Nagisetty, R., Natarajan, S., Neirynek, J., Ott, A., Parker, C., Sebastian, J., Shaheed, R., Sivakumar, S., Steigerwald, J., Tyagi, S.: A 65 nm logic technology featuring 35 nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and  $0.57 \mu\text{m}^2$  SRAM cell. *IEEE International Electron Devices Meeting*, pp. 657–660 (2004)
- International Technology Roadmap for Semiconductors 2.0. US (2015).
- Jain, P., Prabhat, V., Ghosh, B.: Dual metal-double gate tunnel field effect transistor with mono/hetero dielectric gate material. *J. Comput. Electron.* **14**, 537–542 (2015)
- Choi, W.Y., Lee, H.K.: Demonstration of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs). *Nano Conv.* **3**, 13 (2016)
- Kyung, C.-M.: *Nano Devices and Circuit Techniques for Low-Energy Applications and Energy Harvesting*. Springer, Berlin (2015)
- Boucart, K., Ionescu, A.M.: Double-gate tunnel FET with high-K/metal gate dielectric. *IEEE Trans. Electron Devices* **54**, 1725–1733 (2007)
- Sarkar, D., Xie, X., Liu, W., Cao, W., Kang, J., Gong, Y., et al.: A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* **526**, 91 (2015)
- Tura, A., Woo, J.C.: Performance comparison of silicon steep subthreshold FETs. *IEEE Trans. Electron Devices* **57**, 1362–1368 (2010)
- Morris, D.H., Avci, U.E., Rios, R., Young, I.A.: Design of low voltage tunneling-FET logic circuits considering asymmetric conduction characteristics. *IEEE J. Emerging Sel. Top. Circ. Syst.* **4**, 380–388 (2014)
- Avci, U.E., Morris, D.H., Young, I.A.: Tunnel field-effect transistors: Prospects and challenges. *IEEE J. Electron Devices Soc.* **3**, 88–95 (2015)
- Ionescu, A.M., Riel, H.: Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **479**, 329 (2011)
- Ram, M.S., Abdi, D.B.: Dopingless PNP tunnel FET with high performance: design and analysis. *Superlattices Microstruct.* **82**, 430–437 (2015)
- Dagtekin, N., Ionescu, A.M.: Impact of super-linear onset, off-region due to uni-directional conductance and dominant Cgd on performance of TFET-based circuits. *IEEE J. Electron Devices Soc.* **3**, 233–239 (2014)
- Madan, J., Chaujar, R.: Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability. *IEEE Trans. Device Mater. Reliab.* **16**, 227–234 (2016)
- Garg, S., Saurabh, S.: Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis. *Superlattices Microstruct.* **113**, 261–270 (2018)
- Saurabh, S., Kumar, M.J.: *Fundamentals of tunnel field-effect transistors*. CRC Press, Boca Raton (2016)
- Chang, H.-Y., Adams, B., Chien, P.-Y., Li, J., Woo, J.C.: Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing. *IEEE Trans. Electron Devices* **60**, 92–96 (2012)
- Abdi, D.B., Kumar, M.J.: In-built N+ pocket pnpn tunnel field-effect transistor. *IEEE Electron Device Lett.* **35**, 1170–1172 (2014)
- Yadav, D.S., Sharma, D., Raad, B.R., Bajaj, V.: Dual workfunction hetero gate dielectric tunnel field-effect transistor performance analysis. *Int. Conf. Adv. Commun. Concr. Comput. Tech (ICAC CCT)*, pp. 26–29 (2016).
- Li, M.O., Esseni, D., Nahas, J.J., Jena, D., Xing, H.G.: Two-dimensional heterojunction interlayer tunneling field effect transistors (thin-TFETs). *IEEE J. Electron Devices Soc.* **3**, 200–207 (2015)
- Sant, S., Schenk, A.: Methods to enhance the performance of InGaAs/InP heterojunction tunnel FETs. *IEEE Trans. Electron Devices* **63**, 2169–2175 (2015)
- Agarwal, S., Klimeck, G., Luisier, M.: Leakage-reduction design concepts for low-power vertical tunneling field-effect transistors. *IEEE Electron Device Lett.* **31**, 621–623 (2010)
- Verhulst, A.S., Vandenberghe, W.G., Maex, K., Groeseneken, G.: Tunnel field-effect transistor without gate-drain overlap. *Appl. Phys. Lett.* **91**, 053102 (2007)
- Chattopadhyay, A., Mallik, A.: Impact of a spacer dielectric and a gate overlap/underlap on the device performance of a tunnel

- field-effect transistor. *IEEE Trans. Electron Devices* **58**, 677–683 (2011)
25. Saurabh, S., Kumar, M.J.: Novel attributes of a dual material gate nanoscale tunnel field-effect transistor. *IEEE Trans. Electron Devices* **58**, 404–410 (2010)
  26. Saurabh, S., Kumar, M.J.: Impact of strain on drain current and threshold voltage of nanoscale double gate tunnel field effect transistor: Theoretical investigation and analysis. *Jpn. J. Appl. Phys.* **48**, 064503 (2009)
  27. Madan, J., Chaujar, R.: Gate drain underlapped-PNIN-GAA-TFET for comprehensively upgraded analog/RF performance. *Superlattices Microstruct.* **102**, 17–26 (2017)
  28. Vijayvargiya, V., Vishvakarma, S.K.: Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance. *IEEE Trans. Nanotechnol.* **13**, 974–981 (2014)
  29. Raad, B.R., Nigam, K., Sharma, D., Kondekar, P.: Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement. *Superlattices Microstruct.* **94**, 138–146 (2016)
  30. Sahay, S., Kumar, M.J.: Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX. *IEEE Trans. Electron Devices* **62**, 3882–3886 (2015)
  31. Wu, J., Taur, Y.: Reduction of TFET OFF-current and subthreshold swing by lightly doped drain. *IEEE Trans. Electron Devices* **63**, 3342–3345 (2016)
  32. Raad, B.R., Tirkey, S., Sharma, D., Kondekar, P.: A new design approach of dopingless tunnel FET for enhancement of device characteristics. *IEEE Trans. Electron Devices* **64**, 1830–1836 (2017)
  33. Anghel, C., Gupta, A., Amara, A., Vladimirescu, A.: 30-nm tunnel FET with improved performance and reduced ambipolar current. *IEEE Trans. Electron Devices* **58**, 1649–1654 (2011)
  34. Boucart, K., Ionescu, A.M.: Length scaling of the double gate tunnel FET with a high-k gate dielectric. *Solid State Electron.* **51**, 1500–1507 (2007)
  35. Shaker, A., El Sabbagh, M., El-Banna, M.M.: Influence of drain doping engineering on the ambipolar conduction and high-frequency performance of TFETs. *IEEE Trans. Electron Devices* **64**, 3541–3547 (2017)
  36. Jain, A.K., Sahay, S., Kumar, M.J.: Controlling L-BTBT in emerging nanotube FETs using dual-material gate. *IEEE J. Electron Devices Soc.* **6**, 611–621 (2018)
  37. Atlas user's manual. Silvaco International Software, Santa Clara, CA, USA (2016).
  38. Mamidala, J.K., Vishnoi, R., Pandey, P.: Tunnel field-effect transistors (TFET): modelling and simulation. Wiley, Boca Raton (2016)
  39. Zareiee, M.: A new architecture of the dual gate transistor for the analog and digital applications. *AEU Int. J. Electron. Commun.* **100**(2), 114–118 (2019)

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