Journal of Computational Electronics (2020) 19:658–667
https://doi.org/10.1007/s10825-020-01484-8

Controlling the ambipolar current in ultrathin SOI tunnel FETs using the back-bias effect

Tripuresh Joshi[1] · **Balraj Singh**[1] · **Yashvir Singh**[1]

Published online: 31 March 2020

Abstract

A two-dimensional (2-D) technology computer-aided design (TCAD)-based simulation study of the back bias in the ultrathin silicon-on-insulator (SOI) tunnel field-effect transistor (TFET) is presented. The transfer characteristics of a conventional TFET called the back-bias TFET (BB-TFET) depend on the back bias and the oxide thickness below the TFET epitaxial layer. The back bias affects the electric field at the source/channel and drain/channel junctions, hence both the ON-state current (I_{ON}) and the ambipolar current (I_{AMB}) reduce with a negative back-bias voltage. This reduction in I_{ON} is not desirable in a TFET, hence a modified TFET structure called the back-bias underdrain TFET (BBUD-TFET) is proposed. In the BBUD-TFET, the back bias is applied on a *p*-Si pocket placed under the drain region, which is isolated using an ultrathin oxide. The back bias in the proposed BBUD-TFET mainly affects the electric field at the drain/channel interface, having a negligible impact on the source/channel interface. The BBUD-TFET structure is analyzed with SiO_2 or HfO_2 as the gate oxide. In the BBUD-TFET with HfO_2 as the gate oxide, the back bias completely suppresses the ambipolar current without reducing I_{ON}. Furthermore, the oxide thickness and back-bias voltage are optimized for the BBUD-TFET structure. In this study, 2-D TCAD simulations are carried out to investigate and analyze the performance of the BB-TFET and BBUD-TFET.

Keywords Tunnel field-effect transistor (TFET) · Silicon-on-insulator (SOI) · Back bias · Subthreshold swing

1 Introduction

Tunneling field-effect transistors (TFETs) are gaining importance due to their suppressed subthreshold swing (SS). However, these devices also suffer from low ON-state current (I_{ON}) and high leakage current due to ambipolar conduction, i.e., the conduction of current in the OFF-state (I_{OFF}) [1–3]. This ambipolar effect is undesirable for the performance of inverter-based logical circuits [4]. On the other hand, the low I_{ON} increases the charging and discharging time, hence decreasing the speed of circuits and making the TFET unsuitable to meet International Technology Roadmap for Semiconductors (ITRS) requirements [4, 5]. Therefore, increasing I_{ON} while suppressing the ambipolar current (I_{AMB}) are the main research challenges to make TFETs suitable for use in low-power circuit applications.

Several techniques have been reported in literature to suppress I_{AMB} in TFETs [5–14]. Hraziia et al. [5] utilized a gate–drain underlap region and a low-κ spacer in the gate–drain region, and placed the contact at the top and bottom of the structure to reduce the ambipolar effect in double-gate (DG)-TFETs. The proposed structure delivered $I_{AMB} \sim 10^{-14}$ A/μm with $I_{ON} \sim 10^{5}$ A/μm. Abdi and Kumar [6] proposed a gate-on-drain overlapping configuration in the DG-TFET to suppress I_{AMB}. The overlapped gate-on-drain configuration suppresses I_{AMB} ($\sim 10^{-15}$ A/μm) with I_{ON}/I_{OFF} of $\sim 10^{6}$. Raad et al. [7] reported a TFET structure with three gate materials in which the work function of the gate material on the source and drain sides was taken to be lower than the work function of the gate material in the middle. This device also employed a low-κ dielectric on the drain side and a high-κ dielectric on the source side. The reported TFET suppressed I_{AMB} to $\sim 10^{-16}$ A/μm while improving I_{ON} to $\sim 10^{4}$ A/μm. Narang et al. [8] used

✉ Balraj Singh
balraj.bits@gmail.com

Tripuresh Joshi
tripuresh.joshi@coolcog.in

Yashvir Singh
om_ysingh@yahoo.co.in

[1] Department of Electronics and Communication Engineering, G. B. Pant Institute of Engineering and Technology, Pauri 246194, Uttarakhand, India

a heterogeneous gate oxide with a gate–drain underlap configuration to minimize the I_{AMB} (~ 10^{-12} A/μm) of the device. Similarly, gate material engineering has been used to reduce the I_{AMB} of DG-TFETs by Nigam et al. [9]. They took a low-work-function gate material at the source and drain sides and a high-work-function gate material in the middle. This DG-TFET structure has been demonstrated to achieve a SS, I_{OFF}, and I_{ON}/I_{OFF} of 19 mV/dec, 2.29×10^{-17} A/μm, and 7.22×10^{11}, respectively. Sharkar et al. [10] presented a drain engineering approach to lower the I_{AMB} of the SOI TFET. Those authors established that the relative increase in thickness of the low-doping drain region over the high-doping drain region increased the tunneling width, leading to an appreciable reduction in I_{AMB} (~ 10^{-15} A/μm). Singh and Kondekar [11] proposed an electrostatically doped ferroelectric Schottky barrier TFET (ED-FE-SB TFET) by analyzing the effect of negative capacitance. The proposed device showed SS, I_{AMB}, and I_{ON}/I_{OFF} of 56 mV/dec, 8.74×10^{-9} A/μm, and 6.74×10^{7}, respectively. Rahimian and Fathipour [12] demonstrated an asymmetric junctionless nanowire (AJN) TFET having an n^{+} pocket at the source. The AJN TFET provided SS, I_{AMB}, and I_{ON}/I_{OFF} of 38 mV/dec, 7.5×10^{-12} A/μm, and 3.87×10^{9}, respectively. Ashita et al. [13] reported an electron–hole bilayer (EHB) TFET with double dielectric pockets in the source and drain. The proposed structure achieved an SS, I_{OFF}, and I_{ON}/I_{OFF} of 17.75 mV/dec, 9.09×10^{-17} A/μm, and 2.55×10^{9}, respectively. Further, Bal et al. [14] proposed a dual-material gate (DMG) TFET and studied its energy band modulation profile. The DMG TFET provided SS, I_{OFF}, and I_{ON}/I_{OFF} of 17 mV/dec, 3×10^{-13} A/μm, and 6.67×10^{9}, respectively.

The effect of back biasing on the performance of TFETs has also been studied in literature [15–18]. Guo et al. [15] improved the I_{ON}/I_{OFF} ratio and SS of the SOI TFET through back biasing, including the effect of variation in the source and drain doping underneath the gate electrode. A similar study was reported on the germanium-on-insulator (GOI) TFET by Matheu et al. [16]. Sahay and Kumar [17] proposed the inclusion of a heterodielectric box (HDB) over a heavily doped grounded substrate at the channel/drain interface with SiO_2 under the source/channel interface and a high-κ (HfO_2) dielectric under the drain region. Those authors reduced I_{AMB} to ~ 10^{-16} A/μm due to the increased tunneling width at the drain/channel interface and improved the I_{ON}/I_{OFF} ratio to ~ 10^{10}. Further, Wang et al. [18] presented an ultrathin-body GeSn TFET with a back gate bias to improve the I_{ON}, SS, and I_{AMB}.

Note that the techniques applied to suppress I_{AMB} in the cited articles also degrade the I_{ON} of the TFET, resulting in a low I_{ON}/I_{OFF} ratio. Therefore, it is desirable to design a TFET structure that can provide a lower I_{AMB} but higher I_{ON} simultaneously. In this work, the conventional TFET with a back bias applied on the p-Si layer over the buried oxide (BOX) and under the device is called the BB-TFET. In the BB-TFET structure, I_{AMB} is completely suppressed and the SS is improved. However, I_{ON} is also reduced in the BB-TFET structure. To overcome this reduction in I_{ON}, the back-bias underdrain TFET (BBUD-TFET) is proposed, in which the back biasing is applied on the p-Si pocket under the drain region. The BBUD-TFET achieves complete elimination of I_{AMB} as well as a significant improvement in SS and I_{ON}. The performance of the BB-TFET and BBUD-TFET is investigated using 2-D TCAD simulations in the ATLAS device simulator [19].

2 The simulation setup

The BB-TFET and BBUD-TFET structures are implemented in the TCAD simulator by invoking suitable models. In this study, the Lombardi mobility (CVT) model is used to include the effect of the concentration- and field-dependent mobility. The Shockley–Read–Hall (SRH) model is chosen to incorporate the phenomenon of carrier recombination. The bandgap narrowing (BGN) model is selected to include the effect of the high concentration in the bandgap. Fermi–Dirac statistics is employed to incorporate certain properties of the highly doped region. Moreover, the nonlocal band-to-band tunneling model is used to simulate the tunneling effect in the devices. To calibrate the simulation setup, a prefabricated TFET [20] is implemented and simulated using the above-mentioned models. Figure 1 shows a comparison of the simulated and fabricated transfer characteristics of the published TFET structure, revealing a good match between the simulated and experimental results.

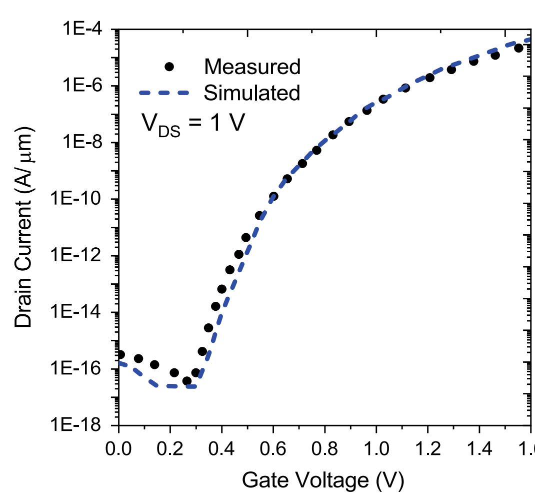


Fig. 1 The calibration of the simulation setup using a prefabricated TFET [20]

2.1 The device structures, results, and discussion

A cross-sectional view of the BB-TFET structure on SOI is shown in Fig. 2. The structure consists of an ultrathin SiO_2 layer over the *p*-Si region placed on the BOX. The various device structural parameters used in this study are: gate oxide (GOX) thickness (T_{OX}) = 1 nm, channel length (L) = 50 nm, channel thickness (T_{si}) = 10 nm, p^+-source region doping = 1×10^{20} cm^{-3}, *n*-channel doping = 1×10^{17} cm^{-3}, n^+-drain region doping = 5×10^{18} cm^{-3}, *p*-Si layer doping = 1×10^{15} cm^{-3}, and the work function of the gate material = 4.7 eV, while the dimension of the ultrathin SiO_2 (T_{OB}) is varied from 2 to 10 nm. A negative back-bias voltage (V_{BB}) is applied to the *p*-Si layer from the drain to source uniformly. The application of V_{BB} reduces the electric field at the drain/channel and source/channel interfaces. Note that the electric field at the drain/channel interface is responsible for the I_{AMB} in the TFET structure. Therefore, the reduction in the electric field at this interface leads to suppression of I_{AMB}. The I_{ON} of the device depends on the tunneling of carriers at the source/channel interface, hence a reduction in the electric field at this interface results in a degradation in I_{ON}.

The effect of V_{BB} on the transfer characteristics of the BB-TFET is shown in Fig. 3. Note from this figure that the application of a negative V_{BB} entirely suppresses the I_{AMB} but also decreases the I_{ON} of the device. This figure reveals that, when V_{BB} is increased from −1 to −2 V, the I_{AMB} in the device is completely suppressed but the I_{OFF} increases. In the OFF-state condition ($V_{GS} = 0$ V), the current in the BB-TFET is obtained as 1.49×10^{-11} A/µm, 1.5×10^{-17} A/µm, and 3.8×10^{-17} A/µm at $V_{BB} = 0$ V, $V_{BB} = -1$ V, and $V_{BB} = -2$ V, respectively. Further, changing V_{BB} from −1 to −2 V significantly reduces the I_{ON}. In the ON-state condition ($V_{GS} = 1.2$ V), the I_{ON} is found to be 1.64×10^{-6} A/µm, 8.8×10^{-7} A/µm, and 3.76×10^{-8} A/µm at $V_{BB} = 0$ V, $V_{BB} = -1$ V, and $V_{BB} = -2$ V, respectively. For $V_{BB} = -1$ V, the SS and threshold voltage (V_t) are calculated as 17.5 mV/dec and 0.84 V, respectively.

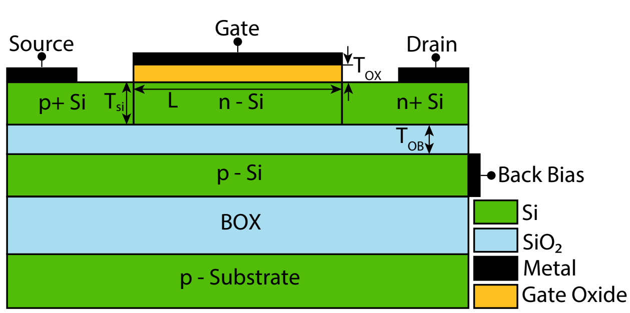


Fig. 2 A schematic cross-sectional view (not to the scale) of the BB-TFET

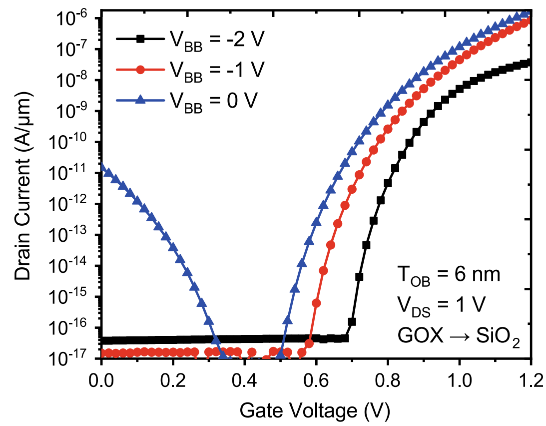


Fig. 3 The transfer characteristics of the BB-TFET at different back-bias voltages

The reduction in I_{AMB} and I_{ON} with V_{BB} can be better explained based on the electric field distribution in the structure.

The I_{ON} and I_{AMB} of the TFET depend on the band-to-band tunneling (BTBT) at the source/channel and drain/channel junctions, respectively [21]. The BTBT rate (G_{BTBT}) depends on the local electric field (ε) at the junction according to the equation [22]

$$G_{BTBT} = A\varepsilon^{\sigma}\exp\left(-\frac{B}{\varepsilon}\right), \quad (1)$$

where A is a constant related to the effective electron mass, B is the tunneling probability constant, and σ is the transition constant. The 2-D electric field distribution in the BB-TFET with and without back bias in the OFF-state is shown in Fig. 4. As depicted in Fig. 4b, in the OFF-state ($V_{GS} = 0$ V), the application of the back bias drastically reduces the

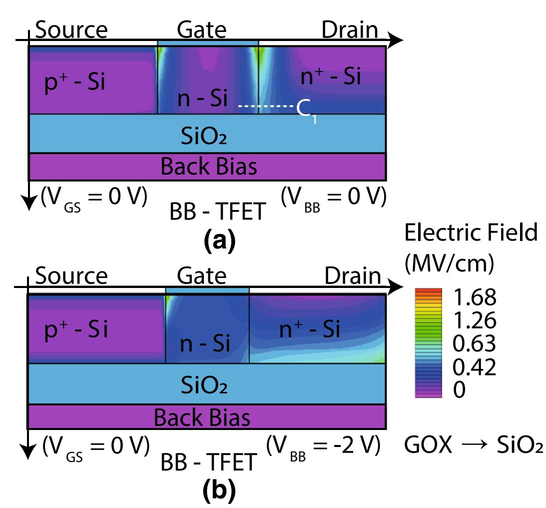


Fig. 4 The electric field distribution in the BB-TFET in the OFF-state at **a** $V_{BB} = 0$ V and **b** $V_{BB} = -2$ V

electric field at the drain/channel interface compared with Fig. 4a. This reduction in the electric field at the drain/channel junction leads to complete suppression of I_{AMB}. Note that, although I_{AMB} is suppressed with the back bias, I_{OFF} increases as V_{BB} is increased from 1 to −2 V due to the higher electric field in the drain region.

Furthermore, the effect of the back bias on the transfer characteristics of the BB-TFET can be explained based on the tunneling probability. The tunneling probability (T_{WKB}) in a TFET is given by the Wentzel–Kramer–Brillouin (WKB) approximation, which is written as [2, 23]:

$$T_{\mathrm{WKB}} \approx \exp\left(-\frac{4\lambda\sqrt{2m^{*}}\sqrt{E_{\mathrm{g}}^{3}}}{3q\hbar(E_{\mathrm{g}}+\Delta\phi)}\right), \tag{2}$$

where λ and $\Delta\phi$ denote the tunneling width and the effective tunneling energy range, respectively (as shown in Fig. 5). The effective electron mass is m^*, and the bandgap energy is E_g.

Figure 5 shows the energy band diagram of the BB-TFET at different V_{BB} values along the cut line C_1 in the OFF-state. This figure reveals a significant overlap between the conduction band (CB) and valance band (VB) at the drain/channel junction without a back bias ($V_{BB} = 0$ V). This increases the T_{WKB} at the drain/channel interface, leading to a large I_{AMB}. On the other hand, with the application of the back bias, there is no overlap between the CB and VB at the drain/channel interface, hence the I_{AMB} is completely eliminated.

In the ON-state ($V_{GS} = 1.2$ V), the effect of the back bias on the electric field and energy band diagram at the source/channel interface is illustrated in Figs. 6 and 7. It is clear from Fig. 6a, b that the back bias also reduces the electric field significantly at the source/channel junction. This decrease in the electric field at the source/channel junction degrades the I_{ON} of the BB-TFET. Meanwhile, it is evident from the energy band diagram (Fig. 7) that the λ remains almost unaffected by the back bias, while $\Delta\phi$ reduces with an increase in the negative V_{BB}. As observed from this figure, the reduction in $\Delta\phi$ is small at $V_{BB} = -1$ V as compared with at $V_{BB} = -2$ V. Therefore, the I_{ON} decreases by a small amount at $V_{BB} = -1$ V when compared with I_{ON} without a back bias. On the other hand, the I_{ON} decreases significantly at $V_{BB} = -2$ V due to the large reduction in $\Delta\phi$.

Although the back bias in the BB-TFET suppresses the ambipolar current completely at $V_{BB} = -1$ V, it also degrades the I_{ON}. This is due to the fact that the negative back bias reduces the $\Delta\phi$ at the drain/channel and source/channel junctions. To overcome this effect of V_{BB} on the

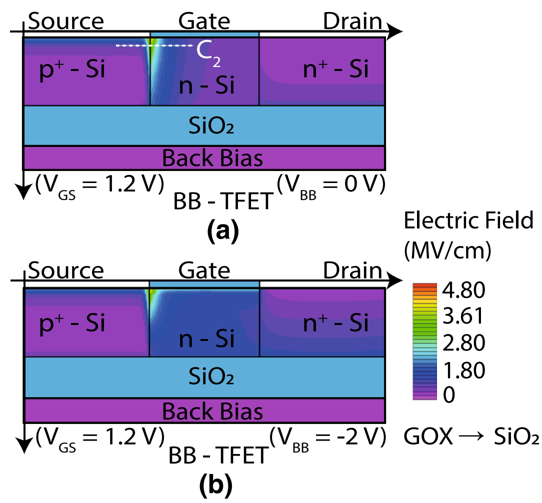


Fig. 6 The electric field distribution in the BB-TFET in the ON-state at **a** $V_{BB} = 0$ V and **b** $V_{BB} = -2$ V

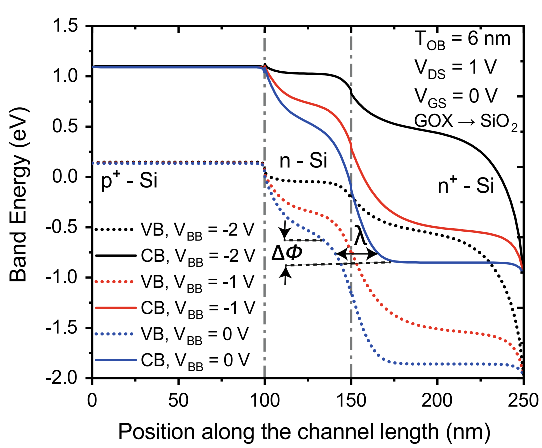


Fig. 5 The energy band diagram along the cut line C_1 in the BB-TFET with SiO_2 as the GOX in the OFF-state

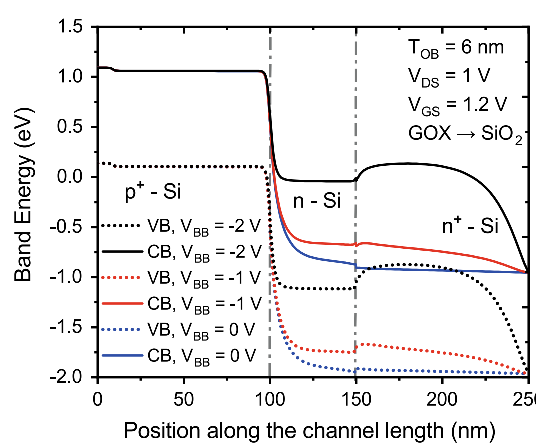


Fig. 7 The energy band diagram along the cut line C_2 in the BB-TFET with SiO_2 as the GOX in the ON-state

I_{ON} in the BB-TFET, the back bias can be applied under the drain region only, resulting in the new structure called the BBUD-TFET as proposed in Fig. 8. In this structure, a *p*-Si region is introduced below the drain, being separated from the *n*+ drain by an oxide with thickness of T_{OB}. The V_{BB} is applied to the *p*-Si region, which will mainly affect the drain/channel junction but with a negligible effect on the source/channel interface. The other structural parameters of the BBUD-TFET remain identical to those of the BB-TFET to enable comparison of their performance parameters.

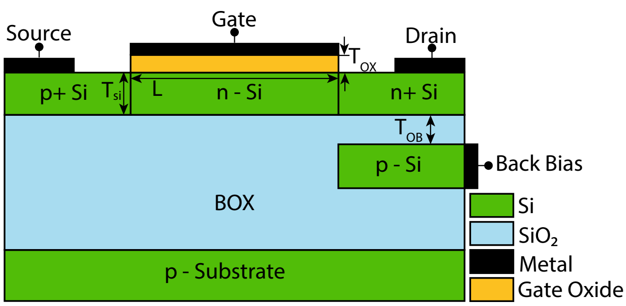
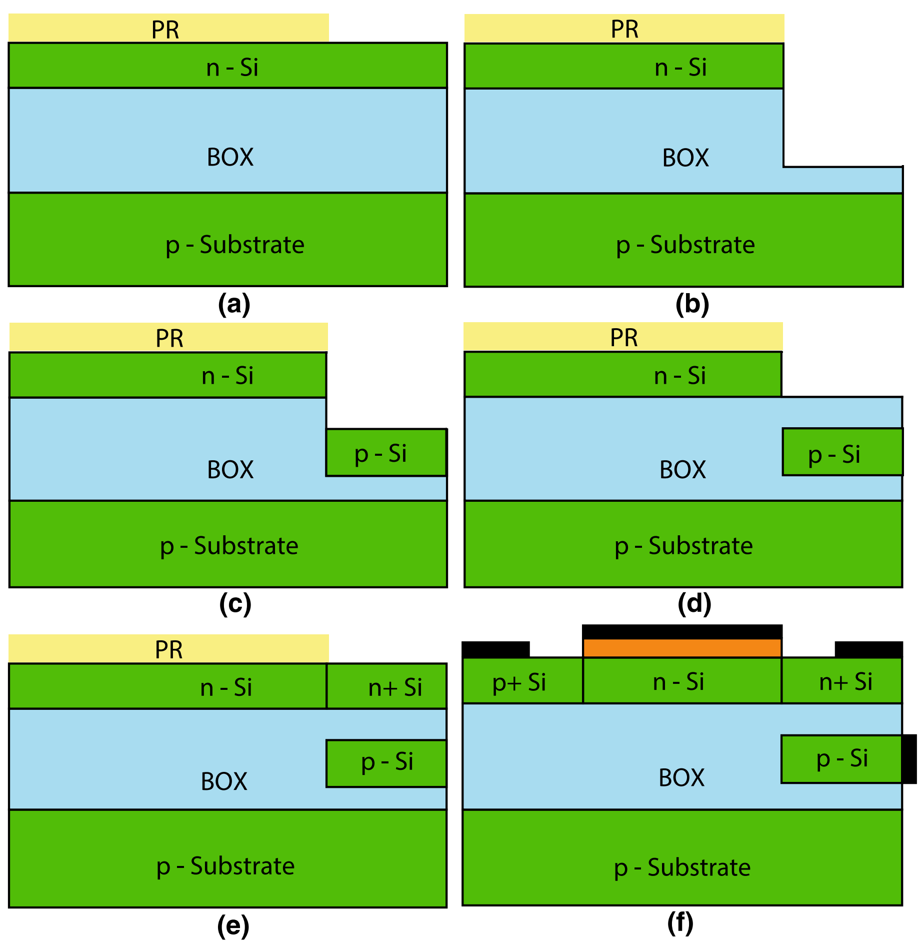


Fig. 8 A schematic cross-sectional view (not to the scale) of the BBUD-TFET

The fabrication steps for the BBUD-TFET are illustrated in Fig. 9. Initially, an SOI wafer with the required *n*-channel concentration is taken. Photoresist (PR) is applied over the whole wafer then patterned as shown in Fig. 9a. Reactive-ion etching (RIE) is used to remove the desired *Si n*-epitaxial layer as well as SiO_2 (BOX) layer to obtain the trench structure shown in Fig. 9b. The RIE process offers a high selectivity ratio of 35:1 for both Si and SiO_2. In the next step, *p*-type Si is grown in the trench, as shown in Fig. 9c. The growth of Si over SiO_2 is achieved using a chemical vapor deposition (CVD) process in which the epitaxial layer is seeded through an opening in the SiO_2 surface. This growth is carried out using a mixture of SiH_2Cl_2, H_2, and HCl in the temperature range of 1050 to 1200 °C. To avoid problems related to the occurrence of silicon nucleation over SiO_2, which would introduce defects into the overgrowing Si epitaxial layer, the growth process is carried out in a series of growth/etch steps [24]. As illustrated in Fig. 9d, a SiO_2 layer with thickness T_{OB} is deposited over the *p*-Si in the trench. In the next step, $n^+ - Si$ is grown over the SiO_2 to form the drain region of the TFET, as shown in Fig. 9e. Finally, as

Fig. 9 The fabrication steps for the BBUD-TFET structure



shown in Fig. 9f, the proposed BBUD-TFET structure is obtained using the same fabrication steps as applied for a conventional TFET [25, 26]. Note that, in the BBUD-TFET, the p-Si region is aligned with the n^+ drain region, which is advantageous from the fabrication point of view.

The transfer characteristics of the BBUD-TFET for different values of V_{BB} are plotted in Fig. 10. Note from this figure that the OFF-state characteristics of the BBUD-TFET are identical to those of the BB-TFET. However, the effect of V_{BB} on I_{ON} is significantly reduced in the BBUD-TFET. Therefore, the I_{ON} in the BBUD-TFET is higher than that in the BB-TFET. At $V_{BB} = -1$ V, the I_{ON} and I_{OFF} of the BBUD-TFET are found to be 1.71×10^{-6} A/μm and 1.54×10^{-17} A/μm, respectively. Moreover, at $V_{BB} = -1$ V, the SS and V_t are obtained as 15.2 mV/dec and 0.79 V, respectively.

It is clear from Fig. 11a, b that the electric field contours at the drain/channel junction are almost identical for both structures. This fact is also illustrated by the energy band diagram shown in Fig. 12, in which there is negligible change in λ and $\Delta\phi$. Therefore, the OFF-state characteristics of the BB-TFET and BBUD-TFET are identical.

Figure 13a and b show the effect of V_{BB} on the electric field distribution in the BB-TFET and BBUD-TFET in the ON-state condition, respectively. It is observed from this figure that the electric field at the source/channel junction in the BBUD-TFET is higher than that in the BB-TFET with a back bias. Furthermore, it is clear from the energy band diagram shown in Fig. 14 that the λ decreases while $\Delta\phi$ increases with the back bias in the BBUD-TFET in comparison with BB-TFET. Therefore, the effect of V_{BB} at the source/channel junction of the BBUD-TFET is lesser compared with in the BB-TFET, hence the I_{ON} in the BBUD-TFET is higher than that in the BB-TFET.

Moreover, the transfer characteristics of the BBUD-TFET can be further improved by using a high-κ dielectric material as the GOX [27, 28]. In this work, the BBUD-TFET structure is also simulated with the replacement of SiO_2 by HfO_2 as the GOX. Note that the thickness of the HfO_2 is kept the same as that of the SiO_2 (1 nm). Figure 15 shows the transfer characteristics of the BBUD-TFET with HfO_2 as the GOX. As shown in this figure, without a back bias ($V_{BB} = 0$), both the I_{ON} and I_{AMB} of the BBUD-TFET with HfO_2 as the GOX are substantially higher than for the BBUD-TFET with SiO_2 as the GOX (as shown in Fig. 10). However, the V_{BB} in this device also results in complete elimination of the I_{AMB} with only slight degradation in I_{ON}. It is observed that, for $V_{BB} = -1$ V, the device exhibits the lowest I_{OFF} without any compromise in I_{ON}. At $V_{BB} = -1$ V, the I_{ON} and I_{OFF} of the BBUD-TFET with HfO_2 as the GOX are found to be 3.13×10^{-4} A/μm and 1.77×10^{-17} A/μm,

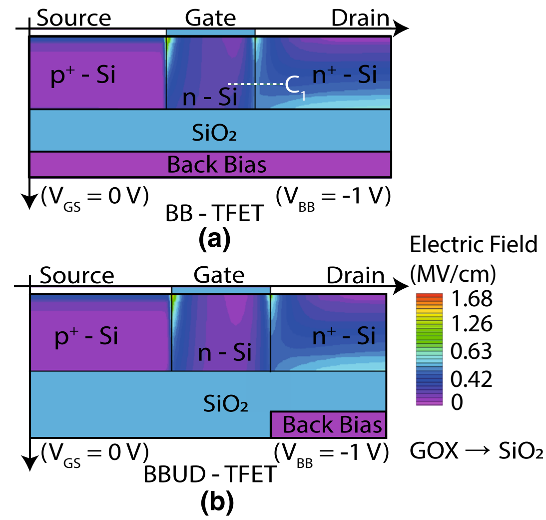


Fig. 11 The OFF-state electric field distribution in the **a** BB-TFET and **b** BBUD-TFET with SiO_2 as the GOX

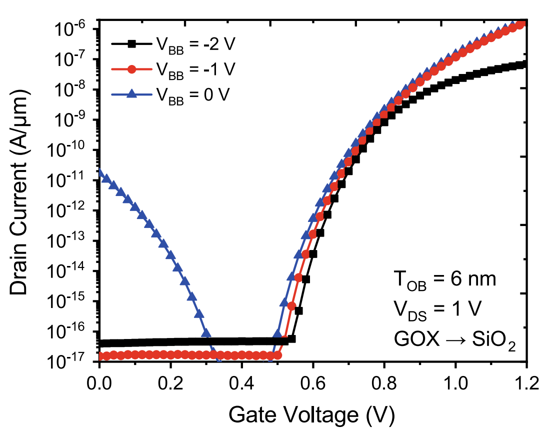


Fig. 10 The transfer characteristics of the BBUD-TFET

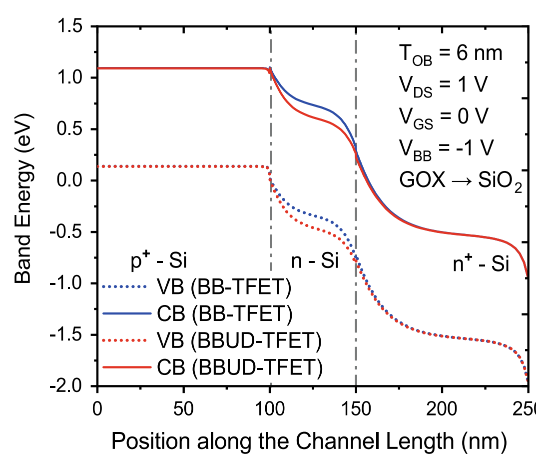


Fig. 12 The OFF-state energy band diagram along the cut line C_1 in the BB-TFET and BBUD-TFET with SiO_2 as the GOX

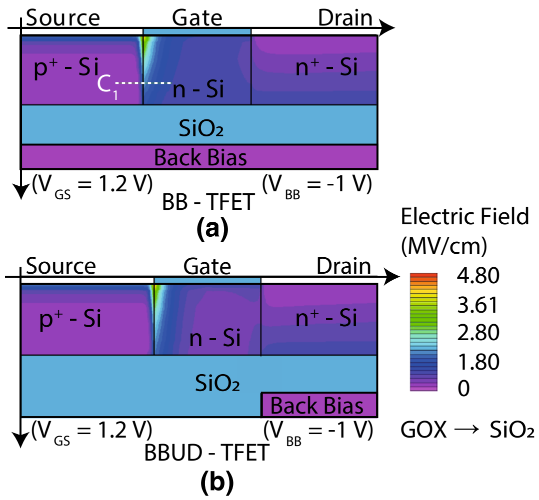


Fig. 13 The ON-state electric field distribution in the **a** BB-TFET and **b** BBUD-TFET with SiO_2 as the GOX

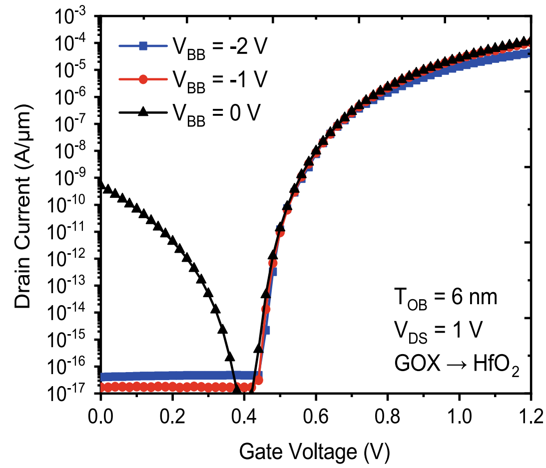


Fig. 15 The transfer characteristics of the BBUD-TFET with HfO_2 as the GOX

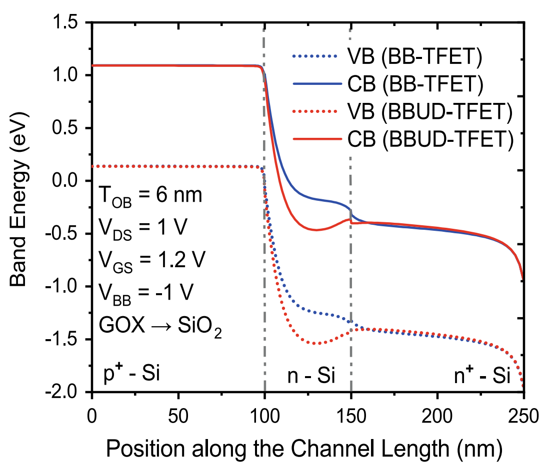


Fig. 14 The ON-state energy band diagram along the cut line C_1 in the BB-TFET and BBUD-TFET with SiO_2 as the GOX

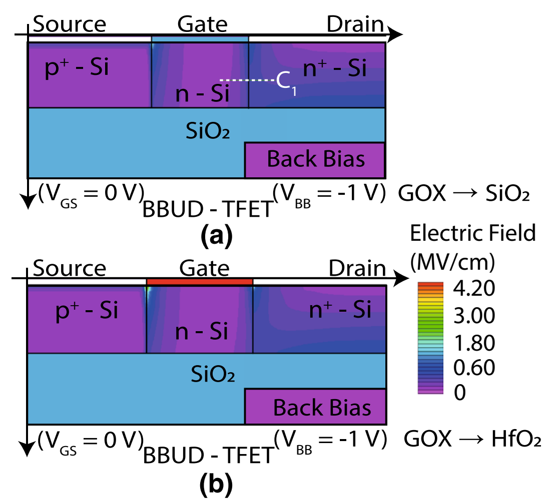


Fig. 16 The OFF-state electric field distribution in the BBUD-TFET with **a** SiO_2 and **b** HfO_2 as the GOX

respectively. Moreover, at $V_{BB} = -1$ V, the SS and V_t are obtained as 7.6 mV/dec and 0.42 V, respectively.

This improvement in the transfer characteristics of the BBUD-TFET can be explained with the help of the electric field distribution and energy band diagram with SiO_2 and HfO_2 as the GOX (Figs. 16, 17). As observed from Fig. 16, the electric field at both junctions near the gate is higher in the case of HfO_2. On the other hand, the electric field is identical in both structures near the channel/SiO_2 interface due to the back-bias effect. The cut line C_1 is taken at the drain/channel interface near to the back surface. The energy bands overlap with each other in both cases, hence the I_{OFF} is identical in both devices. The electric field contours and energy band diagram in the BBUD-TFET in the ON-state are shown in Figs. 18 and 19. From Fig. 18, it is observed that the electric field at the source/channel interface in the BBUD-TFET is higher with HfO_2 as compared with SiO_2. This enhanced electric field at the source/channel junction results in greater energy band bending, as illustrated in Fig. 19.

3 The optimization of the BBUD-TFET

Figure 20 shows the transfer characteristics of the BBUD-TEFT with HfO_2 as the GOX for different values of T_{OB} at $V_{BB} = -1$ V. Note from this figure that I_{OFF} decreases with an increase in T_{OB} up to 6 nm. Thereafter, I_{AMB} increases due to the reduced control of the V_{BB} over the electric field at the drain/channel junction. On the other hand, the I_{ON}

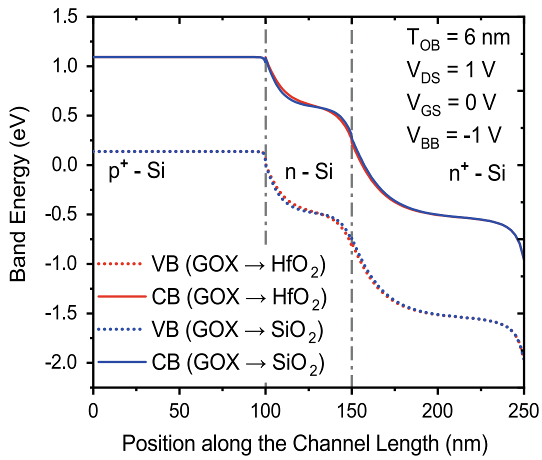


Fig. 17 The OFF-state energy band diagram along the cut line C_1 in the BBUD-TFET with SiO_2 and HfO_2 as the GOX

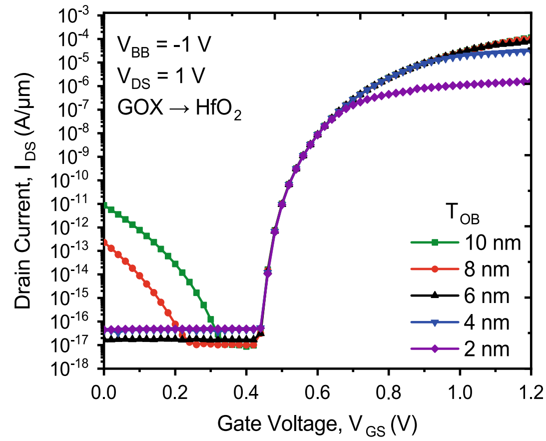


Fig. 20 The effect of T_{OB} on the transfer characteristics of the BBUD-TFET with HfO_2 as the GOX

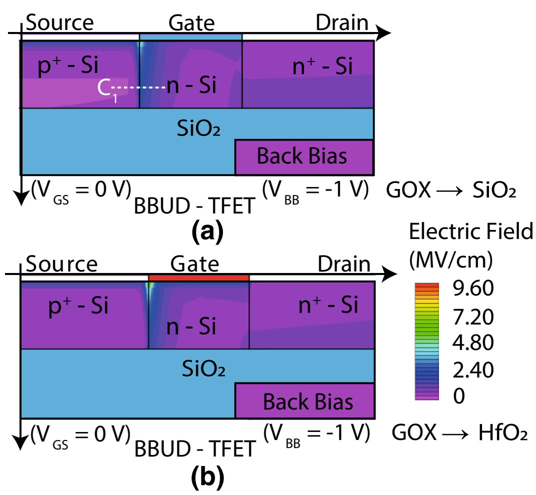


Fig. 18 The ON-state electric field distribution in the BBUD-TFET with **a** SiO_2 and **b** HfO_2 as the GOX

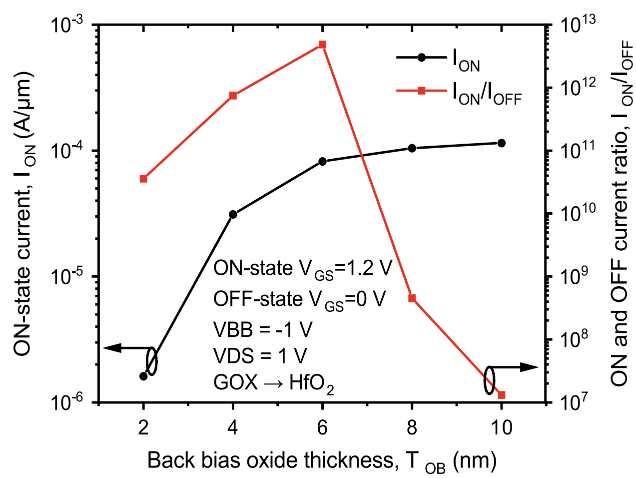


Fig. 21 The variation in I_{ON} and the I_{ON}/I_{OFF} ratio with T_{OB} for the BBUD-TFET with HfO_2 as the GOX

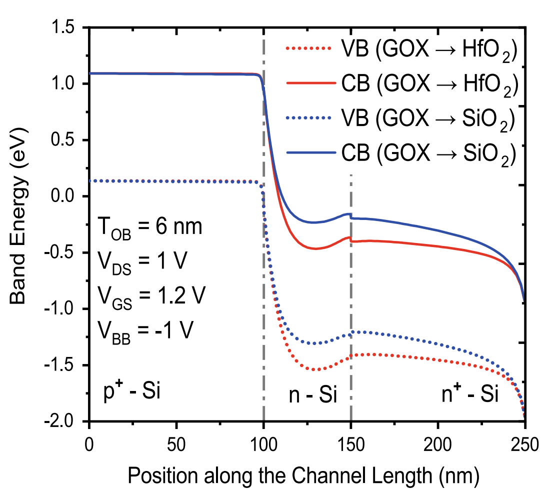


Fig. 19 The ON-state energy band diagram along the cut line C_1 in the BBUD-TFET with SiO_2 and HfO_2 as the GOX

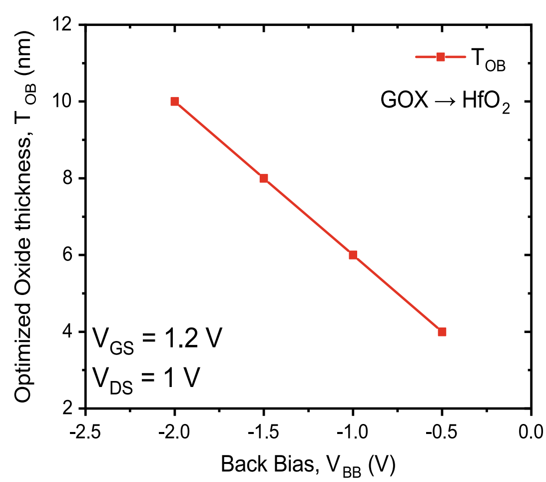


Fig. 22 The optimized values of T_{OB} for different values of V_{BB} for the BBUD-TFET with HfO_2 as the GOX

Table 1 A comparison of the performance parameters of the BB-TFET and BBUD-TFET structures with other reported TFETs

Performance	Parameters		
	I_{AMB} or I_{OFF} (A/μm)	I_{ON}/I_{OFF} ratio	SS (mV/dec)
ED-FE-SB TFET [11]	8.74×10^{-9}	6.74×10^{7}	56
AJN TFET [12]	7.5×10^{-12}	3.87×10^{9}	38
DMCG-TFET [9]	2.29×10^{-17}	7.22×10^{11}	19
HDB *p–n–p–n* TFET [17]	$\sim 10^{-16}$	$\sim 10^{10}$	-
EHB TFET [13]	9.09×10^{-17}	2.55×10^{9}	17.75
DMG TFET [14]	3.0×10^{-13}	6.67×10^{9}	17
BB-TFET (this work)	1.50×10^{-17}	5.87×10^{10}	17.53
BBUD-TFET (this work)	1.54×10^{-17}	1.11×10^{11}	15.21
BBUD-TFET (GOX → HfO_2) (this work)	1.77×10^{-17}	1.77×10^{13}	7.60

increases continuously with an increase in T_{OB} because, for higher values of T_{OB}, the effect of V_{BB} on the source/channel junction is diminished. To determine the optimum value of T_{OB} at $V_{BB} = -1$ V, the I_{ON} and I_{ON}/I_{OFF} ratio are plotted in Fig. 21, clearly revealing that the I_{ON}/I_{OFF} ratio is maximum for $T_{OB} = 6$ nm. Therefore, the optimum value of T_{OB} is taken as 6 nm for $V_{BB} = -1$ V. Similarly, the optimum value of T_{OB} is found for other values of V_{BB} and plotted in Fig. 22. The optimum value of T_{OB} increases for higher values of V_{BB}.

The performance parameters of the BB-TFET and BBUD-TFET structures are compared with other TFETs reported in literature in Table 1. It is evident that the BBUD-TFET with HfO_2 as the GOX provides a I_{ON}/I_{OFF} ratio of 1.77×10^{13}, which is significantly higher than that ($\sim 10^2$) of the reported dual material control gate (DMCG)-TFET structure [9]. Further, it is also observed that the BBUD-TFET with HfO_2 as the GOX provides the lowest value of SS when compared with the other reported structures.

4 Conclusions

The effect of the back-bias voltage on the transfer characteristics of the BB-TFET and BBUD-TFET is evaluated and investigated using 2-D TCAD simulations. The back-bias voltage in the BB-TFET reduces the electric field at both the source/channel and drain/channel junctions, which leads to a reduction in the tunneling probability and hence a substantial reduction in the I_{AMB} and I_{ON} of the device. At $V_{BB} = -1$ V, the I_{ON} and I_{OFF} of the BB-TFET are found to be 2.24×10^{-7} A/μm and 1.18×10^{-17} A/μm, respectively. To overcome the effect of V_{BB} at the source/channel junction in the BB-TFET, the conventional TFET structure is modified to the BBUD-TFET, in which the V_{BB} affects mainly the drain/channel junction. The BBUD-TFET is then studied with SiO_2 or HfO_2 as the GOX. The simulation results reveal that the BBUD-TFET with HfO_2 as the GOX offers complete elimination of I_{AMB} but with no effect on I_{ON}. At $V_{BB} = -1$ V, the I_{ON} and I_{OFF} of the BBUD-TFET with HfO_2 as the GOX are found to be 3.13×10^{-4} A/μm and 1.77×10^{-17} A/μm, respectively. The I_{ON}/I_{OFF} ratio of the BBUD-TFET with HfO_2 as the GOX is found to be 1.77×10^{13}, which is much higher than for other TFET structures. With a back bias in the ultrathin SOI TFET, the T_{OB} and V_{BB} are two important parameters to control the I_{AMB} in the device. The improvement in the performance parameters of the BB-TFET and BBUD-TFET can be explained with the help of the electric field contours and energy band diagrams of the devices. The proposed device exhibits superior performance parameters as compared with other TFET structures reported in literature. Thus, the proposed BBUD-TFET is an attractive candidate for use in low-power switching applications.

References

1. Choi, W.Y., Park, B.G., Lee, J.D., Liu, T.J.K.: Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Lett. **28**(8), 743 (2007). https://doi.org/10.1109/LED.2007.901273
2. Ionescu, A.M., Riel, H.: Tunnel field-effect transistors as energy-efficient electronic switches. Nature **479**(7373), 329 (2011). https://doi.org/10.1038/nature10679
3. Seabaugh, A.C., Zhang, Q.: Low-voltage tunnel transistors for beyond CMOS logic. Proc. IEEE **98**(12), 2095 (2010). https://doi.org/10.1109/JPROC.2010.2070470
4. Krishnamohan, T., Kim, D., Raghunathan, S., Saraswat, K.: Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and <60 mV/dec subthreshold slope. In: 2008 IEEE International Electron Devices Meeting (IEEE, 2008), pp. 1–3 (2008). https://doi.org/10.1109/IEDM.2008.4796839
5. Hraziia, A., Vladimirescu, A., Amara, A., Anghel, C.: An analysis on the ambipolar current in Si double-gate tunnel FETs.

Solid State Electron. **70**, 67 (2012). https://doi.org/10.1016/j.sse.2011.11.009
6. Abdi, D.B., Kumar, M.J.: Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain. IEEE J. Electron Devices Soc. **2**(6), 187 (2014). https://doi.org/10.1109/JEDS.2014.2327626
7. Kondekar, P., Sharma, D., Nigam, K., Raad, B.: Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement. Electron. Lett. **52**(9), 770 (2016). https://doi.org/10.1049/el.2015.4348
8. Narang, R., Saxena, M., Gupta, R.S., Gupta, M.: Assessment of ambipolar behavior of a tunnel FET and influence of structural modifications. J. Semicond. Technol. Sci. **12**(4), 482 (2012). https://doi.org/10.5573/JSTS.2012.12.4.482
9. Nigam, K., Kondekar, P., Sharma, D.: Approach for ambipolar behaviour suppression in tunnel FET by workfunction engineering. Micro Nano Lett. **11**(8), 460 (2016). https://doi.org/10.1049/mnl.2016.0178
10. Shaker, A., El Sabbagh, M., El-Banna, M.M.: Influence of drain doping engineering on the ambipolar conduction and high-frequency performance of TFETs. IEEE Trans. Electron Devices (2017). https://doi.org/10.1109/TED.2017.2724560
11. Singh, S., Kondekar, P.N.: A novel electrostatically doped ferroelectric Schottky barrier tunnel FET: process resilient design. J. Comput. Electron. **16**(3), 685 (2017). https://doi.org/10.1007/s10825-017-0987-6
12. Rahimian, M., Fathipour, M.: Asymmetric junctionless nanowire TFET with built-in n+ source pocket emphasizing on energy band modification. J. Comput. Electron. **15**(4), 1297 (2016). https://doi.org/10.1007/s10825-016-0895-1
13. Loan, S.A., Alharbi, A.G., Rafat, M.: Ambipolar leakage suppression in electron-hole bilayer TFET: investigation and analysis. J. Comput. Electron. **17**(3), 977 (2018). https://doi.org/10.1007/s10825-018-1184-y
14. Bal, P., Ghosh, B., Mondal, P., Akram, M.W., Tripathi, B.M.M.: Dual material gate junctionless tunnel field effect transistor. J. Comput. Electron. **13**(1), 230 (2014). https://doi.org/10.1007/s10825-013-0505-4
15. Guo, A., Matheu, P., Liu, T.J.K.: SOI TFET ION/IOFF enhancement via back biasing. IEEE Trans. Electron Devices **58**(10), 3283 (2011). https://doi.org/10.1109/TED.2011.2161480
16. Matheu, P., Ho, B., Jacobson, Z.A., Liu, T.K.: Planar GeOI TFET performance improvement with back biasing. IEEE Trans. Electron Devices **59**(6), 1629 (2012). https://doi.org/10.1109/TED.2012.2191410
17. Sahay, S., Kumar, M.J.: Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX. IEEE Trans. Electron Devices **62**(11), 3882 (2015). https://doi.org/10.1109/TED.2015.2478955
18. Wang, H., Han, G., Liu, Y., Zhang, J., Hao, Y., Jiang, X.: Theoretical investigation of backgate-biasing effects on ultrathin-body GeSn based tunneling FET. In: 2017 IEEE SOI-3D-Subthreshold Microelectronics Unified Conference, S3S 2017, pp. 1–3 (2018). https://doi.org/10.1109/S3S.2017.8309214
19. Silvaco Inc., Atlas User's Manual. Silvaco Inc. (2016)
20. Boucart, K., Ionescu, A.M.: Double-gate tunnel FET with high-κ gate dielectric. IEEE Trans. Electron Devices **54**(7), 1725 (2007). https://doi.org/10.1109/TED.2007.899389
21. Shih, C.H., Chien, N.D.: Bandgap-dependent onset behavior of output characteristics in line-tunneling field-effect transistors. J. Comput. Electron. **16**(3), 696 (2017). https://doi.org/10.1007/s10825-017-1020-9
22. Adell, P.C., Barnaby, H.J., Member, S., Schrimpf, R.D.: Band-to-band tunneling (BBT) induced leakage current enhancement in irradiated fully depleted SOl devices. IEEE Trans. Nucl. Sci. **54**(6), 2174 (2007)
23. Joshi, T., Singh, Y., Singh, B.: Dual-channel trench-gate tunnel FET for improved ON-current and subthreshold swing. Electron. Lett. **55**(21), 1152 (2019). https://doi.org/10.1049/el.2019.2219
24. Jastrzebski, L., Corboy, J.F., McGinn, J.T., Pagliaro, R.: Growth process of silicon over SiO_2 by CVD: epitaxial lateral overgrowth technique. J. Electrochem. Soc. **130**(7), 1571 (1983). https://doi.org/10.1149/1.2120037
25. Devi, W.V., Bhowmick, B.: Optimisation of pocket doped junctionless TFET and its application in digital inverter. Micro Nano Lett. **14**(1), 69 (2018). https://doi.org/10.1049/mnl.2018.5086
26. Strangio, S., Palestri, P., Esseni, D., Selmi, L., Crupi, F., Richter, S., Zhao, Q.T., Mantl, S.: Impact of TFET unidirectionality and ambipolarity on the performance of 6T SRAM cells. IEEE J. Electron Devices Soc. **3**(3), 223 (2015). https://doi.org/10.1109/JEDS.2015.2392793
27. Atan, N.B., Ahmad, I.B., Majlis, B.B.Y.: Effects of high-K dielectrics with metal gate for electrical characteristics of 18 nm NMOS device. In: 2014 IEEE international conference on semiconductor electronics (ICSE2014), pp. 56–59 (2014). https://doi.org/10.1109/SMELEC.2014.6920794
28. Kumar, S., Goel, E., Singh, K., Singh, B., Kumar, M., Jit, S.: A compact 2-D analytical model for electrical characteristics of double-gate tunnel field-effect transistors with a SiO_2/high-k stacked gate-oxide structure. IEEE Trans. Electron Devices **63**(8), 3291 (2016). https://doi.org/10.1109/TED.2016.2572610