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Sneak, discharge, and leakage current issues in a high-dimensional 1T1M memristive crossbar

V. A. Demin[1] · I. A. Surazhevsky[1] · A. V. Emelyanov[1,2] · P. K. Kashkarov[1,2,3] · M. V. Kovalchuk[1,2,3]

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Abstract
Memristive crossbar arrays are believed to be the future of high-density nonvolatile memory and neuromorphic systems. However, significant challenges related to the passive crossbar architecture, for example, the sneak current issue, impose limitations on their performance. One of the well-known ways to overcome this problem is to use a one-transistor one-memristor (1T1M) scheme. Nevertheless, for a sufficiently large crossbar, even with a 1T1M architecture, problems appear not only with sneak currents but also with leakage through the gates of the transistors and the discharge of their capacitances. These effects are analyzed herein by simulations and analytically to determine their influence on the performance of a 1T1M crossbar, depending on its dimensions. Numerical results are presented for the examples of $(CoFeB)_x(LiNbO_3)_{100-x}$ nanocomposite and ZrO_2(Y)-based memristive structures. The results reveal that the sneak, discharge, and (to a lesser extent) leakage currents can severely degrade the performance of even a not very large ($< 10^3 \times 10^3$) 1T1M crossbar. Finally, analytical estimates are used to reveal how a well-known, simple special scheme for switching and reading can fix these negative effects, even for a 1T1M memristive crossbar with rather large dimensions ($\sim 10^6 \times 10^6$), taking into account its plausible geometrical size and the scaling dependence of its constituent elements.

Keywords Neuromorphic hardware · Memristor · Crossbar array · 1T1M crossbar · Sneak current · Leakage current · Discharge current · Memristive crossbar performance

1 Introduction

Computation using artificial neural networks is nowadays experiencing a renaissance, as the rapid development of the Internet of Things and the availability of large computing power have made it possible to achieve great results in areas such as image, speech, and text recognition, the development of self-driving cars and drones [1–5], etc. However, with their increasing performance, the operation of such systems also requires growing amounts of additional power. Currently, specialized neuromorphic processors are being developed around the world to overcome this problem [6–10]. It is supposed that they will bring neural computation to a fundamentally new level of performance while reducing the associated energy consumption.

One of the promising hardware approaches in this field is the use of memristors. Their ability to change conductivity under certain external influences (resistive switching effect) has allowed researchers to consider memristors as a model for synapses in the brain [11–13]. On the basis of memristive structures, the implementation of mixed analog–digital hardware multilayer neural networks becomes possible [14–16].

The memristive structure with a crossbar topology is one of the most important parts of the widely investigated neurosynaptic core architecture, storing the weights of a configured neural network. However, this structure has a fundamental problem: when reading the conductivity, sneak paths arise around a target memristor, resulting in some additional current that makes the crossbar inoperable [17]. To suppress such sneak currents, a number of different solutions have been proposed based on the addition of

✉ I. A. Surazhevsky
isurazhevsky@yandex.ru

V. A. Demin
demin_va@nrcki.ru

[1] National Research Center "Kurchatov Institute", Moscow, Russia 123182

[2] Moscow Institute of Physics and Technology (State University), Dolgoprudny, Moscow Region, Russia 141700

[3] Faculty of Physics, Lomonosov Moscow State University, Moscow, Russia 119991

some passive or active components to the crossbar, namely diodes set on unselected bit lines [17] or in a one-diode one-memristor (1D1M) crossbar architecture [18, 19], selectors in a one-selector one-memristor (1S1M) architecture [20, 21], or transistors in a 1T1M architecture [22–25]. Such diodes and selectors are passive elements which, due to their rectifying characteristics, limit the sneak paths. They can be formed using self-consistent technology in one process with the memristive layer. Nevertheless, they have notable drawbacks. Structures with the 1D1M architecture have problems with programming the bipolar memristors (due to the small currents in the reverse branch of the diode), while 1S1M structures show strong nonlinearity in the *I*–*V* curve at the reading voltages, which seriously complicates the operation of neuromorphic systems, where close-to-linear *I*–*V* relations are highly desirable. Also, the variation of the characteristics of even the most advanced memristive devices introduces noticeable distortion into the operation of neural network algorithms [26], which must be taken into account during their implementing [27]. The 1S1M architecture requires higher reading voltages, meaning that device variability can cause more severe disturbance of the memristance reading process [28], also leading to an increase in the power consumption.

The 1T1M crossbar architecture is based on active transistor elements and is immune to the drawbacks mentioned for the structures including diodes and selectors. However, it also suffers from some disadvantages, e.g., the necessity for additional technological operations to develop the transistor layer and combine it with the memristive devices, or potentially a lower on-chip density than in the case without transistors. However, the 1T1M topology has been thoroughly investigated, is technologically well developed based on one-transistor one-resistor (1T1R) random-access memory (RAM) technologies [29, 30], and is operationally very robust and adaptive due to the subtle control of the characteristics of the memristors.

Despite the intrinsic ability of a transistor to control the current through it, there is still a problem, as shown below, with the sneak currents in 1T1M crossbars with high dimensions. Moreover, other sources of imperfect operation are also possible. These are known as discharge and leakage currents, being due to the discharge of the gate capacitance of the field-effect transistor (FET) and the nonideal insulator properties of the gate dielectric, respectively.

This work is devoted to consideration of the contributions of these different parasitic currents to the deterioration of the performance of a 1T1M crossbar. This architecture is chosen as it is appropriate for neuromorphic computing; i.e., it sums the inputs in rows multiplied by memristive weights organized in columns for further signal transmission to neurons from I_{outN} outputs (Fig. 1). The assessment is done both analytically and using model simulations based on two example prospective bipolar memristive structures: (i) a nanocomposite $(CoFeB)_x(LiNbO_3)_{100-x}$ structure with metallic nanogranules of CoFeB in a nonstoichiometric oxide matrix, which demonstrates a highly multilevel resistive state storage ability (> 28 states), high endurance (> 10^6), and good high-to-low resistance ratio $R_{off}/R_{on} > 100$ [31–34], and (ii) an yttria-stabilized zirconia-based structure, as its resistive switching process can be well controlled by adjusting the yttrium doping level and it is compatible with standard complementary metal–oxide–semiconductor (CMOS) technology [35, 36]. However, the presented approach is also applicable to other materials with appealing memristive characteristics, e.g., HfO_x [37], SiN_x [38], and others.

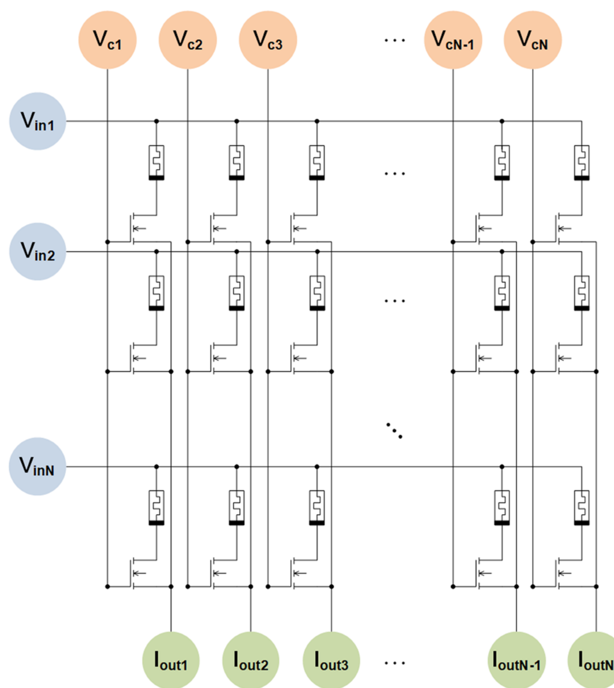

Fig. 1 An $N \times N$ crossbar, where V_{in} and I_{out} designate the input and output lines, and V_c is the crossbar's control line input

2 Device models

(a) The memristor model To determine the applicability of resistive switching elements to neuromorphic systems on a chip, where a large-scale memristive crossbar architecture is required, various memristor models [39–47] with different levels of detail have been developed to date. However, as the dimensions of the simulated crossbar increase, the computing resource requirements increase dramatically. Thus, the memristor model used in this work should meet the following criteria:

- Flexibility: the possibility of adjusting different intrinsic parameters (the threshold voltage, the resistances in the limit states, and others)
- Computational economy: being quite easy to simulate

Based on these criteria, the VTEAM Verilog-A model [40] is chosen. Moreover, models of this kind have potential for further improvement [48].

The *I–V* curve of the memristor in the VTEAM model is shown in Fig. 2. Its only qualitative difference from the *I–V* characteristic of real memristors (Fig. 3) is that the memristor resistance of the model is constant between the values R_{off} and R_{on} over the entire interval from the SET to RESET voltage. However, this discrepancy only results in quantitative changes without affecting the result qualitatively.

Note that the values of R_{off} and R_{on} are chosen in accordance with the physical area of the simulated memristor (Table 1). The dimensions selected for the yttria-stabilized zirconia-based structure correspond to the previously published results for the samples in Ref. [35]. At the same time, the size of the $(CoFeB)_x(LiNbO_3)_{100-x}$ nanocomposite structure is a result of scaling the samples from Ref. [32], assuming a linear dependence of the conductivity on the size of the nanocomposite. The linearity of this dependence is an assumption, but does not affect in principle the conclusions of our study. The real effects of scaling nanocomposite memristors will be studied in future work.

For such large resistances, the influence of the contact wires is minimal; For example, for copper with a resistivity of 17.5×10^{-9} Ωm, even a 1-cm-long wire with cross-sectional area of 1 μm^2 has a resistance of 175 Ω. Meanwhile, the resistance of the transistor in its open state, $R_{FET,on}$, equals 25 kΩ, which is significantly larger and must be taken into account when designing the crossbar.

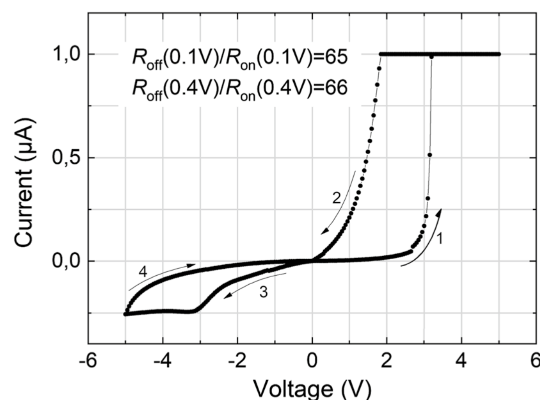

Fig. 3 The experimental *I–V* curve obtained for the $(CoFeB)_x(LiNbO_3)_{100-x}$ memristor with dimensions of $200 \times 500 \times 2\ \mu m^3$ and scaled down to $1 \times 1 \times 2\ \mu m^3$

(b) The FET transistor In this work, an *N*-channel normally closed field-effect transistor model is used, as described in the BSIM-SOI international standard format [49], with gate dimensions of $L = 0.35\ \mu m$ and $W = 1\ \mu m$. This FET is suitable for this study because its geometry and properties approximately correspond to those of the exploited memristors, e.g., in terms of operating currents and switching voltages. It is worth noting that, despite the large dimensions of the transistor, applicable results can be obtained for their use in neuromorphic computing [50].

The simulation process is carried out using Cadence Spectre software.

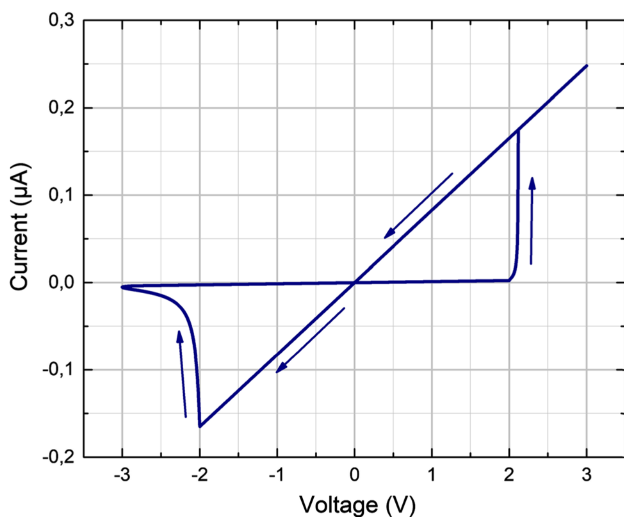

Fig. 2 The *I–V* curve of the VTEAM simulation using scaled $(CoFeB)_x(LiNbO_3)_{100-x}$ memristor parameters

3 The acceptable value of the weight range

Updating the range of synaptic weights affects the learning ability and inference accuracy of the emulated neural network [51]. Consider a memristor-based neural network that requires no fewer than $S = 2^\lambda$ stable levels of memristor conductivity to achieve its admissible performance. Optimally, these can be organized in a uniform distribution of *S* states between the minimal and maximal values of a synaptic

Table 1 The characteristics of the considered memristor structures

No.	Structure	$L \times W \times T$ (μm^3)	R_{on} (MΩ)	R_{off} (MΩ)
1	$(CoFeB)_x(LiNbO_3)_{100-x}$	$8 \times 8 \times 2$	0.2	12.5
2		$4 \times 4 \times 2$	0.8	50
3		$2 \times 2 \times 2$	3.0	200
4		$1 \times 1 \times 2$	12.1	800
5	$Au/Zr/ZrO_2(Y)/TiN/Ti$	$10 \times 10 \times 0.1$	0.003	3
6		$5 \times 5 \times 0.1$	0.008	8

weight range. Note that, for a feedforward neural network classifier, the admissible number λ of weight precision bits is evaluated to be no fewer than 5 [51]. It can certainly be assumed that the smallest precision with which one can process memristive weights equals the minimum value of conductivity $1/R_{\rm off}$. Indeed, at this end of the conductivity range, strong variations in the resistance values are generally observed during cyclic endurance testing [22–25, 29, 30, 34, 36], making it difficult to control the magnitude of the weights with accuracy greater than $1/R_{\rm off}$.

This reasoning leads us to the following necessary condition for acceptable performance of a memristor-based neural network:

$$R_{\rm off}/R_{\rm on} \geq S. \tag{1}$$

Even if one could perfectly control a single memristor state by precisely setting S levels in its conductivity range, the problems arising in a 1T1M memristive crossbar under the influence of parasitic currents will severely deteriorate the accuracy of reading the weights and, consequently, of teaching the whole neural network. Thus, careful evaluation of the influence of parasitic currents on the performance of the crossbar is required.

4 Methods

The first goal of this study is to simulate a 256×256 1T1M crossbar and determine the dimensions of the crosspoint memristive structure for which the distortions introduced by sneak currents are minimum. Then, a 512×512 crossbar is simulated to determine the sneak currents for the memristor with the identified optimal dimensions.

The simulations are implemented in a worst-case mode, where the target memristor is located at the most distant position on the crossbar relative to its inputs and outputs (at the upper-right corner) and set in its high-resistance state, while all other resistive switching elements of the crossbar are in the low-resistance state. Under these conditions, the sneak currents influencing the target memristor will be the largest [52]. Regarding Fig. 1, the target memristor is the element located at the intersection of the lines $V_{\rm in1}$ and $I_{{\rm out}N}$ (the current is measured at the output).

According to the estimates above, the resistance of the contact wires is many times lower than that of the transistors or memristive structures, so it is ignored in this study.

The crossbar modeling consists of two consecutive steps (noting that all the unused inputs and outputs of the circuit are floated by default during the modeling):

1. Since all the memristors are initially in the low-resistance state, it is necessary to switch the target memristor with matrix index (1, 256) to the high-resistance state. This is achieved by applying a voltage pulse with an amplitude of −3 V to the input $V_{\rm in1}$, while connecting the memristor's output to ground. While changing the conductivity of the memristor, the values $V_{\rm c,1-255} = -3.3$ V and $V_{\rm c,256} = 3.3$ V are applied to the control lines of the transistors, to close and open the corresponding bit lines, respectively.
2. The conductivity of the memristor is read by the application of a reading pulse with an amplitude of 1 V to the input $V_{\rm in1}$, while the output current $I_{\rm out,256}$ is analyzed. To close or open the corresponding bit lines, the transistor control voltages $V_{\rm c,1-255} = 0$ V and $V_{\rm c,256} = 3.3$ V are applied, as opposed to the first step. The zero voltage on the control lines for closing the transistors is caused by changing the conductivity of some of the nontarget memristors in the first row of the crossbar under the influence of a total bias of 4.3 V (the sum of the reading and control voltage amplitudes) applied to the series-connected transistor–memristor pairs.

5 The sneak current issue

The simulations of the 256×256 1T1M crossbar show that it is possible to create crossbars on the basis of both analyzed memristive structures with dimensions greater than 256×256 (Tables 2, 3).

This conclusion is due to the following values of the sneak currents obtained during the study of the 256×256 crossbar:

- For the $(\rm CoFeB)_x(\rm LiNbO_3)_{100-x}$ nanocomposite, the maximum sneak current value is less than 51% of the reading current through the memristive structure;
- For the yttria-stabilized zirconia-based structure, the sneak currents do not exceed 0.6% of the operating current in the OFF-state of the target memristor.

The sneak currents in the worst-case mode can be easily evaluated analytically by applying Kirchhoff's laws to the circuit shown in Fig. 1, leading to the following formulae (for $N \gg 1$):

$$I_{\rm sneak} \approx \frac{V_{\rm r}}{R_{\rm FET,off}} N, \tag{2}$$

$$R^{*}_{\rm off} \approx \frac{R_{\rm off} R_{\rm FET,off}/N}{R_{\rm off} + R_{\rm FET,off}/N}, \tag{3}$$

where $V_{\rm r}$ is a reading voltage, $R_{\rm off}$ is the real resistance of a memristor in its fully nonconductive state, $R^{*}_{\rm off}$ is the measured resistance of the upper corner memristor according to

Table 2 The sneak currents for the $(CoFeB)_x(LiNbO_3)_{100-x}$ -based memristive crossbar

No.	$L \times W \times T$ [μm^3]	Crossbar size	I_{outN} [nA]	I_{single}* [nA]	Sneak current** [pA] (%)
1	$8 \times 8 \times 2$	256×256	80.659	79.986	673 (0.84)
2	$4 \times 4 \times 2$	256×256	20.670	19.999	671 (3.35)
3	$2 \times 2 \times 2$	256×256	5.665	4.999	666 (13.3)
4	$1 \times 1 \times 2$	256×256	1.885	1.249	636 (50.9)
		512×512	2.577		1328 (106.3)

*I_{single} is the reading current measured for the single memristive device accessed through the opened *n*-FET transistor

**The sneak current computed as $I_{out,N} - I_{single}$ (in pA) or $(I_{out,N} - I_{single})/I_{out,N}$ (in %)

Table 3 The sneak currents for the Au/Zr/ZrO_2(Y)/TiN/Ti-based memristive crossbar

No.	$L \times W \times T$ [μm^3]	Crossbar size	I_{outN} [nA]	I_{single}* [nA]	Sneak current** [pA] (%)
1	$10 \times 10 \times 0.1$	256×256	333.799	333.103	696 (0.21)
2	$5 \times 5 \times 0.1$	256×256	125.642	124.968	674 (0.54)

*I_{single} is the reading current measured for the single memristive device accessed through the opened *n*-FET transistor

**The sneak current computed as $I_{out,N} - I_{single}$ (in pA) or $(I_{out,N} - I_{single})/I_{out,N}$ (in %)

the reading current at its output, and $R_{FET,off}$ is the resistance of the transistor in its closed state (with 0 V applied to the gate).

The approximate Eq. (2) reveals that the sneak currents do not depend on the characteristics of the memristor at all, because the transistor resistance in the OFF state is much greater than that of the memristor in any resistive state, not to mention the series resistance related to the CMOS metal lines and electrodes, which are a thousand times smaller. Using the BSIM-SOI transistor model, $R_{FET,off}$ with 0 V at its gate is evaluated as 350 GΩ. Using this value, the magnitude of the sneak current for the $256 \times 256 (N = 256)$ crossbar is obtained as approximately 732 pA, which is quite close to the numerical results presented in Tables 2 and 3. The difference may be related to the accuracy of the simulation and taking into account the line resistance of the CMOS metal lines and electrodes in the simulation. At the same time, increasing the line resistance to the level of 3 kΩ, as in Ref. [53], leads to a change in the final result of less than 3%.

For the example using the $(CoFeB)_x(LiNbO_3)_{100-x}$ nanocomposite with dimensions of $1 \times 1 \times 4\,\mu m^3$, the results of the simulation of the 512×512 crossbar are presented in Table 2. In this case, the sneak current equals 1328 pA, which is approximately twice the value for the crossbar with $N = 256$ and corresponds to Eq. (2). Guided by Eq. (1) described in Sect. 2, this crossbar cannot be considered to be fully operational, because the sneak currents distort the R_{off}/R_{on} ratio, resulting in a conventional boundary value less than 32 corresponding to 5 bits of weight precision ($R^*_{off}/R_{on} = 30.4$).

It is possible to estimate the largest size of a 1T1M crossbar that will still be insignificantly influenced by the sneak currents in the operational sense of condition (11). Substituting R_{off} for R^*_{off} in Eq. (1) and using Eq. (3) for R^*_{off}, the maximum allowable size of a 1T1M crossbar can be deduced to be

$$N^{(sneak)}_{max} \approx \frac{R_{FET,off}}{R_{off}} \left(\frac{1}{S} \frac{R_{off}}{R_{on}} - 1 \right). \tag{4}$$

Equation (4) determines the crossbar size when R^*_{off}/R_{on} becomes equal to S, representing the limit of allowable operational functionality due to the parasitic effect of sneak currents in the worst-case mode.

For example, considering the characteristics of the $(CoFeB)_x(LiNbO_3)_{100-x}$ nanocomposite memristor with dimensions of $1 \times 1 \times 2\,\mu m^3$, the largest crossbar achieving a satisfactory range of resistive ratio values ($S = 32, R_{off}/R_{on} = 66$) is approximately 465×465. These results are in good agreement with the numerical estimate presented above.

6 The discharge current issue

The application of the crossbar architecture shown in Fig. 1 via the sequence of steps described in Sect. 4 imposes certain limits: during the switching of control lines, for an accurate current (or conductivity) measurement, it is necessary to discharge the transistors'

capacitances. If this is not done, the resulting discharge of the transistors' gates during control voltage changes will result in strong distortion of the readings of the conductivity of the target memristor.

Figure 4 shows the RESET process of the upper corner memristor with subsequent reading using line $I_{out,256}$ of the 1T1M 256×256 $(CoFeB)_x(LiNbO_3)_{100-x}$ nanocomposite memristor crossbar. Note that the control lines of the non-target bit lines ($V_{c,1-255}$ in Fig. 4c) should be switched to the negative voltage to be closed during the application of the negative potential to the input word line 1 to reset the target upper-right corner memristor. In this process, relaxation current pulses with a time constant of approximately 15 μs are observed at the output (I_{out256} in Fig. 4b). These are associated with the recharging of the transistor gate capacitances. If the reading process (the 1-V pulse in Fig. 4a, f) starts before the current relaxation ends, the result will be significantly different from the expected one, as shown in Fig. 4d; indeed, the output current in this case can exceed the expected one by several orders of magnitude. The general scheme of the crossbar currents (for only one row) is shown in Fig. 4g.

Thus, the influence of this transient process depends on the time that has elapsed since the end of the resistive switching of a memristor. Several solutions can be proposed to fix this problem:

- Waiting for the end of the transition process, which could require quite a lot of time
- Using samples with a larger area, but this approach is undesirable because of problems with both scaling and higher power consumption of the crossbar
- Using an additional simple discharge circuit

The last approach is to use a transimpedance amplifier, whose input is connected to the corresponding output column (Fig. 4g). It connects a column to a virtual ground without significantly reducing the input impedance of the circuit, which is of great importance for large crossbars.

The gray curve in Fig. 4b shows the result for the output current when using this discharge technique. In this case, substantially less time is needed for complete relaxation of the currents in the control lines before switching or reading the target memristor state, and the read result is almost undistorted (Fig. 4e), compared with in the absence of the discharge circuit.

Note that such use of a virtual ground is a well-known technique in electronic circuits with a crossbar architecture

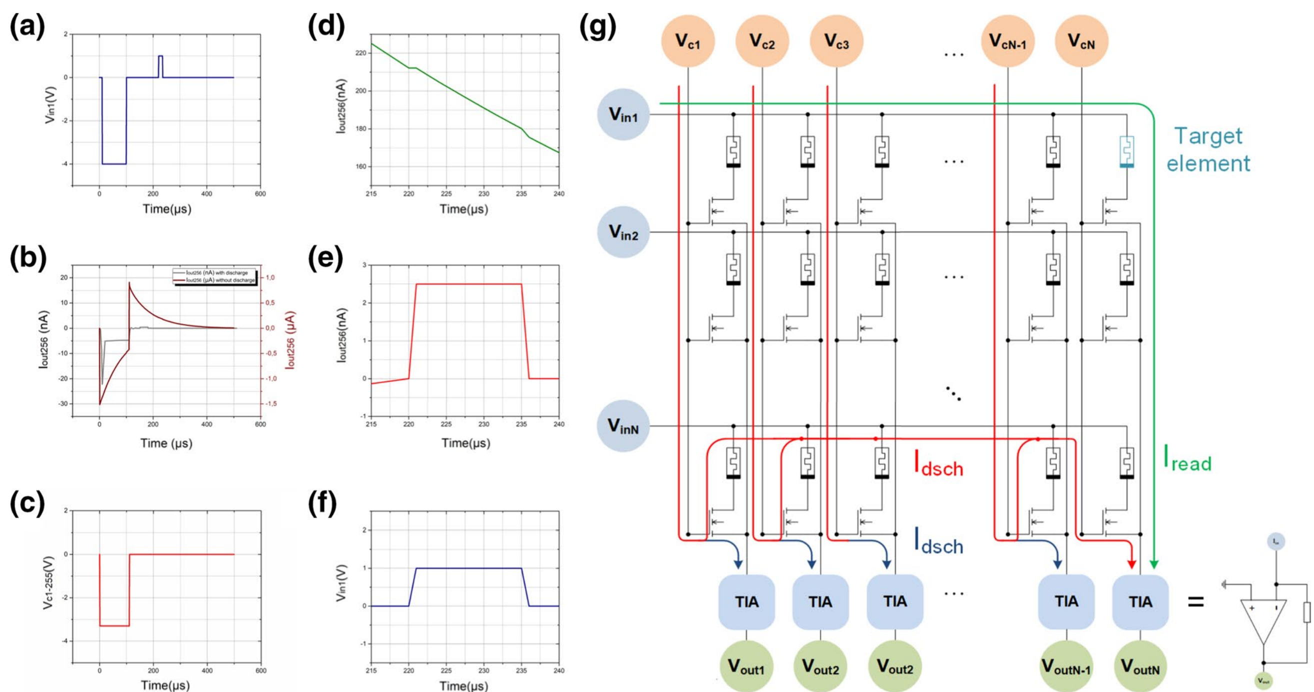

Fig. 4 The process for reading the conductivity of the $(CoFeB)_x(LiNbO_3)_{100-x}$ $1 \times 1 \times 2\,\mu m^3$ memristor and a map of the currents in the crossbar. **a** The input voltage (V_{in1}) trace: the pulse switching the memristor to the OFF state, followed by the reading pulse, **b** the dynamics of the output current ($I_{out,256}$), with an active discharge circuit (grey color) and without it (brown color), **c** the voltage applied to the control lines ($V_{c,1-255}$), **d** the reading current pulse ($I_{out,256}$) in the crossbar without a discharge circuit, **e** the reading current pulse ($I_{out,256}$) in the crossbar with an active discharge circuit, **f** the input voltage reading pulse [enlarged from (**a**)], **g** a map of the currents in the crossbar during the reading process, where the influence of the discharge currents (I_{dsch}) can be attenuated by using a discharge circuit

[54, 55]; the novelty of this work is the demonstration of the relationship between the different kinds of parasitic current effects and the estimation of the maximum allowable size of the 1T1M crossbar that can be built with and without such a discharge circuit in its design.

In this regard, it can be concluded that the effect of the sneak currents on the read result is not as destructive as that of the transient relaxation processes arising in the 1T1M crossbar. Moreover, the addition of the suggested simple discharge circuit at the outputs can solve this problem.

7 The leakage current issue

Besides the sneak and discharge currents, there is one more possible source of result distortion in the 1T1M crossbar architecture, namely the leakage current through the gate dielectric of the transistors in the control lines. This occurs even in the stationary, fully relaxed mode of the crossbar system and appears due to the nonideal properties of the gate dielectric (i.e., its noninfinite resistance).

A leakage current is generated only by those control lines that have a nonzero potential difference between the voltage on the gates of their transistors and the output of the crossbar. Accounting for the fact that, generally, the output is accepted to be grounded, this condition means that nonzero values of V_c are applied to the control lines.

In the worst-case mode, the highest total leakage current is observed in the case of reading the conductivity of the memristive in the upper corner when all the other bit lines are closed by a negative or positive (depending on the type of transistor) voltage V_c on the control lines. Then, these currents flow (up to the flow direction) from the gate to the source of each transistor and through one of the memristors in the rightmost column, opened by the corresponding control line, to the ground at the crossbar output.

The resistance of the gate dielectric layer is generally much greater than that of any transistor channel (source–drain) or memristor resistive state, even in their OFF state. Therefore, the total leakage current at the output for a large ($N \gg 1$) 1T1M crossbar can be estimated as

$$I_{\mathrm{leak}} \approx \frac{V_{\mathrm{c}}}{R_{\mathrm{gd}}} N^2, \tag{5}$$

where R_{gd} is the resistance of the transistor gate dielectric. As noted above, $R_{\mathrm{gd}} \gg R_{\mathrm{FET,off}}$, so such an influence of the leakage currents on the read result is not observed in our numerical experiments. However, Eq. (5) displays a parabolic dependence on the crossbar size N, in contrast to the linear dependence in Eq. (2) for the sneak currents. Thus, for some large dimension of the crossbar, the leakage currents will become close in magnitude to the sneak currents. This will occur for a size

$$N_{\mathrm{ls}} \approx \frac{V_{\mathrm{r}}}{|V_{\mathrm{c}}|} \frac{R_{\mathrm{gd}}}{R_{\mathrm{FET,off}}}, \tag{6}$$

where N_{ls} is on the order of 10^6. This is quite a large size, but degradation of the performance may occur for crossbars with rather smaller dimensions, due to the absolute values of the leakage currents, without regard to the sneak currents. If V_c is a positive blocking voltage (for a p-type FET), then this deterioration effect will occur, again, when $R^*_{\mathrm{off}}/R_{\mathrm{on}} \geq S$, where R^*_{off} is the measured resistance of the target upper-corner memristor in the worst-case mode, distorted due to the leakage currents:

$$\frac{V_{\mathrm{c}}}{R_{\mathrm{gd}}} N^2 + \frac{V_{\mathrm{r}}}{R_{\mathrm{off}}} = \frac{V_{\mathrm{r}}}{R^*_{\mathrm{off}}}. \tag{7}$$

Then,

$$N^{(\mathrm{leak})}_{\max} \approx \sqrt{\frac{R_{\mathrm{gd}}}{R_{\mathrm{off}}} \frac{V_{\mathrm{r}}}{|V_{\mathrm{c}}|} \left(\frac{1}{S} \frac{R_{\mathrm{off}}}{R_{\mathrm{on}}} - 1 \right)}, V_{\mathrm{c}} > 0. \tag{8}$$

When V_c is the negative blocking voltage (for an n-type FET, as in this work), an incorrect result will be obtained when the total current becomes negative when reading the target memristor conductivity, viz.

$$-\frac{|V_{\mathrm{c}}|}{R_{\mathrm{gd}}} N^2 + \frac{V_{\mathrm{r}}}{R_{\mathrm{off}}} < 0, \tag{9}$$

and therefore

$$N^{(\mathrm{leak})}_{\max} \approx \sqrt{\frac{R_{\mathrm{gd}}}{R_{\mathrm{off}}} \frac{V_{\mathrm{r}}}{|V_{\mathrm{c}}|}}, V_{\mathrm{c}} > 0. \tag{10}$$

Considering that the factor $(R_{\mathrm{off}}/(SR_{\mathrm{on}}) - 1)$ is on the order of magnitude of 1 (for $R_{\mathrm{off}}/R_{\mathrm{on}} \approx 100$), Eq. (4) can be simplified and expressions (8) and (10) combined to obtain

$$N^{(\mathrm{sneak})}_{\max} \sim \frac{R_{\mathrm{FET,off}}}{R_{\mathrm{off}}}, \tag{11a}$$

$$N^{(\mathrm{leak})}_{\max} \sim \sqrt{\frac{R_{\mathrm{gd}}}{R_{\mathrm{off}}} \frac{V_{\mathrm{r}}}{|V_{\mathrm{c}}|}}. \tag{11b}$$

According to Eq. (11b), the biggest allowable size of such a crossbar containing nanocomposite memristors could be ~ 20,000 (for $V_r = 1$ V and $V_c = -3.3$ V), which is much smaller than the size of 10^6 given by Eq. (6), from the point of view of the proximity of the leakage and sneak current values. On the other hand, the use of high-k dielectric transistors could improve this situation, as this would allow a decrease of the

leakage current by several orders of magnitude, thus increasing the maximum size to 200,000 or even greater.

8 Discussion

Before designing a crossbar with the 1T1M architecture, it should be checked whether the desired crossbar size is less than the least of the values given by Eq. (11) [or, more precisely, by (4), (8), and (10)], according to the characteristics of the memristive devices and transistors used. Generally, the size defined by (11a) is much less than that given by (11b), so the sneak current is still the major problem, as for crossbars without transistors or selector devices.

Partial solutions of the sneak current problem, according to formula (4), may be: (i) increasing the ratio R_{off}/R_{on} of the memristive devices used, or (ii) using a control FET with a high resistance $R_{FET,off}$ in its closed state.

It is important to note that the derived formulae are valid when $R_{on} \gg R_{FET,on} + r$ (the latter being the series resistance related to the CMOS metal lines and electrodes). Otherwise, the physical characteristics of the crossbar line resistance will affect the ratio calculated based on the output currents. Nevertheless, formulae (4) and (8) remain valid if R_{on} is replaced by the sum $(R_{on} + R_{FET,on} + r)$. Also, it is necessary to apply linear corrections for the wire resistances when measuring conductivities in different columns of the crossbar.

To reduce the destructive effect of the leakage currents through the FET gates, one should use transistors whose gate dielectric exhibits good insulating properties. Also, it is possible, as in this work, to choose V_c equal to 0 V during the reading process (only for normally closed transistors, i.e., with an induced channel), so that $N_{max}^{(leak)}$ diverges to infinity, according to Eq. (11b).

The most destructive (in terms of their amplitude) are the transistor gate discharge currents in the control lines of a 1T1M crossbar. Their effect can be eliminated either by waiting until the end of the relaxation phenomena after switching the control lines, or by using a simple discharge circuit in the form of a transimpedance amplifier-based virtual ground.

Another issue that should be considered is the geometrical scaling of the crossbar. If the length and width of a transistor channel from the source to drain are designated as l and w, respectively, then

$$R_{FET,off} \propto \frac{l}{w}, \tag{12a}$$

$$R_{off} \propto \frac{l}{wl}. \tag{12b}$$

The last expression approximately applies because the memristive device is generally laid above the drain and corresponds to its size. It can be seen that R_{off} depends quadratically on a linear scaling factor, whereas $R_{FET,off}$ almost does not depend on the scaling. Thus, the ratio $R_{FET,off}/R_{off} \propto l^2$ decreases quadratically with downscaling of the size of the elements. This is a serious issue because of the reduction of the maximum allowable crossbar size due to the increase of the sneak currents according to Eq. (11a).

Another fundamental solution to the problem of sneak currents is to use a special scheme for reading the 1T1M crossbar, compatible with that suggested for eliminating the discharge currents. One can apply V_r to a chosen word line and 0 V to a chosen bit line, which intersect at the target memristor, while connecting all other word and bit lines to the (virtual) ground (0 V). At the same time, only the target control line should be open, while all the others are closed (Fig. 5). This, in principle, should lead to the absence or a reduction by orders of magnitude of the sneak current values in the target bit line. A simple evaluation based on Kirchhoff's equations shows that the sneak current in the worst case can be expressed as

$$I_{sneak} \approx \frac{r^2}{R_{FET,off}\left(R_{FET,on} + R_{on}\right)} \frac{V_r}{R_{FET,off}} N^2, \tag{13}$$

where r is the resistance of one contact bus and the series electrodes. It is assumed that $r << R_{FET,off}/N$. Repeating the considerations described above yields

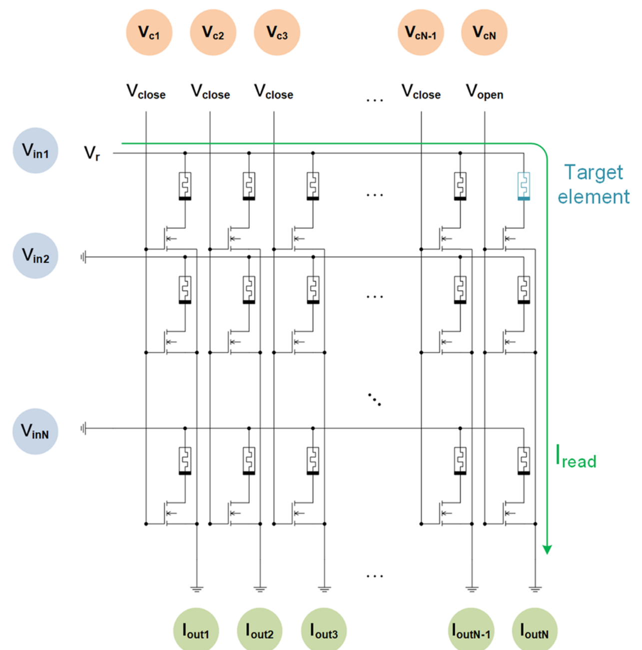

Fig. 5 The proposed reading scheme where all the unselected bit and word lines are (virtually) grounded

$$N_{max}^{(leak)} \sim \sqrt{\frac{R_{FET,on} + R_{on}}{R_{off}} \frac{R_{FET,off}}{r}} \tag{14}$$

[cf. formula (11a)]. Moreover, this approach simultaneously diminishes the problems with the discharge and leakage currents, as it allows them to drain into the (virtual) ground connected to the bit lines.

Note that, if such a scheme is not justified in practice due to the additional hardware cost of grounding the unused crossbar word lines, a simple scheme of virtually grounding only the nontarget columns can be chosen. In this case, the estimates for the amplitude of the sneak current and the allowable crossbar size are

$$I_{sneak} \approx \frac{r}{R_{FET,off}} \frac{V_r}{R_{FET,off}} N^2, \tag{15}$$

$$N_{max}^{(sneak)} \sim \frac{R_{FET,off}}{\sqrt{rR_{FET,off}}}. \tag{16}$$

This scheme yields a maximum 1T1M crossbar size that is $\sqrt{(R_{on} + R_{FET,on})/r}$ times smaller than that given by Eq. (14).

9 Conclusions

The results of this study reveal that, in a large memristive crossbar built with the 1T1M architecture, the sneak and discharge currents and even the leakage current through the transistor gate dielectric must be accounted for to enable correct estimation of the crosspoint memristor resistances. Simple evaluations based on Kirchhoff's equations give the maximum size of a crossbar corresponding to the allowable quality of its operation in neuromorphic calculations. It is demonstrated that the stationary sneak and dynamical discharge currents have the most deteriorating effect on the performance of the crossbar.

Nevertheless, all these negative effects can be overcome by using a simple proposed scheme for switching and measurement, consisting of grounding all the nontarget word and bit lines. It is also worth noting that such virtual grounding should be realized by using transimpedance amplifiers, so as to not significantly reduce the input impedance of the circuit with increasing crossbar size.

This scheme of operation enables 1T1M crossbars with dimensions of up to $N \sim \sqrt{(R_{on} + R_{FET,on})/R_{off} R_{FET,off}/r}$, where R_{on} and

R_{off} are the resistances of the memristor in its low- and high-resistive states, $R_{FET,off}$ and $R_{FET,on}$ are the resistances of a control FET channel in its closed and open states, and r is the resistance of the bus electrode or some appropriate small compliance resistance connected to it in series. This upper value of N can reach as much as 10^8 or even more, depending on the compliance resistance, memristors, and FETs chosen. At the same time, taking into account a plausible geometrical size of a 1T1M crossbar (up to $\sim$ 10cm) and a scaling dependence of type (12b) for the resistances r, R_{off}, and R_{on}, the maximum allowable dimensions of a 1T1M crossbar can be estimated as $N \sim 10^6$.

In this case, the reading or writing times and, consequently, the overall performance are limited mainly by the relaxation time constant rC, with C designating the transistor gate capacity. By choosing a sufficiently small r, it is possible to improve the crossbar performance within certain limits.

It is believed that the results of this study will support the development of high-speed and reliable analog and multistate neuromorphic systems based on large memristive crossbars for different prospective applications, from neuromorphic computation to brain–computer interfaces and neuroprostheses.

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