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# An efficient design of edge-triggered synchronous memory element using quantum dot cellular automata with optimized energy dissipation

**Mukesh Patidar**[1,2] · **Namit Gupta**[1,2]

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**Abstract**
Quantum dot cellular automata (QCA) constitute an emergent nanoscale-based digital nanoelectronics technology with comprehensive applications in nanocomputing based on the small nanometer size of such circuits and their ultralow power consumption, fast operation, and high clock frequency in comparison with transistor-based complementary metal–oxide–semiconductor (CMOS) technologies. A novel design for edge-triggered synchronous J-K flip-flop (FF) and D (data or delay) flip-flop memory elements based on QCA cells with quantum wires is presented herein. The proposed design has fewer QCA cells and lower latency and area and uses the coplanar crossover method to overcome the complexity of multilayer quantum wire crossing. The design is analyzed to determine the average output polarization (AOP) of the edge-triggered synchronous D-FF and JK-FF at different temperature levels and the optimized energy dissipation. The layout design and computational simulation of the circuit are carried out using QCADesigner V. 2.0.3 software, while the energy dissipation is analyzed using the QCADesigner-E V. 2.2 tool.

**Keywords** Quantum dot cellular automata (QCA) · Nanoelectronics · Quantum dots · Quantum wire · Average output polarization (AOP) · Energy dissipation

## 1 Introduction

Moore's law [1], predicting that the number of transistors per square inch of integrated circuit (IC) or microchip doubles about every 2 years for traditional transistor-based semiconductor technologies such as CMOS and very large-scale integration (VLSI), has been found to be true [1, 2]. However, it now faces many challenges such as increased power consumption [3], thermal dissipation [4], and high lithography costs and leakage current [3, 4]. To solve these problems with CMOS technology, the use of quantum dot cellular automata as an emerging nanoelectronics-based technology was suggested by Lent [5] and demonstrated experimentally in 1997. The major developments in memory elements enabled by QCA technology can play an important role in nanocommunication networks based on devices such as random-access memory (RAM) [6], crossbar schedulers for system-on-chip networks [7], and modern secured static RAM (SRAM)-based true random number generator (TRNG) technology [8]. These devices have a great impact on nanocommunication and secured systems. The molecular fabrication process for QCA supports clocking frequencies in the THz range at room temperature [9]. This work considers synchronous sequential circuits (SSCs) consisting of a combinational circuit and memory element. The memory element is connected through a feedback path, enabling such devices to store binary information. The main contributions of this work are as follows:

1. The proposal of a new, single-layer QCA-based synchronous memory elements with D-type flip-flop (PDT-I, PDT-II) and JK-type flip-flop (PJKT) designs with a reduced number of QCA cells, design area, and area

✉ Mukesh Patidar
mukesh.omppatidar@gmail.com

Namit Gupta
namitg@hotmail.com

[1] Department of Electronics Engineering, Shri Vaishanv Institute of Technology and Science, Indore, India

[2] Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore, Madhya Pradesh 453331, India

utilization factor (AUF) as calculated using the QCADesign bistable simulation engine.
2. The analysis of the energy dissipation of the PDT-I, PDT-II, and PJKT flip-flops using the novel layout design tool QCADesigner-E in the Coherence Vector (w/Energy) simulation engine.
3. A reduction of the latency of the proposed edge-triggered synchronous sequential circuits based on coplanar crossover quantum cells using the QCADesigner tool, considering a cell size of 18 nm × 18 nm.
4. The calculation of the average output polarization (AOP) of the proposed sequential circuits and graphical plots of temperature versus polarization.

## 2 Computational procedures

The architecture for the quantum dot cellular automata was designed using the coplanar crossover (single-layer) method with a majority gate (MG), inverter, and quantum wires in a regular (90°) and rotated (45°) QCA cell.

### 2.1 QCA cell

The fundamental unit of a QCA device is the QCA cell [10, 11], considered here to have the standard size of 18 nm × 18 nm. Each QCA cell contains four quantum dots with diameter of 5 nm, placed on the four corners of a square [11]. Two extra mobile electrons in the square QCA cell (SQC) can tunnel freely between the quantum dots under the effect of columbic repulsion. In this technology, in the null (polarization = 0) state, the electrons are not settled, while other states corresponding to digital logic bistate [12] of zeros (polarizations $P = -1$) and ones (polarization $P = +1$) [13], based on the electron pairs as shown in Fig. 1 [10]. The electrons experience the maximum repulsion in the horizontal/vertical position of the quantum dots and the minimum diagonally, as shown in Fig. 2 [2]. The QCA cell polarization ($P$) can be calculated using Eq. (1) [14], where $\rho_i$ represents the charge density at the $i$th point [14, 15]:

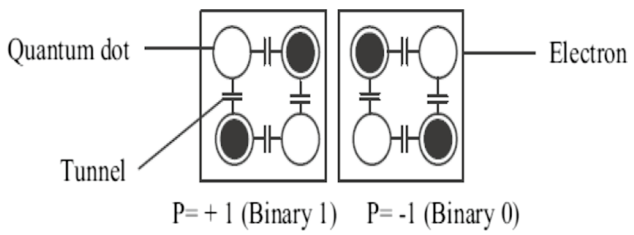


**Fig. 1** The cell polarizations $P = +1$ and $P = -1$ in the quantum dot cellular automata

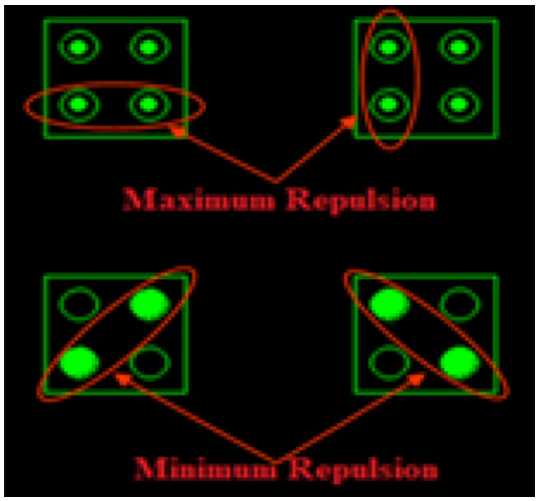


**Fig. 2** The repelled electron positions in a QCA cell

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)}. \quad (1)$$

### 2.2 QCA wires

The QCA wires are used to transmit information from the origin to the destination in the forward direction based on the electronic interaction between neighboring QCA cells [16], with either a linear 90° arrangement of straight wires, or bent as shown in Fig. 3.

### 2.3 The majority voter

The majority voter (MV) lies at the heart of QCA technology. The three-input MV logic gate is presented in Fig. 4a. The majority gate design requires a minimum of five quantum cells, viz. three input cells $A$, $B$, and $C$, a processing cell in the

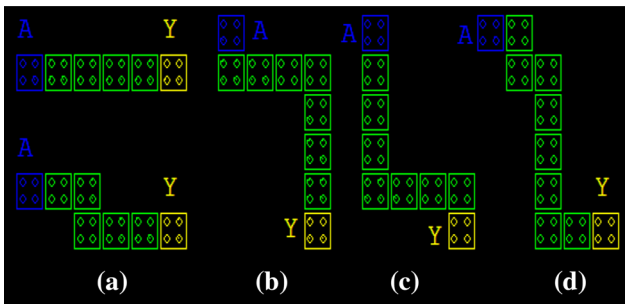


**Fig. 3** **a** Straight and **b**–**d** bent QCA wires, where $A$ is the input and $Y$ is the output

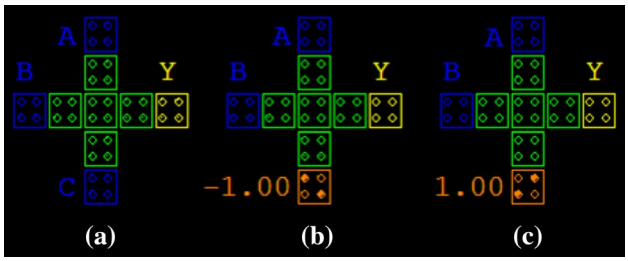


**Fig. 4** The standard QCa gates: **a** the majority voter, **b** the two-input AND gate, and **C** the two-input OR gate

center, and an output cell ($Y$). The mathematical function for the MG is shown in Eq. (2) [17]:

$$\text{Majority logic gate } Y(A,B,C) = A \cdot B + B \cdot C + A \cdot C. \quad (2)$$

Gates achieving the other logical operations AND and OR can be obtained from the majority gate by fixing any one of the three inputs to a logical value of 0 for ($P = -1$) or 1 for ($P = +1$) [17, 18], as shown in Fig. 4b and c, respectively [19].

The function of the AND and OR logic gate is presented in Eqs. (3) and (4). The truth tables of the MG, AND, and OR logical functions using three inputs are presented in Table 1.

$$\text{AND logic gate } Y(A,B,0) = AB, \quad (3)$$

$$\text{OR logic gate } Y(A,B,1) = A + B. \quad (4)$$

**Table 1** The truth tables of the majority gate, AND gate, and OR gate

| Logical function | Inputs | | | Output |
|---|---|---|---|---|
| | $A$ | $B$ | $C$ | $Y$ |
| Majority gate | 0 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 0 |
| | 0 | 1 | 0 | 0 |
| | 0 | 1 | 1 | 1 |
| | 1 | 0 | 0 | 0 |
| | 1 | 0 | 1 | 1 |
| | 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 | 1 |
| The two-input logical AND gate with one fixed input ($A = -1$) | 0 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 0 |
| | 0 | 1 | 0 | 0 |
| | 0 | 1 | 1 | 1 |
| The two-input logical OR gate with one fixed input ($A = +1$) | 1 | 0 | 0 | 0 |
| | 1 | 0 | 1 | 1 |
| | 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 | 1 |

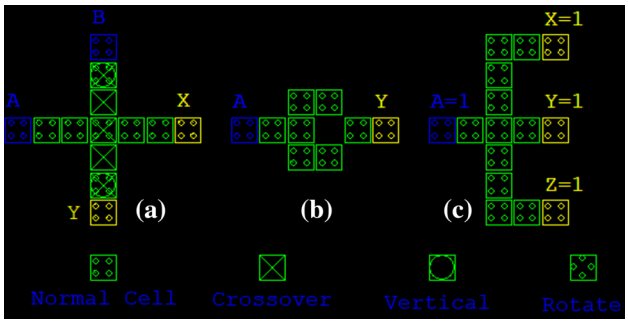


**Fig. 5** Interconnection elements for QCA circuits: **a** the crossover design, **b** an inverter, and **c** a fan-out

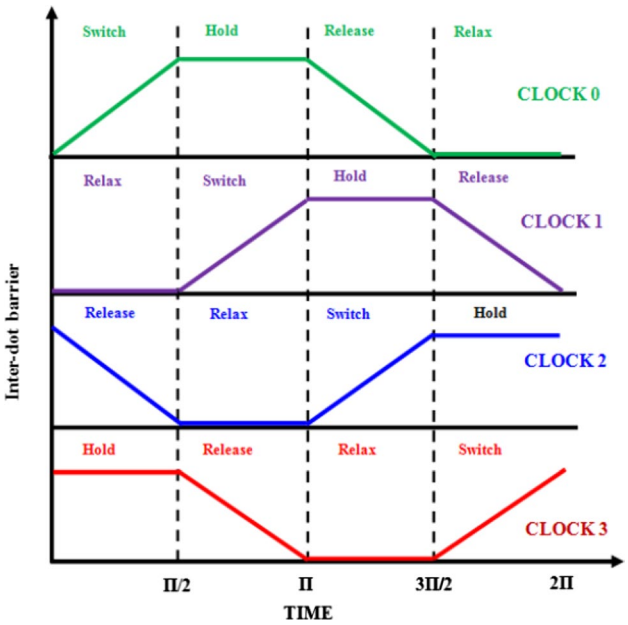


**Fig. 6** QCA synchronization via the four phases of the clock (CLK)

## 2.4 Crossover and the QCA inverter

To reduce the complexity as well as quantum cost of QCA design layouts, crossover of QCA wires can be applied using one of two methods, viz. coplanar crossover for a single layer or multilayer crossover for designs with more than one layer. The multilayer coplanar design is shown in Fig. 5a, using different interconnected quantum cells such as the normal cell, crossover cells, vertical (via), and rotated cells. Meanwhile, the basic single-layer designs for a QCA inverter and fan-out circuit are shown in Fig. 5b and c, respectively.

## 2.5 The QCA clocking mechanism

The clock is one of the important features used to control CMOS circuits. Similarly, a QCA circuit is also controlled

**Table 2** The standard simulation design parameters used in QCADesigner (QD) and QCADesigner-E (QD-E)

| Parameter | Description | Standard value for tool | |
|---|---|---|---|
| | | QCADesigner (version 2.0.3) | QCADesigner-E (version 2.2) |
| Cell area | Dimensions (length × width) of cell | 18 nm × 18 nm | |
| Quantum dot | The size of each dot in the cell | 5 nm | |
| Layer separation | Multilayer crossing | 11.5 nm | |
| Cell distance | The distance between two quantum cells | 20 nm | |
| $\epsilon_r$ | The relaxation time in seconds (s) | 1.0e−15 s | |
| $\gamma_H$ (Clock-Max) | The saturation energy of the CLK signal in joules (J) | 9.8e−22 J | |
| $\gamma_L$ (Clock-Min) | | 3.8e−23 J | |
| $\epsilon_r$ | The relative permittivity | 12.9 | |
| Temp | The operating temperature in kelvin (K) | 1.00 K | |
| $T_\gamma$ | The CLK signal period | – | 4.0e−12 s |
| $\gamma_{slope}$ | The fall and rise time slope of the CLK | – | 1.0e−12 s |
| $\gamma_{Shape}$ | The shape of the CLK signal slopes | – | 1.0e−12 s |
| $T_{in}$ | The period of the input signals in seconds (s) | – | 4.0e−12 s |
| $T_{sim}$ | The total time of the simulation for Coherent Vector (CV) | 7.0e−11 s (CV) | 7.0e−11 s (CV), 5.0e−11 s (CV for energy) |
| $T_{step}$ | The time interval of each iteration step | 1.0e–16 s | |
| The radius of effect | The effective radius of the QD cell | 80.00 nm (coherent vector)<br>65.00 nm (bistable approximation) | |
| Simulation engine applied | Layout design simulation engine | Coherent vector and bistable approximation | Coherent vector, bistable approximation, and CV (w/ Energy) |

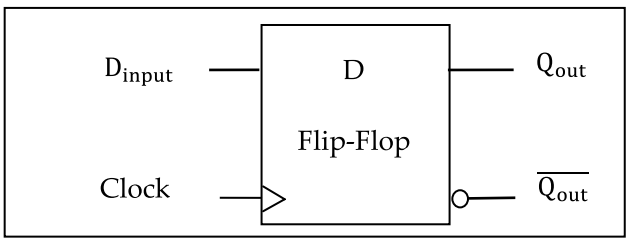


**Fig. 7** The symbols for the D-type flip-flop

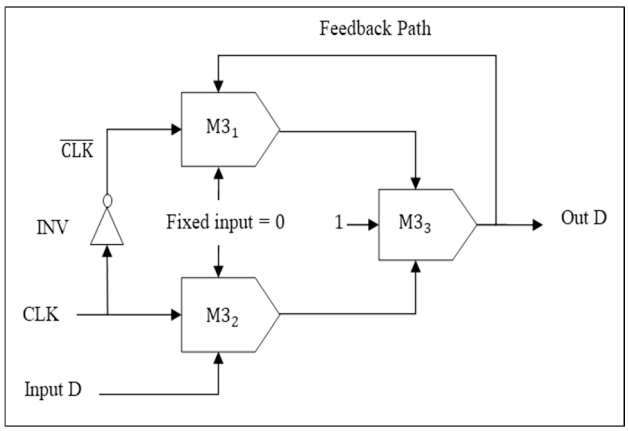


**Fig. 8** A schematic diagram of the D-type flip-flop

by a clock [12], which determines the tunneling barriers between the quantum dots and thus the transfer of electrons [2]. Ultralow-latency computer networks based on QCA circuits can play an important role in enabling resource sharing by facilitating communication between different users [6].

The clocking mechanism is divided into four different $\pi/2$ phases [1], viz. clock-0: switch, clock-1: hold, clock-2: release, and clock-3: relax [1]. In a QCA design, information propagates in the forward direction [5] from one CLK zone to another, viz. from zone 1 to 2, 2 to 3, 3 to 4, then 4–1, or in the opposite direction if a feedback path is available, with the clocking scheme shown in Fig. 6 [17]. In the JK and data

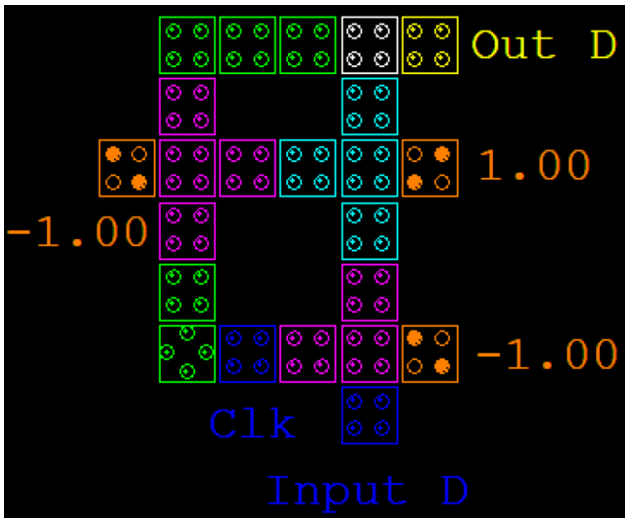


**Fig. 9** The first proposed QCA layout design (PDT-I) for the edge-triggered synchronous sequential D-type FF

flip-flops, the clock (CLK) pulse is used for synchronization and also acts as an additional control input.

## 3 A review of related work

QCA-based nanocommunication is currently a growing field of research, although very few such studies have been reported, mainly being in the field of reversible computing and networking [20]. QCA represents a novel nanotechnology paradigm and a new alternative to transistor-based technologies [21, 22] due to the small size and ultralow power consumption of such devices offering different nanocomputational logical functions [1]. Over the last two decades, QCA devices using quantum cells have had a great impact on circuit design, as well as the development of devices for use in digital circuits. Several designs have been proposed for JK flip-flops to enhance their performance by using a single layer with a bistable simulation engine [16]. Multilayer

**Table 3** The excitation table of the D flip-flop

| Trigger | Input | Output | | | | Description |
|---|---|---|---|---|---|---|
| Clock (CLK) | $D$ | Present state | | Next state | | |
| Low = 0 | × | $Q$ | $\bar{Q}$ | $Q$ | $\bar{Q}$ | Memory no charge |
| Apply clock high = 1 | 0 | 0 | 1 | 0 | 1 | Reset |
| | 0 | 1 | 0 | 0 | 1 | |
| | 1 | 0 | 1 | 1 | 0 | Set |
| | | 1 | 0 | 1 | 0 | |

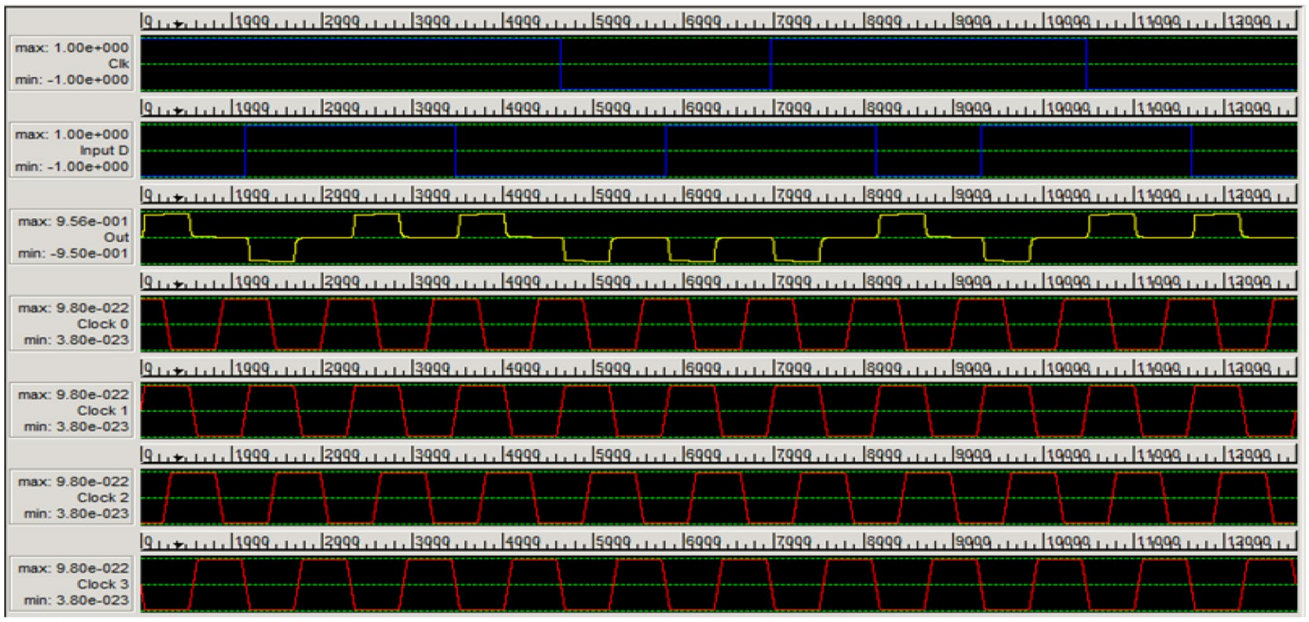


**Fig. 10** The simulation results for the first proposed D-type flip-flop (PDT-I)

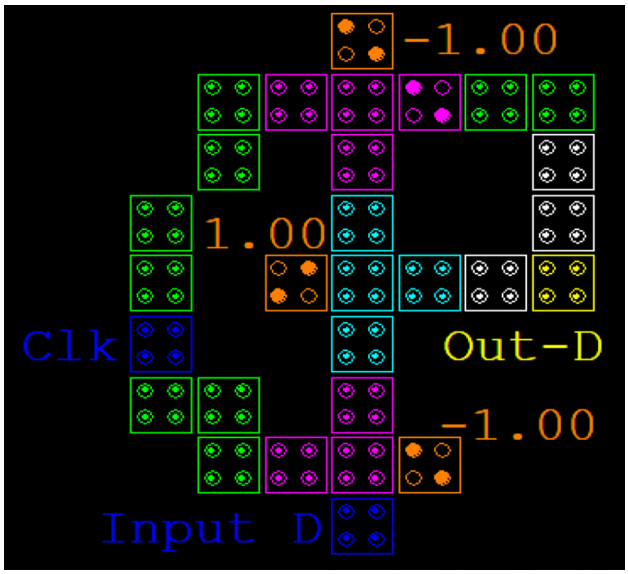


**Fig. 11** The second proposed QCA layout design for the edge-triggered synchronous sequential D-type flip-flop (PDT-II)

D and JK flip-flop designs have also been presented [23, 22], as well as synchronous counters and a level-sensitive D flip-flop design [13], and single-layer JK flip-flop and synchronous sequential counter designs [24]. Three different D-type flip-flop and multilayer QCA serial in serial out (SISO) shift register designs were presented by Divshali et al. [14].

## 4 The proposed design and its specifications

The flip-flop (FF) is an electronic circuit that is widely used in memory devices for digital counters, in telecommunications for information exchange, in spacecraft for many processes, and for the storage of logical data. QCA nanocommunication technology has now developed sufficiently to build a whole variety of types of memory. In QCA-based designs, motion through the cells is required for the memory function; i.e., the memory state must be successively moved through a set of cells [24]. Such synchronous sequential circuits (SSCs) that use a clock pulse at the inputs of the memory elements are called clocked sequential circuits. The FF controls the functionality of the integrated circuit. In this paper proposed Three different layout designs (PDT-I, PDT-II, and PJKT) using a QCA majority gate, 45° rotated cell, and crossover wires are proposed herein with the help of the standard simulation layout design tool QCADesigner (QD, version 2.0.3G) by Schulhof et al. and its modified designer tool QCADesigner-E version 2.2 by Frank Sill Torres et al. The different parameter values used in the tool are presented in Table 2 [25].

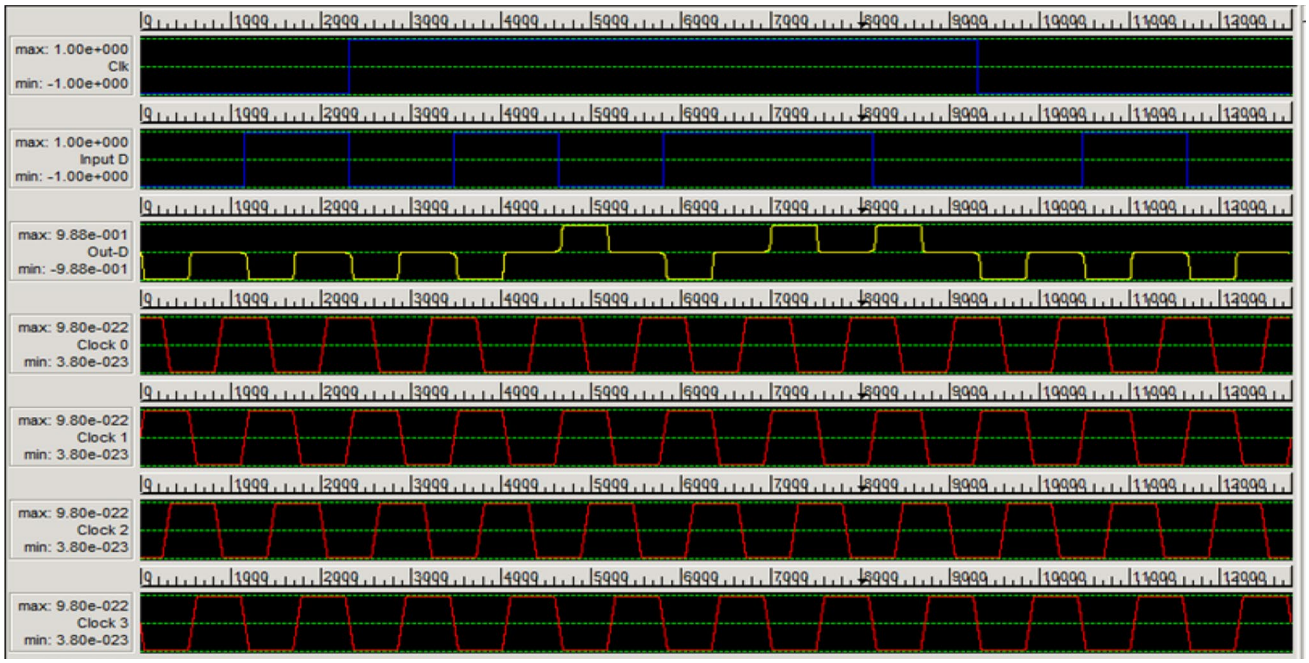


**Fig. 12** The simulation results for the second proposed D-type flip-flop (PDT-II)

**Table 4** A comparison of the results obtained for different D-type flip-flop designs

| Design | Cell count | Total design area ($\mu m^2$) | Latency | Cell area ($\mu m^2$) | | | |
|---|---|---|---|---|---|---|---|
| *Proposed designs of D-type flip-flop* | | | | | Single-layer design | Size of quantum cell: 18 nm× 18 nm | Maximum iterations per sample: 100 |
| First proposed design (PDT-I) | 23 | 0.03 | 1.00 | 0.075 | | | |
| Second proposed design (PDT-II) | 29 | 0.03 | 1.00 | 0.094 | | | |
| *Existing designs of D flip-flops* | | | | | | | |
| Chakrabarty [18] | 43 | 0.042 | 1.25 | 0.139 | | | |
| Rezaei [26] | 46 | 0.05 | 1.25 | 0.149 | | | |
| Purkayastha [27] | 48 | 0.03 | 0.75 | 0.156 | | | |
| Goswami [10] | 48 | 0.06 | 4.00 | 0.156 | | | |
| Abutaleb [13] | 74 | 0.10 | 1.50 | 0.240 | | | |

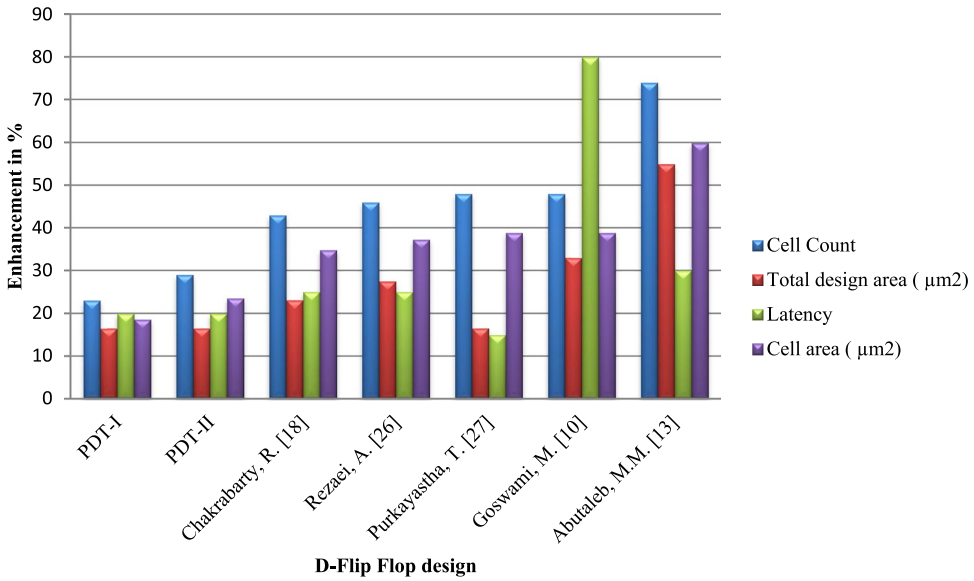


**Fig. 13** A comparison of the results obtained for PDT-I and PDT-II versus existing designs

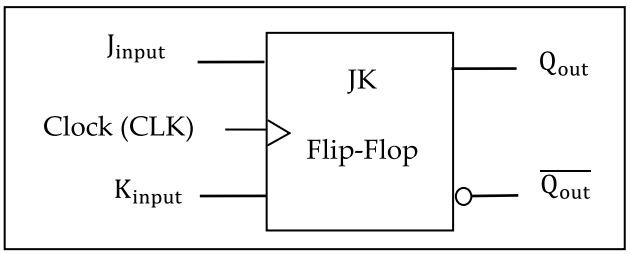


**Fig. 14** The symbols for the JK flip-flop

## 4.1 The proposed QCA synchronous D-type flip-flops

The implementation and optimization of the first and second edge-triggered synchronous sequential flip-flop designs (PDT-I and PDT-II) proposed herein using QCA technology are described in this section. The layout is described in terms of the quantum cells and the total design area in $\mu m^2$, consider a maximum number of iterations of 100 per sample, a relaxation time of 1.0e−15 s, and a relative permittivity of 12.9 (corresponding to GaAs and AlGaAs). The first proposed layout (PDT-I) is a robust and simple design with only three, three-input majority voters and one 45° rotated cell for the QCA inverter, and connecting wires formed using the coplanar crossover method. The symbols for the D-FF are shown in Fig. 7, the characteristic mathematical equation of the D flip-flop in Eqs. (5) and (6), and a schematic diagram of the proposed PDT-I in Fig. 8.

**Table 5** The excitation table of the JK flip-flop

| Trigger | Inputs | | Output | | | | Description |
|---|---|---|---|---|---|---|---|
| | | | Present | | Next | | |
| | $J$ | $K$ | $Q$ | $Q'$ | $Q$ | $Q'$ | |
| No CLK | × | × | – | | – | | Latched |
| Apply clock high = 1 | 0 | 0 | 0 | 1 | 0 | 1 | No change |
| | | | 1 | 0 | 1 | 0 | |
| | 0 | 1 | 0 | 1 | 0 | 1 | Reset |
| | | | 1 | 0 | 0 | 1 | |
| | 1 | 0 | 0 | 1 | 1 | 0 | Set |
| | | | 1 | 0 | 1 | 0 | |
| | 1 | 1 | 0 | 1 | 1 | 0 | Toggle |
| | | | 1 | 0 | 0 | 1 | |

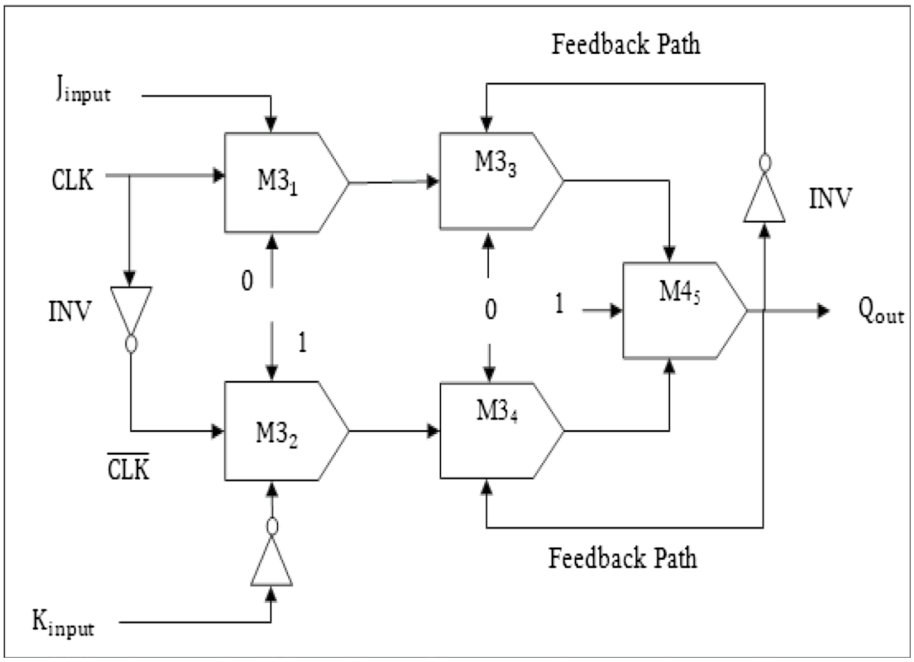


**Fig. 15** A schematic diagram of the JK-type flip-flop

For PDT-I, the number of QCA cells is calculated as 23, the total circuit design area as 0.03 μm$^2$, the cell area as 0.075, the percentage area utilization factor (AUF) as 24.84% using Eq. (7), the quantum cost of the overall design area as 0.03 μm$^2$ using Eq. (8), and the cell density as 766.67 cell/μm$^2$. The layout design of the simulated QCA PDT-I is shown in Fig. 9, using three majority voters and one inverter; the active trigger signal and output results are confirmed by the excitation table presented in Table 3. In the excitation table of the D flip-flop, the CLK signal is activated by high = 1, and the input data signal 0 or 1 is stored in the output state ($Q$); when the clock signal is low = 0, it is deactivated and the output ($Q$) state will never be affected by any of the inputs. The simulation results of PDT-I are shown in Fig. 10, with a maximum output polarization of 9.56e−01 and minimum output polarization of −9.50e−01, with the output result calculated at clock-3.

$$Q(t+1)_{\text{next}} = D\bar{Q} + DQ \tag{5}$$

$$Q(t+1)_{\text{next}} = D \tag{6}$$

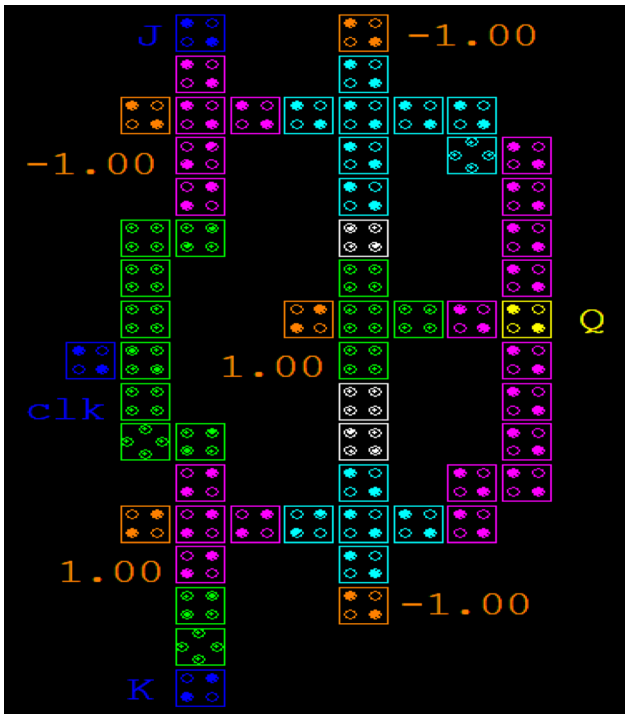


**Fig. 16** The QCA layout design for the edge-triggered synchronous sequential JK-type flip-flop (PJKT)

$$\%\text{Area utilization factor (AUF)} = \frac{\text{Net cell Area } (\mu\text{m}^2)}{\text{Total Area}(\mu\text{m}^2)} \times 100 \tag{7}$$

$$\text{Quantum cost} = \text{Total design area } (\mu\text{m}^2) \times (\text{Latenct})^2 \tag{8}$$

A schematic layout of the architecture of the second proposed design (PDT-II) is shown in Fig. 11, consisting of three majority gates using two AND and one OR logic plus one inverter, which is beneficial for the design of digital memory-based sequential circuits. This layout architecture design utilizes 29 QCA cells, with a total design area (length × width) of 0.03 μm$^2$, cell area of 0.094 μm$^2$, AUF of 31.32%, and cell density of 966.67 cell/μm$^2$. The operational functionality of the layout is verified by the excitation table presented in Table 3. PDF-II was simulated using QCADesigner 2.0.3, and the generated output results are shown in Fig. 12. Table 4 compares the results obtained for PDT-I and PDT-II with previous QCA designs in terms of the cell count, total design area, latency, and cell area in μm$^2$ (Fig. 13).

### 4.2 The proposed edge-triggered synchronous QCA-PJKT design

The novel design proposed for the JK flip-flop with a QCA architecture for memory storage offers an enhanced reduction in the number of quantum cells, design area, and delay. The edge-triggered JK-FF is a refinement of the SR-FF to solve the indeterminate state problem. In the JK flip-flop, when both inputs are zero ($J=K=0$), the output in the next state $Q(t+1)$ is the same as its previous value, being reset (R) when $J=0$, $K=1$ and set (S) when $J=1$, $K=0$. The symbol of the JK flip-flop is shown in Fig. 14, the excitation table is presented in Table 5, while the characteristic mathematical equation of the JK flip-flop is Eq. (9).

$$Q(t+1)_{\text{next}} = J\bar{Q} + \bar{K}Q. \tag{9}$$

A schematic diagram of the proposed edge-triggered synchronous JK FF is shown in Fig. 15, while the layout simulated in the QCADesigner-E tool is shown in Fig. 16, incorporating three 45° rotated QCA cells in place of the inverter, five three-input majority gates (MGs), three inputs J, K, and the Clock, and one output-$Q$ in a single-layer coplanar design.

This design has a cell count of 59, the total design area has selection extents of (131.00, 151.00) [178.00 × 338.72] = 60,293.02 nm$^2$ = 0.06 μm$^2$, the cell area is 0.019 μm$^2$, and the utilized area fraction is 31.86%. The JK edge-triggered flip-flop with this layout design passes through four clocks in one zone, and its latency is counted as one clock cycle. The delay or latency can be calculated by using Eq. (10). Information must pass from the input to the output in a number of clock zones (CZ) as described by Frank Sill Torres [25]. The simulation results for the PJKT design are shown in Fig. 17 and compared with those obtained for existing JK flip-flop designs in Table 6 (Fig. 18).

$$\text{Delay or latency} = \frac{1}{4 \times f_{\text{clk}}} \times \text{delay (clock zones)}. \tag{10}$$

## 5 The energy calculation for the proposed design

The power dissipated from a quantum cell depends on the rate of change of the tunneling energy and the clock cycle [31]. The energy consumption is calculated using QCADesigner-E with the coherence vector (w/Energy) simulation engine, considering the parameter values presented in Table 2 [25]. The total power dissipated by any nanocommunication-based quantum

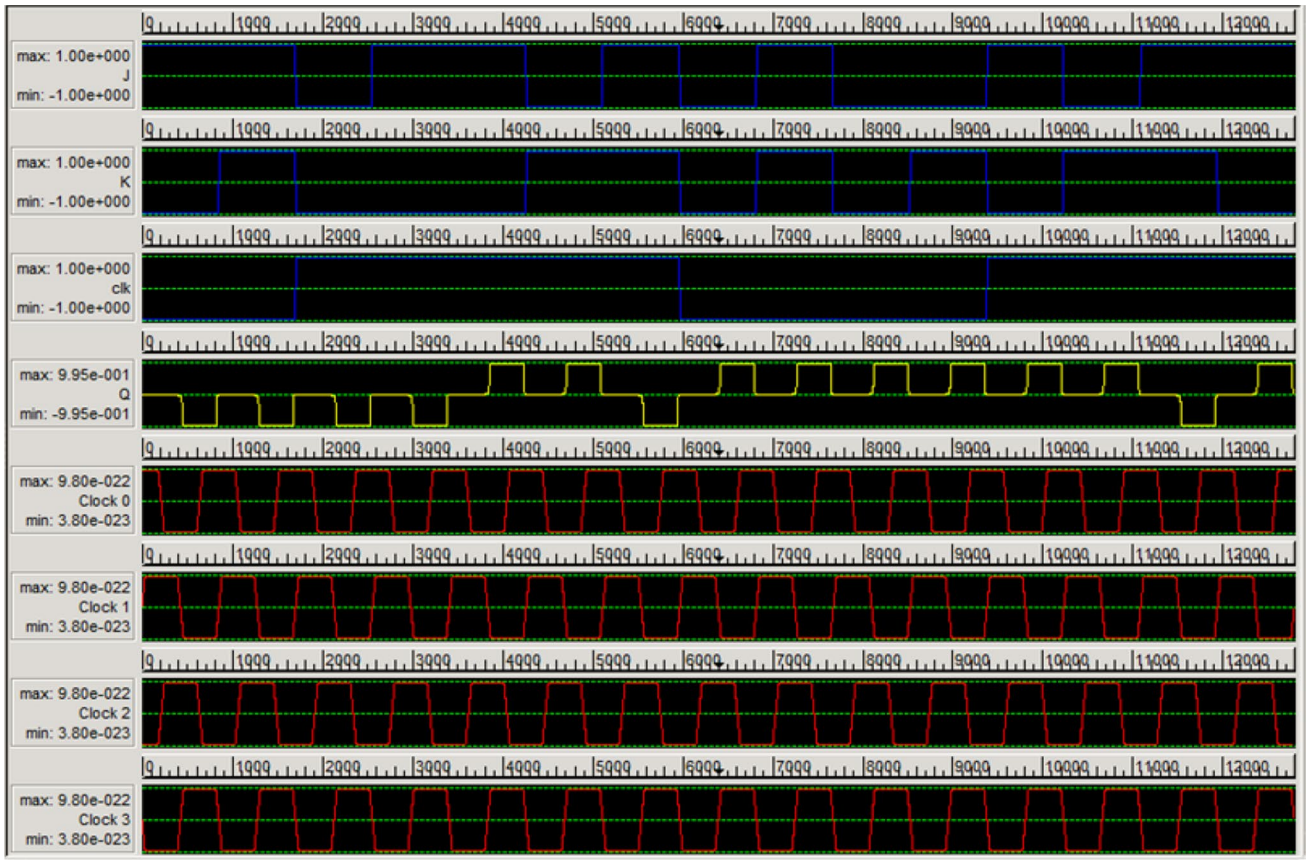


**Fig. 17** The simulation results for the proposed JK-type flip-flop (PJKT)

**Table 6** A comparison of the results obtained for the PJKT flip-flop versus existing JK-FF designs

| JK flip-flop design | Cell count | Total design area ($\mu m^2$) | Latency | Cell area ($\mu m^2$) | | | |
|---|---|---|---|---|---|---|---|
| *The proposed JK-type flip-flop design* | | | | | Single-layer design | Size of quantum cell: 18nm × 18 nm | Maximum iterations per sample: 100 |
| Proposed design (PJKT) | 59 | 0.06 | 1.00 | 0.019 | | | |
| *Existing JK flip-flop designs* | | | | | | | |
| Chakrabarty [18] | 78 | 0.07 | 1.00 | 0.025 | | | |
| Angizi [28] | 78 | 0.12 | 1.50 | 0.025 | | | |
| Lim [29] | 80 | 0.16 | 1.25 | 0.026 | | | |
| Zhang [30] | 132 | 0.06 | 1.00 | 0.043 | | | |

dot circuit depends on the number of majority gates (MGs) and inverters [32]. Energy dissipation occurs due to loss of information. The heat energy dissipated by the loss of a single bit of information can be expressed by Eq. (11), where $K_B$ is Boltzmann's constant ($K_B = 1.3807 \times 10^{-23}$ J $K^{-1}$) and $T$ is the absolute temperature [33]:

$$\text{Energy dissipated} = K_B T \times \log_e 2 \text{ J}. \tag{11}$$

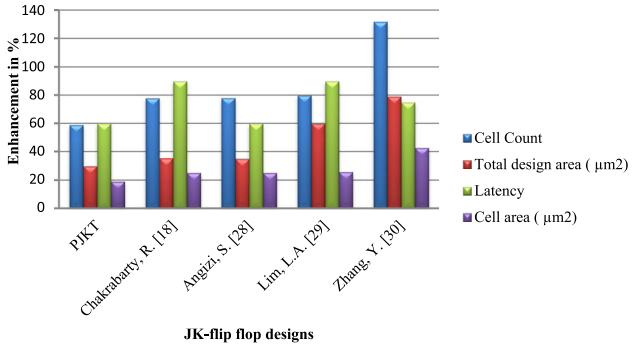


**Fig. 18** A comparison of the results obtained for the proposed JK-type flip-flop versus existing designs

Tables 7, 8, and 9 present the energy consumption calculated for the PDT-I, PDT-II, and PJKT design, respectively, where *E*_bath_total ($E_{btx}$) is the sum of all the energy transferred to the bath by all the quantum cells ($E_{bt1}$, $E_{bt2}$, $E_{bt3}$,…..) in each clock, *E*_clk_total ($E_{ctx}$) is the total energy transferred ($E_{ct1}$, $E_{ct2}$, $E_{ct3}$,….) between the quantum cells and the clock split by each clock, and in the $E_{ctx}$ column in Tables 7, 8, and 9 a positive sign indicates the receipt of clock energy while a negative sign indicates energy transfer, and *E*_Error_total is the summation of each error ($E_{et1}$, $E_{et2}$, $E_{et3}$,….) of the cell for every clock. For the whole clock cycle, the sum of the total energy movement by the QCA cell is zero, as represented in Eq. (12) [34].

$$\text{Error} = E_{\text{bath}} - \left(E_{\text{clock}} + E_{\text{IO}}\right). \tag{12}$$

Sum_bath $S_b$ (Er: $S_{be}$) is the total energy dissipation, where $S_b$ is the energy transfer and $S_{be}$ is the related error. Avg_bath $A_b$ (Er: $A_{be}$) is the average energy dissipated per clock cycle, where $A_{be}$ is the average value of the energy transfer or movement to the bath and Sum_clk $S_c$ is the energy moved during the whole simulation. For the whole simulation process, we consider QCA cell dimensions of 18 nm × 18 nm.

**Table 7** The energy dissipation analysis of the D-type flip-flop (PDT-I) design

| *E*_bath_total ($E_{btx}$) | *E*_clk_total ($E_{ctx}$) | *E*_Error_total ($E_{Etx}$) | Sum_bath ($S_b$) | Avg_bath ($A_b$) | Sum_clk ($S_c$) | Avg_clk ($A_c$) |
|---|---|---|---|---|---|---|
| 1.3253e−003 | 1.4469e−005 | −1.9561e−004 | 1.41e−002 eV (error: −1.66e−003eV) | 1.28e−003 eV (error: −1.5e−004eV) | −1.44e−03 | −1.31e−04 |
| 1.5001e−003 | 1.2831e−005 | −2.7346e−004 | | | | |
| 1.2710e−003 | −1.0192e−003 | −1.7538e−004 | | | | |
| 8.3809e−004 | 7.9626e−004 | 1.4508e−004 | | | | |
| 8.3931e−004 | 6.5090e−004 | −1.4205e−004 | | | | |
| 2.0479e−003 | −6.5003e−004 | −3.3385e−004 | | | | |
| 1.2710e−003 | −1.0192e−003 | −1.7538e−004 | | | | |
| 8.3809e−004 | 7.9626e−004 | 1.4508e−004 | | | | |
| 8.3931e−004 | 6.5090e−004 | −1.4205e−004 | | | | |
| 2.0479e−003 | −6.5003e−004 | −3.3385e−004 | | | | |
| 1.2710e−003 | −1.0192e−003 | −1.7538e−004 | | | | |

**Table 8** The energy dissipation analysis of the D-type flip-flop design (PDT-II)

| *E*_bath_total ($E_{btx}$) | *E*_clk_total ($E_{ctx}$) | *E*_Error_total ($E_{Etx}$) | Sum_bath ($S_b$) | Avg_bath ($A_b$) | Sum_clk ($S_c$) | Avg_clk ($A_c$) |
|---|---|---|---|---|---|---|
| 1.3501e−003 | 4.6628e−004 | −1.3058e−004 | 1.58e−002 eV (error: −1.74e−003eV) | 1.44e−003 eV (error: −1.58e−004eV) | 2.57e−03 | 2.34e−04 |
| 1.5883e−003 | 4.5970e−004 | −3.3307e−004 | | | | |
| 1.3870e−003 | −5.3214e−004 | −1.3496e−004 | | | | |
| 1.0965e−003 | 1.0357e−003 | 6.6176e−004 | | | | |
| 1.0067e−003 | 9.0799e−004 | −9.2575e−005 | | | | |
| 2.2490e−003 | −3.2300e−004 | −4.0775e−004 | | | | |
| 1.3870e−003 | −5.3214e−004 | −1.3496e−004 | | | | |
| 1.0965e−003 | 1.0357e−003 | 6.6176e−004 | | | | |
| 1.0067e−003 | 9.0799e−004 | −9.2575e−005 | | | | |
| 2.2490e−003 | −3.2300e−004 | −4.0775e−004 | | | | |
| 1.3870e−003 | −5.3214e−004 | 1.3496e−004 | | | | |

**Table 9** The energy dissipation analysis of the JK-type flip-flop (PJKT) design

| $E$_bath_total ($E_{btx}$) | $E$_clk_total ($E_{ctx}$) | $E$_Error_total ($E_{Etx}$) | Sum_bath ($S_b$) | Avg_bath ($A_b$) | Sum_clk ($S_c$) | Avg_clk ($A_c$) |
|---|---|---|---|---|---|---|
| 1.2100e−003 | −3.5508e−005 | −1.0513e−004 | 1.84e−002 eV (error: −1.64e−003eV) | 1.67e−003 eV (error: −1.50e−004eV) | −7.08e−03 | −6.43e−04 |
| 1.7616e−003 | −8.8490e−004 | −1.5057e−004 | | | | |
| 1.2153e−003 | −8.9387e−005 | −1.0570e−004 | | | | |
| 1.7703e−003 | −9.3843e−004 | −1.5157e−004 | | | | |
| 2.3139e−003 | −1.3294e−003 | −2.2883e−004 | | | | |
| 2.3471e−003 | −7.3944e−004 | −2.1698e−004 | | | | |
| 2.1174e−003 | −1.7950e−003 | −2.0636e−004 | | | | |
| 1.9391e−003 | −2.5334e−004 | −1.7135e−004 | | | | |
| 1.1129e−003 | −4.9544e−004 | −9.6365e−005 | | | | |
| 1.5661e−003 | −6.5559e−004 | −1.2827e−004 | | | | |
| 1.0199e−003 | 1.4002e−004 | −8.3441e−005 | | | | |

**Table 10** The average output polarization (AOP) calculated for the PDT-I, PDT-II, and PJKT design

| Temp. (K) | Polarization for PDT-I | | | Polarization for PDT-II | | | Polarization for PJKT | | |
|---|---|---|---|---|---|---|---|---|---|
| | Max. | Min. | Avg. | Max. | Min. | Avg. | Max. | Min. | Avg. |
| 1 | 9.56e−001 | −9.50e−001 | 3.506 | 9.88e−001 | −9.88e−001 | 3.635 | 9.95e−001 | −9.95e−001 | 3.660 |
| 2 | 9.56e−001 | −9.50e−001 | 3.506 | 9.88e−001 | −9.88e−001 | 3.635 | 9.95e−001 | −9.95e−001 | 3.660 |
| 3 | 9.56e−001 | −9.50e−001 | 3.506 | 9.88e−001 | −9.88e−001 | 3.635 | 9.95e−001 | −9.95e−001 | 3.660 |
| 4 | 9.55e−001 | −9.50e−001 | 3.504 | 9.88e−001 | −9.88e−001 | 3.635 | 9.95e−001 | −9.95e−001 | 3.660 |
| 5 | 9.55e−001 | −9.49e−001 | 3.502 | 9.88e−001 | −9.88e−001 | 3.635 | 9.95e−001 | −9.95e−001 | 3.660 |
| 6 | 9.52e−001 | −9.45e−001 | 3.489 | 9.88e−001 | −9.88e−001 | 3.635 | 9.94e−001 | −9.94e−001 | 3.657 |
| 7 | 9.46e−001 | −9.38e−001 | 3.465 | 9.88e−001 | −9.88e−001 | 3.635 | 9.93e−001 | −9.93e−001 | 3.653 |
| 8 | 9.38e−001 | −9.27e−001 | 3.430 | 9.88e−001 | −9.87e−001 | 3.633 | 9.90e−001 | −9.90e−001 | 3.642 |
| 9 | 9.26e−0010 | −9.13e−001 | 3.383 | 9.87e−001 | −9.87e−001 | 3.631 | 9.84e−001 | −9.84e−001 | 3.620 |
| 10 | 9.11e−001 | −8.95e−001 | 3.322 | 9.86e−001 | −9.86e−001 | 3.627 | 9.74e−001 | −9.57e−001 | 3.552 |
| 11 | 8.92e−001 | −8.75e−001 | 3.250 | 9.84e−001 | −9.84e−001 | 3.620 | 9.58e−001 | −9.58e−001 | 3.524 |
| 12 | 8.72e−001 | −8.52e−001 | 3.171 | 9.82e−001 | −9.81e−001 | 3.611 | 9.34e−001 | −9.34e−001 | 3.436 |

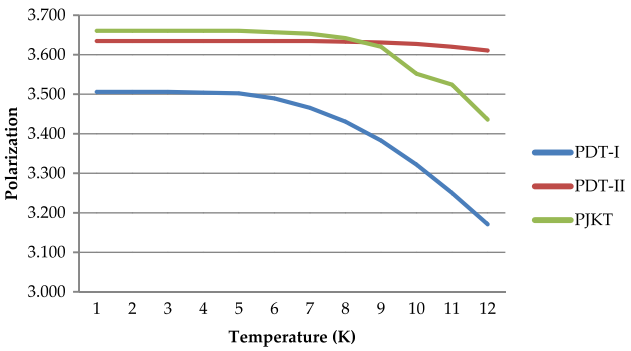


**Fig. 19** The average output polarization of the PDT-I, PDT-II, and PJKT designs

For this proposed design, no energy dissipation (Sum_$E_{bath}$) and (Avg_$E_{bath}$) occurs on average per cycle for the input cells or the fixed input cells of all the majority gates, but the output cell shows an energy dissipation (Sum_$E_{bath}$) of 7.84e−005 eV, 1.80e−004 eV, and 3.14e−004 eV and an average energy dissipation per cycle (Avg_$E_{bath}$) of 7.12e−006 eV, 1.63e−005 eV, and 2.85e−005 eV for DFF-I, DFF-II, and JK FF, respectively, as calculated using the QCADesigner-E tool.

## 6 The AOP calculation

The average output polarization (AOP) of an output cell can be calculated as the difference between the maximum and minimum value of polarization (in eV), divided by two, as expressed in Eq. (13) and measured in joules (J) [35]. For the considered example, at $T = 2$ K, the maximum polarization is 9.56e−01 and the minimum polarization is −9.50e−01 for the output cell (Output-D) of the DFF-I design, the AOP for output-D is [(9.56e−01) − (−9.50e−01)]/2 = 3.506 [35], as in Table 10.

$$\text{AOP for output cell} = \frac{\text{Maximum polarization} - \text{Minimum polarization}}{2} \quad (13)$$

The AOP versus the temperature of PDT-I, PDT-II, and PJKT flip-flop QCA designs is shown in Fig. 19 for the temperature range of 1–12 K. The AOP of the circuit decreases when raising the temperature but decreases slowly up to *T* of 1–7 K, in which temperature range the circuit works completed [36]. Table 10 presents the polarity calculated at different temperates, as also presented graphically in Fig. 19.

## 7 Conclusions

Unique QCA-based edge-triggered synchronous sequential flip-flop circuits (PDT-I, PDT-II, and PJKT) without multilayer crossover are presented herein, being very simple and easy to implement in large nanoscale. The first (PDT-I), second (PDT-II), and JK flip-flop (PJKT) designs achieve an 46.51%, 32.55%, and 24.35% improvement in the QCA cell count. Similarly, the area of the PDT-I, PDT-II, and PJKT designs is calculated to be 28.57%, 28.57%, and 14.28%, respectively, being smaller in comparison with the design previously presented by Chakrabarty [18] with 12,800 samples. In addition, the QCADesigner-E (QD-E) simulation tool is used to calculate the energy dissipation, and the AOP at different temperatures (K) of all three designs (PDT-I, PDT-II, and PJKT).

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