An improved tunnel field-effect transistor with an L-shaped gate and channel

Nithin Abraham[1] · Rekha K. James[2]

Abstract

An improved tunnel field-effect transistor with an L-shaped gate and channel (LLTFET) is proposed herein. The new structure shows an increased ON-current without any change in the overall area in comparison with state-of-the-art structures. The L-shaped gate extends into the substrate and overlaps with part of the source. An N^+ pocket located just below the gate facilities tunneling in both the horizontal and vertical directions, which results in the increased ON-current. Three different models are proposed herein to increase the ON-current with the added advantage of simplified fabrication steps. For one of the proposed models, the ON-current is improved by 63% while the OFF-current is reduced to 12.5% compared with an L-shaped gate TFET (LGTFET) described in literature. An optimum model is also proposed, achieving a subthreshold swing of 21.2 mV/decade at $0.05V_{gs}$. The simulations are performed using Silvaco ATLAS with the nonlocal band to band tunneling (BTBT) model.

Keywords Band to band tunneling · Tunnel field-effect transistor · TFET · Tunnel field-effect transistor with L-shaped gate and channel · LLTFET

1 Introduction

Ultralow-power devices are the future of integrated circuits. However, the application of metal–oxide–semiconductor (MOS) transistors in applications where low power and fast switching are desired is limited by the subthreshold swing of 60 mV/decade. The need for transistors which can achieve subthreshold swing values below 60 mV/decade has led to the development of tunnel field-effect transistors (TFETs) [1, 2], because the limit of 60 mV/decade does not apply when the basic operating principle is band to band tunneling (BTBT), resulting in good candidates for use in low-power applications. In a conventional TFET, the tunneling occurs parallel to the channel, resulting in a decreased tunneling area which reduces the maximum ON-current that the device can support. The ON-current can be increased by increasing the channel width and thereby the tunneling area, at an expense of larger device size. Many models have been suggested in literature to improve the ON-current without increasing the area. The LTFET [3], UTFET [4], and LGTFET [5] use gates which extend into the substrate, to increase the tunneling area by making the tunneling take place perpendicular to the channel. Meanwhile, a tunnel field-effect transistor with an L-shaped gate and channel is proposed herein. The inverted L-shaped channel helps achieve a large tunneling area and hence increase the ON-current. The changes applied in the structure result in simplified fabrication steps compared with those required to obtain the LGTFET [5]. The results of the simulations show that the proposed structure offers better performance in terms of the ON-current, OFF-current, and subthreshold swing. The effect of various parameters on the drain current (I_d) of the proposed structure are also investigated.

✉ Nithin Abraham
  nithina@iisc.ac.in

  Rekha K. James
  rekhajames@cusat.ac.in

1 Indian Institute of Science (IISc), Bangalore, India

2 Division of Electronics, Cochin University of Science and Technology, Kochi, India
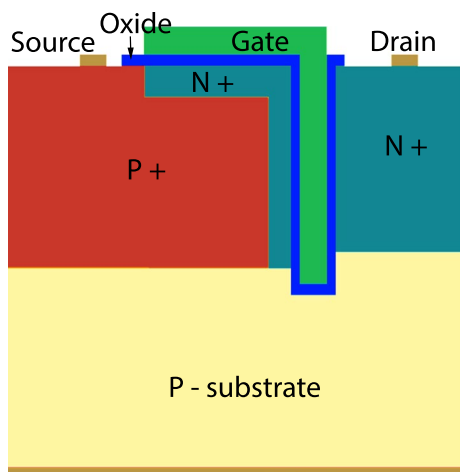
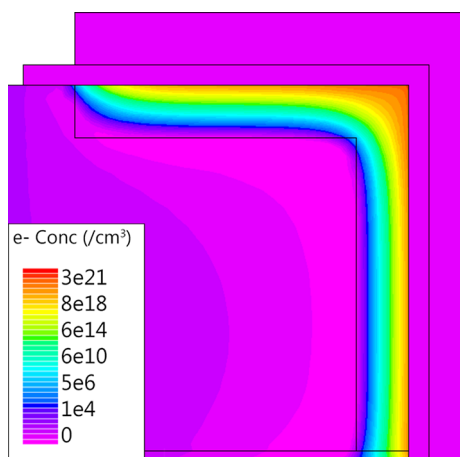**Fig. 1** The structure of the proposed TFET with an L-shaped gate and channel

Fig. 2 The formation of the L-shaped channel under the gate region

2 The device structure

The aim of this study is to investigate the performance improvements obtained by modifying the shape of the gate. The model of the proposed LLTFET is illustrated in Fig. 1. In this structure, the gate is extended into the substrate, which helps tunneling to occur perpendicular to the vertical channel. The L-shaped gate region extends in the horizontal direction, providing a horizontal channel below the gate overlap, which contributes to the ON-current. An N^+ pocket in the shape of an inverted L helps with channel formation and tunneling [4, 6]. Figure 2 clearly depicts the shape of the resulting channel. Tunneling occurs in the vertical and horizontal directions, thereby increasing the tunneling rate and hence the ON-current compared with previously proposed structures.

The substrate is based on silicon doped P^- type. A source region with a P^+ concentration of $10^{20}/cm^3$ and height of 35 nm is grown by epitaxy. The N^+ pocket is also grown epitaxially to a thickness of 5 nm with a doping concentration of $10^{19}/cm^3$. The optimum width of the N^+ pocket has been found to be 5 nm [5]. Increasing the width of the N^+ pocket width increases the barrier width for electron tunneling, which in turn reduces the tunneling probability. Therefore, the N^+ pocket must be grown carefully using accurate epitaxial methods. The N^+ drain region is formed by ion implantation with a concentration of $10^{19}/cm^3$. Unlike the N^+ pocket, the N^+ drain can have a diffused profile. Different models are proposed herein based on variation of the depth of the drain region and thereby the tunneling area. The gate region is made of polysilicon with a thickness of 5 nm, extending 38 nm into the substrate in the vertical direction and 32 nm over the source region. The oxide layer is formed with a thickness of 2 nm. This structure requires reduced fabrication steps compared with the LGTFET. Since the N^+ region is in the shape of an inverted L, the P^+ source can be grown by epitaxy or ion implantation. For the LGTFET, the P^+ source is formed only by epitaxy, which reduces the number of etching stages required. The overlap of the gate over the source facilitates the fabrication of the contact to the gate electrode, as the surface area for the contact is increased. In this structure, the entire N^+ pocket region supports channel formation, whereas in previous versions, part of the N^+ pocket in the horizontal direction had less effect on the channel formation. The described reduction in the fabrication steps due to the change in the shape of the gate is also applicable for other similar structures. The exact fabrication steps depend on the type of TFET for which the modification is made.

3 Simulations and results

Three models are proposed herein by varying the depth of the drain region of the LLTFET, being denoted as LLT-FETv1, LLT-FETv2, and LLTFETv3. The depth of the drain region is varied from 10 to 48 nm, where the depth is low for LLTFETv1, moderate for LLTFETv2, and high for LLT-FETv3. All the models are simulated using Silvaco ATLAS with the nonlocal BTBT model. The device operates under a drain-to-source voltage (V_{ds}) of 1 V while the gate-to-source voltage (V_{gs}) is ramped from 0 to 1.5 V. The drain current (I_d) versus V_{gs} characteristic for the LGTFET structure and the different proposed models of the new LLTFET structure are shown in Fig. 3. For the same drain depth as in the LGT-FET, the proposed LLTFETv1 structure offers improved performance due to the increased tunneling area. Meanwhile, LLTFETv2 and LLTFETv3 also have the same tunneling

Fig. 3 Simulation results showing I_d versus V_{gs} for the three variants of the LLTFET and LGTFET at $V_{ds} = 1$ V. **a** I_d on a linear scale, showing the variations in I_{ON}. **b** The results on a log scale, showing the variations in I_{OFF}. The X-axis is scaled to show the OFF-current
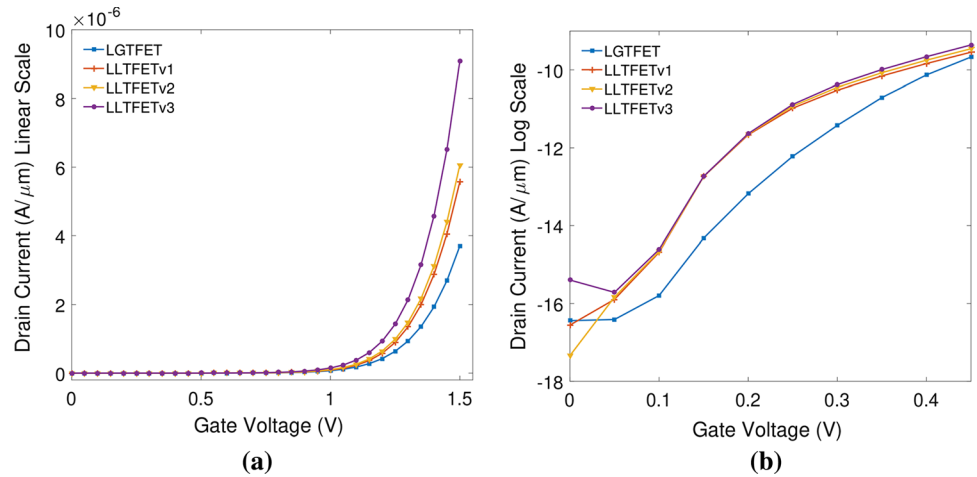
area as LLTFETv1 but with higher ON-currents. Figure 3a clearly depicts the increase of the ON-current found for the three models compared with the LGTFET.

The variation of the ON- and OFF-currents results due to the increase in the drain depth. The N^+ pocket below the P^+ source, as in Ref. [3–5], is not present in the proposed models. This reduces the leakage current resulting from the presence of minority electrons in the region between the source and drain. Of the three models proposed, although LLTFETv3 gives the maximum ON-current, LLTFETv2 is considered to be the optimum structure since it gives an increased ON-current as well as a reduced OFF-current. The LLTFETv2 model shows an increased ON-current of 6.06×10^{-6} A/µm and a reduced OFF-current of 4.57×10^{-18} A/µm, compared with 3.71×10^{-6} A/µm and 3.63×10^{-17} A/µm respectively for the LGTFET. A larger ON-current is possible with the LLTFETv3, but this comes at the expense of the OFF-current. Even then, the OFF currents of the LLTFETv1 and LLTFETv3 are comparable to that of the LGTFET.

In the proposed models, the response to a variation of the gate voltage is increased due to the larger area of the N^+ pocket closer to the gate. A minimum subthreshold swing of 21.2 mV/decade is observed at 0.05 V for the LLTFETv2, representing a reduction of 17.3 mV/decade compared with the value of 38.5 mV/decade for the LGTFET. From Fig. 3b, it is clear that the subthreshold swing for the LLTFETv2 is lower compared with that for LGTFET in the low voltage region. At higher voltages, the subthreshold swing for LLTFETv2 is slightly higher than that for LGTFET. However, at very low voltages, the plot in Fig. 3b for the LGTFET is becoming flat while that for LLTFETv2 remains steep. This indicates that, in these regions, the LLTFETv2 responds to a change in V_{gs} whereas the LGTFET cannot.
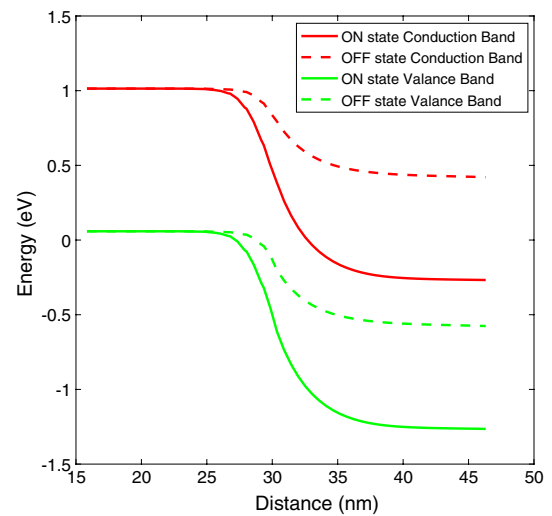

Fig. 4 The energy band diagram in the ON- and OFF-states along the horizontal tunneling region below the gate

The energy band diagram for the LLTFETv2 in the ON- and OFF-states are shown in Fig. 4. The analysis is done along the horizontal direction just below the gate where the horizontal channel is formed. The band diagram along the vertical channel is similar and is already discussed in detail in Ref. [5]. The proposed models also provide a significant amount of band overlap over a larger area, which is one of the key factors for the increased ON-current.

3.1 The effect of area

The inverted L-shaped gate increases the channel area in the LLTFET compared with the LGTFET. Figure 5a shows the direction of the electric field lines, which are perpendicular to the channel under the gate region. Due to this field, the tunneling of electrons from the valance

Fig. 5 **a** The electric field lines at V_{gs} of 1.5 V, showing the magnitude and direction of the electric field in the tunneling region. **b** The electron tunneling across the channel
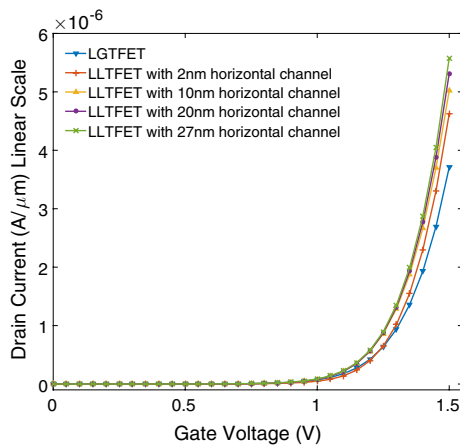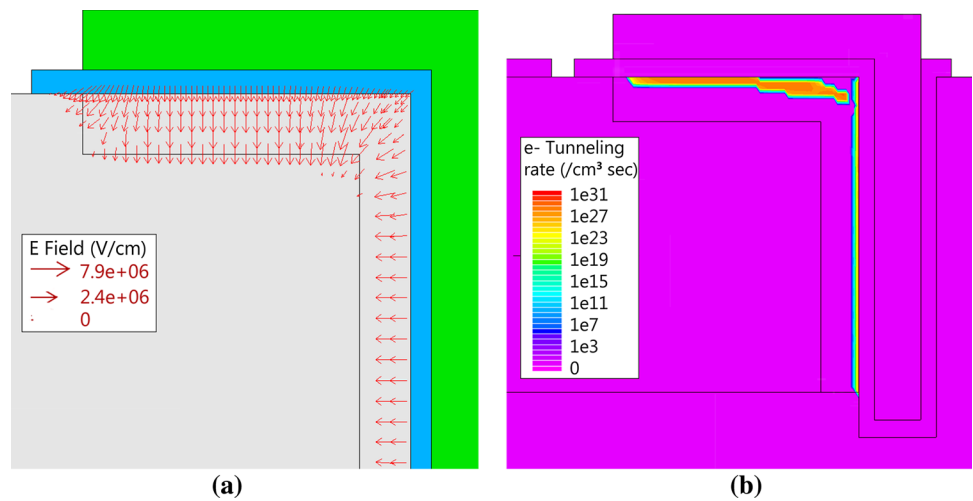

(a)

(b)

Fig. 6 The I_d versus V_{gs} characteristic for different horizontal tunneling areas with a 10-nm-deep drain region
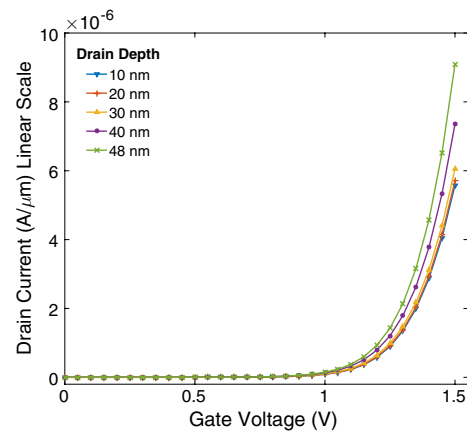

Fig. 7 The I_d versus V_{gs} characteristic for different depths of the drain region with a gate extending 27 nm horizontally over the source

band of the P^+ source to the conduction band of the N^+ pocket is greater compared with the flow in the reverse direction. This results in electrons tunneling horizontally into the vertical channel, vertically into the horizontal channel, and diagonally near the intersection. The diagonal and vertical tunneling is the result of the inverted L-shaped N^+ pocket structure. The increase in the tunneling rate results in an increase in the ON-current, which is achieved without any overhead in terms of the total device area. Figure 5b shows the tunneling rate of electrons into the channel, while Fig. 6 shows the increase in the ON-current with the increase in the tunneling area. The addition of diagonal tunneling itself has a large effect of the total current, which aids the increase of the ON-current from 3.71×10^{-6} to 5.57×10^{-6} A/µm. Similar to in conventional TFETs, in the horizontal channel, tunneling also occurs parallel to the channel, although this

factor is small compared with the effect due to the perpendicular tunneling.

3.2 The effect of the drain depth

The drain region is formed by ion implantation. The device characteristics can be improved by controlling the depth to which the ions are implanted. The ON-current is found to increase with the depth of the drain region. This is due to the change in the channel length and the ease of formation of the channel. When the drain depth is small, the channel length is greater, and when the drain depth is high, the

channel length is less. Decreasing the channel length gives rise to a reduced channel resistance and thereby increases the ON-current. When the drain depth is increased, the change in the channel length is the main reason for the change in the ON-current, until the depth of the drain aligns with the bottom of the gate, after which point the channel length does not decrease. However, the channel width will increase, thus further reducing the channel resistance. Moreover, the presence of the drain below the gate will increase the electron concentration in the nearby P^- regions and make the channel formation easier. However, this will also result in an increased OFF-current. So, in the optimum LLTFET model, the drain depth is fixed just above the bottom of the gate. Figure 7 shows the variation in the ON-current with increasing drain depth. The drain current varies from 5.57×10^{-6} A/µm for the LLTFET with a drain depth of 10 nm to 9.09×10^{-6} A/µm for the LLTFET with a drain depth of 48 nm, after which the drain extends further into the substrate than the bottom of the gate.

3.3 The reduction in the OFF-current

The electron current density at $V_{gs} = 0$ V and $V_{ds} = 1$ V for the LGTFET and the proposed model are shown in Figs. 8 and 9, respectively. The electron concentration below the gate is higher for the LGTFET. This is due to the presence of the horizontal N^+ pocket sandwiched between the P^+ source and the substrate. This layer will increase the electron concentration in the substrate near the gate, where they are minority carriers. These electrons contribute to the leakage between the source and drain and thus result in higher OFF-current. The removal of the horizontal N^+ pocket below the source in the proposed structure reduces the minority concentration in the substrate and thereby the leakage current. Similar to the presence of the $^+$ pocket, the depth of the
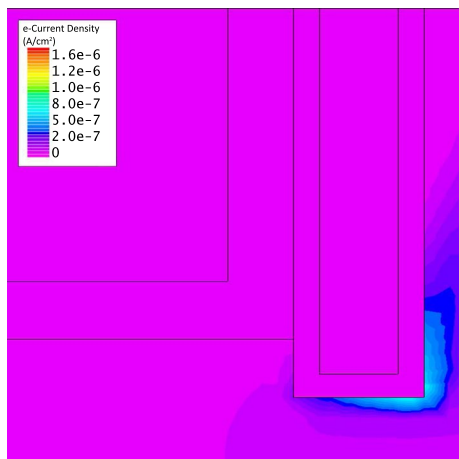

Fig. 8 The electron current density under the gate region of the LGTFET at $V_{gs} = 0$ V and $V_{ds} = 1$ V
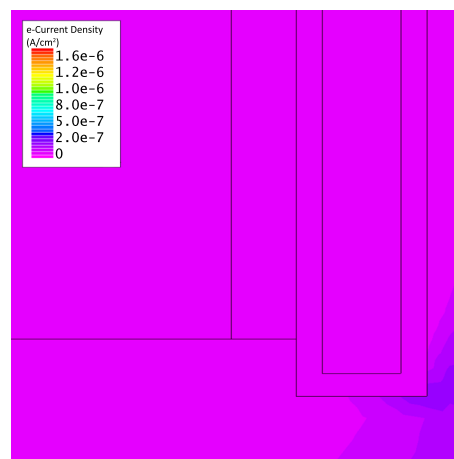

Fig. 9 The electron current density under the gate region of the LLTFETv2 at $V_{gs} = 0$ V and $V_{ds} = 1$ V

drain region also affects the minority carrier concentration and thus impacts on the OFF-current. The OFF-current for the optimum model is 4.57×10^{-18} A/µm, representing a reduction of 87.5% compared with the LGTFET.

Table 1 presents a comparison of the proposed structure with previously described structures based on the ON-current, OFF-current, and subthreshold swing. The optimum model (LLTFETv2) and the model with better ON-current (LLTFETv3) are compared with the LGTFET [5] and UTFET [4].

4 Conclusions

An LLTFET structure with an L-shaped gate and channel is proposed and studied. Simulations are carried out using Silvaco ATLAS. A larger ON-current and smaller OFF-current are achieved for the proposed structure. Compared with the LGTFET, the ON-current is increased by 63% while the OFF current is reduced to 12.5% for the optimum model of the proposed structure. One of the models gives an increase of the ON-current by 145% compared with that of the LGTFET with the same OFF-current. The removal of the N^+ pocket below the source and the addition of an N^+ pocket above the source result in reduced fabrication steps

Table 1 A comparison with previously described structures

	ON-current (A/µm)	OFF-current (A/µm)	SS (mV/decade)
UTFET	3.00×10^{-7}	5.00×10^{-16}	34.0
LGTFET	3.71×10^{-6}	3.63×10^{-17}	38.5
LLTFETv2	6.06×10^{-6}	4.57×10^{-18}	21.2
LLTFETv3	9.09×10^{-6}	4.00×10^{-16}	26.6

and improved performance. The tunneling area is increased without increasing the overall device area. The effects of the depth of the drain region on the ON- and OFF-currents are also investigated. A subthreshold swing of 21.2 mV/decade is achieved, which along with the better current characteristics, makes the proposed LLTFET a good candidate for use in ultralow-power applications. This idea of extending the gate into and over the P^+ source, along with the addition of an N^+ pocket just below the gate, could also be adopted for conventional devices.

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