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Boosting the performance of an ultrascaled carbon nanotube junctionless tunnel field-effect transistor using an ungated region: NEGF simulation

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Abstract
This paper focuses on the role of the longitudinal spacing between the auxiliary gate and control gate in boosting the performance of an ultrascaled junctionless carbon nanotube tunnel field-effect transistor (JL CNT-TFET). The investigation is based on self-consistent quantum simulations in the nonequilibrium Green's function formalism in the ballistic limit. It is found that dilation of the ungated longitudinal space between the gates causes a significant improvement in the leakage current, ambipolar behavior, subthreshold swing, on/off-current ratio, power–delay product, and intrinsic delay. In addition, a substantial enhancement in the swing factor and current ratio is also recorded for the JL CNT-TFET with coaxial control gate length below 10 nm. The results indicate that adjusting the spacing between the auxiliary gate and control gate is a simple, efficient, and promising approach to achieve ultrascaled JL CNT-TFETs with very high performance.

Keywords Junctionless · Carbon nanotube tunnel field-effect transistor (CNT-TFET) · Nonequilibrium Green's function (NEGF) · Tunneling · Spacing · Switching characteristics · Sub-10-nm technology

1 Introduction

Field-effect transistors (FETs) with 1-nm gate length can now be fabricated [1], which represents a substantial advancement that could open the door to new technology based on FETs with subnanometer gate lengths. Over the last few years, many experimental and theoretical works have focused on assessment of the performance and scaling capability of new FETs with sub-5-nm gate lengths by exploiting emerging two-dimensional (2D) and pseudo-2D materials to shrink FET gate lengths down to the maximum extent possible within the framework of the International Technology Roadmap for Semiconductors (ITRS) [2–5].

Tunnel field-effect transistors (TFETs) [6, 7] have attracted increasing interest for use in future nanoelectronics due to the benefits they provide at the nanoscale regime, such as subthreshold swing values below 60 mV/dec [8, 9]. The only constraints on the miniaturization of such promising devices is the realization of high-gradient junctions in this ultrascaled domain [6–10]. The junctionless technique is considered to be an efficient solution to avoid such abrupt junctions, easing the burdens in terms of cost, complexity, and reliability [11–13]. For this reason, huge efforts have been focused on junctionless transistors while attempting to continue their miniaturization [11–15]. The idea of using the TFET structure while retaining the junctionless paradigm has resulted in a new sort of TFET called the junctionless tunnel field-effect transistor (JL TFET) [16]. These devices include uniform channel doping, where the TFET mechanism is ensured by electrostatic gating that imitates the different doping levels and controls the carrier transport [16, 17]. For this reason, JL TFETs are considered to be promising candidates for use in modern nanoelectronics due to their advantages in terms of performance improvement, ease of fabrication, and scaling ability [16–18]. Recently, several works have proposed new ways to boost the performance of JL TFETs [17–20], mostly based on dielectric and/or work function engineering. However, the processes required for these techniques are considered infeasible for ultrascaled devices, where many quantum and atomistic effects are active [1–6], thus the reliability, which is the main concern, can be affected by any fabrication inaccuracies. Therefore,

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simple approaches that take into account the scaling capability in terms of fabrication while retaining the required reliability and high performance should be proposed for future nanoelectronics.

Considering the developments described above, we combine herein the benefits of a carbon nanotube (CNT) channel [21], the gate-all-around geometry [22], the junctionless paradigm [12], and the tunnel FET concept [6] to propose a new ultrascaled high-performance device called the junctionless carbon nanotube tunnel field-effect transistor (JL CNT-TFET), in which a beneficial ungated spacing between the two gates is introduced. This new, simple, and efficient design is proposed and assessed by using quantum simulations based on self-consistent solution of the Poisson and Schrödinger equations using the nonequilibrium Green's function (NEGF) formalism [23–25]. It is found that a simple dilation in the ungated spacing between the auxiliary and control gates in the proposed design can significantly improve the switching characteristics.

The remainder of this manuscript is organized as follows: Section 2 describes the structure and dimensions of the conventional (p–i–n) CNT-TFET and the JL CNT-TFET with different ungated spacings between the gates. Section 3 presents a brief description of the quantum simulation approach. In Sect. 4, the simulation results are presented, analyzed, and discussed. Section 5 summarizes the obtained results.

2 Nanodevice structure

Figure 1 shows a lengthwise cut view of the conventional (p–i–n) CNT-TFET and junctionless CNT-TFET. The nominal configuration includes a zigzag (10, 0) carbon nanotube (Z-CNT), which is fully surrounded by a coaxial hafnium (HfO_2) layer with thickness of $t_{OX} = 2$ nm and dielectric constant of $\varepsilon = 16$. The length of the coaxial control gate is taken to be $L_G = 10$ nm in all the nanodevices. In the conventional (p–i–n) CNT-TFET, the source (drain) is heavily p-type (n-type) doped to concentration of -1.5 (1.5) nm^{-1}, while the CNT underneath the coaxial control gate is normally assumed to be intrinsic [17]. Note that the source and drain doping is assumed to be uniform, without considering the possibility of fluctuations.

In the case of the JL CNT-TFET, the Z-CNT is wholly n-type doped (N^+) with a reasonable concentration of $N_{CNT} = 1.5$ nm^{-1}, while avoiding the abrupt junctions present in the conventional CNT-TFET, thus simplifying the fabrication processes. Note that the source side is electrostatically p-type doped via the auxiliary gate (P-gate), which is biased at a fixed $V_{PG} = -0.8$ V [17]. Inspection of Fig. 1b, c reveals that two different ungated distances between the coaxial auxiliary gate (P-gate) and coaxial control gate (L_{SP}) are considered (2 nm and 6 nm), which is the critical consideration

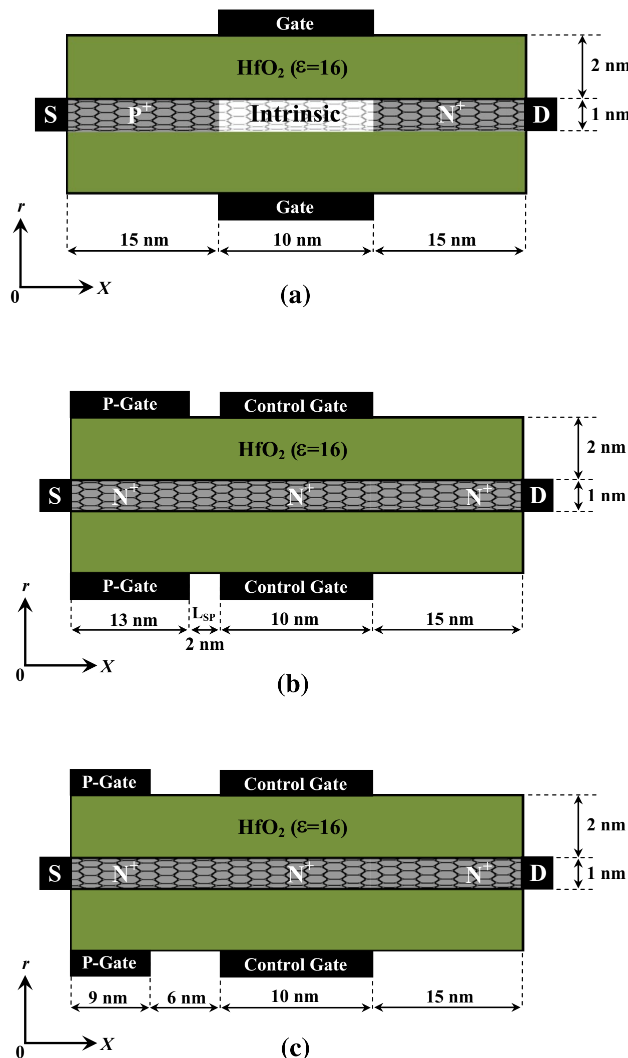

Fig. 1 A cross-sectional view of the **a** conventional (p–i–n) carbon nanotube tunnel field-effect transistor (CNT-TFET), **b** junctionless carbon nanotube tunnel field-effect transistor (JL CNT-TFET), and **c** proposed JL CNT-TFET with longer ungated spacing between the two gates

in this work. Note that the drain side of the JL CNT-TFET with nominal length of 15 nm is not covered by a gate. The drain–source voltage (V_{DS}) is taken to be equal to 0.3 V, and room temperature of $T = 300$ K is considered throughout the investigation. It is worth noting that some geometrical parameters are varied in the scaling analysis.

3 Quantum simulation approach

The investigated CNT-TFETs are simulated using a quantum simulation approach based on the nonequilibrium Green's function (NEGF) formalism, which is principally employed to solve the Schrödinger equation self-consistently

with the Poisson equation [23–28]. Scattering mechanisms are neglected, assuming ballistic transport [26]. Note that phonon scattering has been found to have a small effect on the characteristics of conventional (*p*–i–*n*) CNT-TFETs, as reported in Ref. [29]. The nearest-neighbor tight-binding (TB) Hamiltonian used for the Z-CNT is based on a *pz*-orbital basis as in Ref. [26]. The mode-space NEGF is used to decrease the computational burden, where only the dominant modes are considered [30–32]. The finite difference method is applied to solve the two-dimensional Poisson equation for the cylindrical geometry [33, 34]. After achieving self-consistency of the NEGF and Poisson solvers, the electrical and physical characteristics (drain current, density of states, band diagram, charge density, potential profile, transmission, etc.) of the nanodevices can be extracted from the NEGF quantities [35]. Note that the accuracy of the quantum simulation is confirmed by our previous relevant work [35]. For more details regarding the computational methodology, NEGF equations, and coupling techniques, the reader is referred to previous classic works in the field [26–28].

4 Results and discussion

Figure 2 shows the transfer characteristics of the nanodevices under investigation using a drain bias of 0.3 V. It is clearly seen that the conventional (*p*–i–*n*) CNT-TFET exhibits an ambipolar feature that causes an increase in the leakage current, which is undesirable for digital nanoelectronics applications. This ambipolar behavior has a similar cause to the ambipolar property in Schottky barrier (SB) CNT-FETs [29]. The band-to-band tunneling (BTBT) from

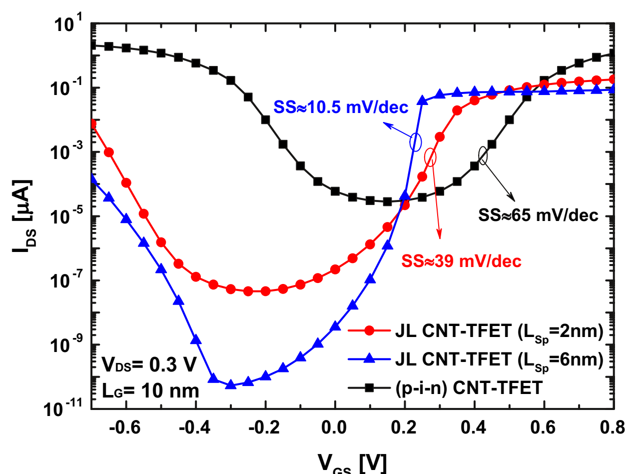

Fig. 2 The I_{DS}–V_{GS} transfer characteristics of the conventional CNT-TFET and JL CNT-TFET with two different longitudinal spacings between the auxiliary gate and control gate

the source (drain) to the channel (CNT channel) results in electron (hole) transmission at high (low) gate–source voltage V_{GS} [29]. Inspection of Fig. 2 reveals that the two JL CNT-TFETs exhibit lower minimal leakage currents in comparison with the conventional (*p*–i–*n*) CNT-TFET due to the increase in the length of the direct tunneling window (in off-state), which is analyzed thoroughly below. It is clear that the ambipolar I_{DS}–V_{GS} characteristic is reduced for the JL CNT-TFET. Moreover, a significant improvement in the subthreshold swing (SS) is also recorded for the JL CNT-TFET, where SS = 39 and 10.5 mV/dec are recorded when using the L_{SP} distances of 2 nm and 6 nm, respectively. However, the aforementioned improvements (in the ambipolar behavior, leakage current, and subthreshold swing) come at the expense of a degraded on-current, as is easily seen from the same figure. It is important to note that the subthreshold swing is numerically extracted using the relation

$$SS = \Delta V_{GS} / \Delta \log_{10} \left(I_{DS} \right). \quad (1)$$

Figure 2 also shows that the tunnel (*p*–i–*n*) FET exhibits a subthreshold swing greater than 60 mV/dec. The latter is due to the considered short gate length (10 nm), which reflects the short direct tunneling window (short tunneling barrier), causing a high off-current and high subthreshold swing. Note that, by considering relatively longer gate lengths, SS values below 60 mV/dec can normally be obtained [25], while ultrashort gate lengths lead to SS values above 60 mV/dec, as in Refs. [4, 30]. In our case, we intentionally consider sub-10-nm-gate lengths in order to show the high performance of the proposed design in the ultrascaled domain.

Figure 3 shows the electron concentration spectrum versus the longitudinal position along the Z-CNT channel for the three TFETs under study. In all these figures, the top and bottom white lines denote the conduction and valence bands, respectively. The bandgap between the energy band diagrams is clearly seen with low electron density. It is worth noting that the figures in the left column are extracted near the minimal drain currents in the *I*–*V* transfer characteristics shown in Fig. 2, while those in the right column are drawn at V_{GS} = 0.6 V.

Inspection of Fig. 3a, c, and e, which correspond to the (*p*–i–*n*) CNT-TFET, JL CNT-TFET with L_{SP} = 2 nm, and JL CNT-TFET with L_{SP} = 6 nm, respectively, reveals that the BTBT distances at the drain side (channel–drain interface) are wider in Fig. 3c, e in comparison with the (*p*–i–*n*) CNT-TFET in Fig. 3a, due to the absence of the abrupt junction. Note that the intrinsic/*n*-type doping junction abruptly changes the band diagram, leading to a shrinking in the right BTBT window as well as the direct tunneling window, as shown in Fig. 3a. In addition, the spacing L_{SP} between the auxiliary and control gates also contributes to the alleviation of the abrupt variation in the band diagram at the

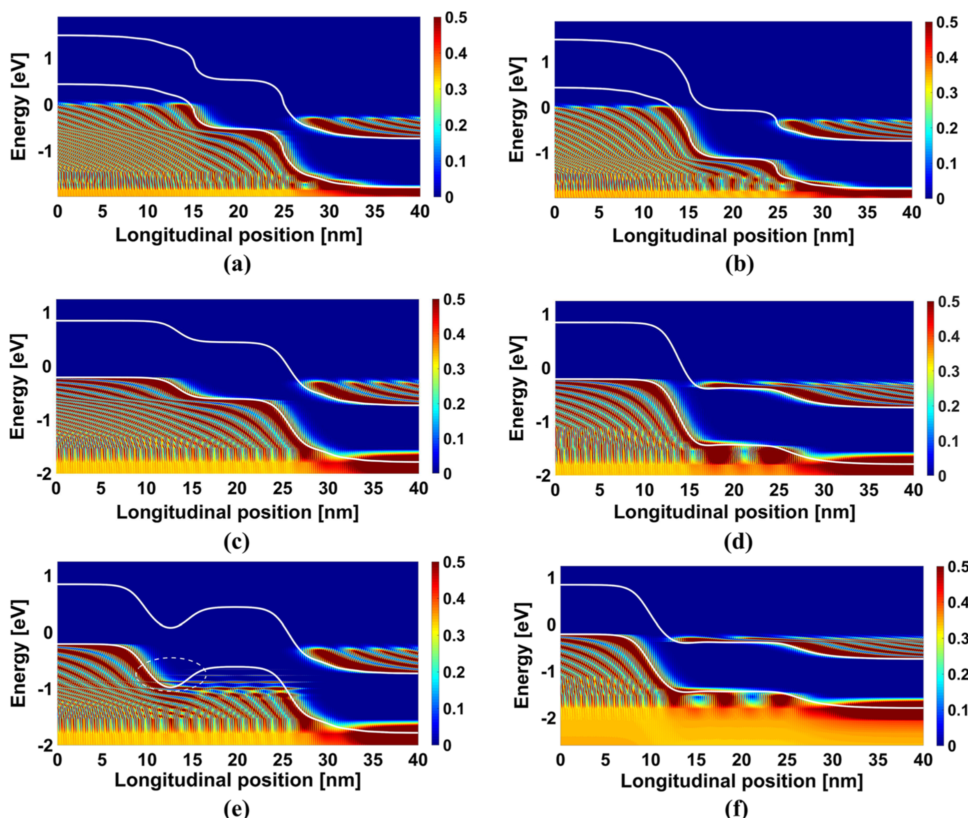

Fig. 3 The electron density per unit energy (dn/dE) as a function of the x-position for **a**, **b** the (p–i–n) CNT-TFET, **c**, **d** the JL CNT-TFET with $L_{SP}=2$ nm, and **e**, **f** the JL CNT-TFET with a longer ungated spacing ($L_{SP}=6$ nm) between the auxiliary and control gates. Note that the left figures are drawn around the minimal drain currents in the transfer characteristics of Fig. 2, while the right figures are extracted at $V_{GS}=0.6$ V

source–channel interface, thus a dilation in the direct tunneling window is also recorded. The afore-described expansions at the source and drain sides explain the enhancements recorded in the minimal leakage current, ambipolar behavior, and swing factor, as shown in Fig. 2. In particular, in Fig. 3e, the increase in L_{SP} (from 2 nm to 6 nm) leads to the appearance of a kind of barrier due to the lack of any electrostatic gating in this zone, hence the barrier curvature tends to the band level of the drain side. This ungated-space-induced barrier, which is surrounded by the dashed circle in the same figure, significantly decreases the carrier tunneling at the initial alignment of the valence band of the channel with the conduction band of the drain, resulting in a great enhancement in terms of the leakage current and ambipolar property, as shown in the I–V characteristics in Fig. 2.

The figures in the left column reveal that the conventional TFET (Fig. 3b) exhibits a smaller BTBT path at the source–channel interval in comparison with the JL CNT-TFETs in Fig. 3d, f, which explains the degradation of the on-current in the JL TFETs (Fig. 2). Note that the BTBT path at the source side in the JL CNT-TFET with $L_{SP}=2$ nm is shorter than that with $L_{SP}=6$ nm, thus the I_{ON} of the JL CNT-TFET with $L_{SP}=2$ nm is greater than that with $L_{SP}=6$ nm, as shown in Fig. 2. Therefore, the enhancements recorded in Figs. 2 and 3 are due to the proposed band-engineering strategy, which is based on adjustment of the ungated region between the gates, due to which the direct tunneling window (tunneling barrier) in off-state becomes longer, leading to the improved swing factor and off-current.

The curves in Fig. 4 are extracted from the I_{DS}–V_{GS} transfer characteristics in Fig. 2 by sweeping (from right to left within a reasonable range) a window of 0.3 V horizontally bounded by V_{GS-ON} and V_{GS-OFF} ($V_{GS-ON}-V_{GS-OFF}=0.3$ V), which corresponds to the on-current (I_{ON}) and off-current (I_{OFF}), respectively [29, 34, 36]. The figure plots the current ratio versus the on-current for the three types of CNT-TFETs under investigation. The

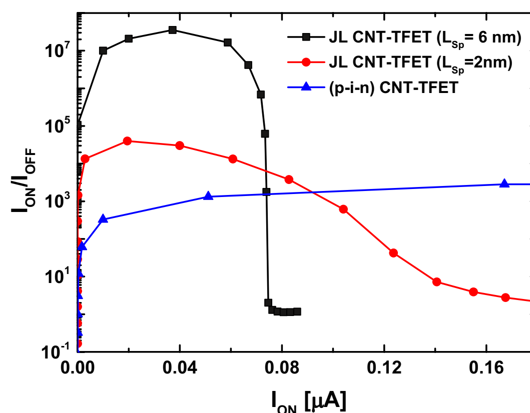

Fig. 4 The I_{ON}/I_{OFF} current ratio as a function of the on-current for the three CNT-TFETs

JL CNT-TFET with $L_{SP}=6$ nm outperforms the JL CNT-TFET with $L_{SP}=2$ nm and the conventional CNT-TFET in terms of the maximum achievable current ratio by about three and four orders of magnitude, respectively. This is considered to represent a substantial improvement by simply using a longer spacing between the auxiliary gate and control gate. Inspection of the same figure reveals that the conventional (*p*–i–*n*) CNT-TFET and the JL CNT-TFET with $L_{SP}=2$ nm exhibit greater on-current in comparison with the JL CNT-TFET with $L_{SP}=6$ nm, but with relatively modest current ratios due to the recorded high off-current.

In order to thoroughly assess the switching behavior of the improved JL CNT-TFET endowed with a large L_{SP} spacing, the intrinsic delay (τ) and power–delay product (PDP) are plotted in Fig. 5a and b, respectively. Note that these important switching characteristics are computed numerically as [34]

$$t = \left(Q_{ON} - Q_{OFF}\right)/I_{ON}, \quad (2)$$

$$\mathrm{PDP} = \left(Q_{ON} - Q_{OFF}\right)V_{DD}, \quad (3)$$

where Q_{OFF} (Q_{ON}) and V_{DD} are the whole channel charge in off-state (on-state) and the power supply voltage (0.3 V), respectively [36]. Note that Q_{OFF} (Q_{ON}) is extracted as I_{OFF} (I_{ON}) in Fig. 4 by considering a window with width of 0.3 V [36, 37]. Figure 5a shows that the JL CNT-TFET with $L_{SP}=6$ nm exhibits a shorter intrinsic delay over the considered I_{ON} range in comparison with the similar device with $L_{SP}=2$ nm or the (*p*–i–*n*) TFET. Figure 5b shows the PDP versus the current ratio for the three devices, clearly revealing that the JL CNT-TFET with $L_{SP}=6$ nm provides the highest maximum current ratio while consuming an energy comparable to the PDP of the other devices. These results indicate that the JL CNT-TFET endowed with an ungated region of $L_{SP}=6$ nm is highly desirable for use in high-speed and low-power applications.

Figure 6 shows the behavior of the subthreshold swing and the maximum reachable current ratio versus gate length downscaling for the JL CNT-TFETs with two different values of the spacing between the gates (2 and 6 nm). Figure 6a shows that the JL CNT-TFET endowed with $L_{SP}=6$ nm exhibits a steep subthreshold swing (< 60 mV/dec) over the whole considered range (4 nm $\leq L_G \leq$ 10 nm), with recorded swing factors of 42.5, 18.5, 11.2, and 10.5 mV/dec for $L_G=4$, 6, 8, and 10 nm, respectively. Shrinking L_{SP} from 6 nm to 2 nm significantly increases the SS factor, with a significant increase being recorded for $L_G=4$ nm. Therefore, the benefit attributed to L_{SP} dilation in terms of the SS is more pronounced below 5 nm, making the presented spacing approach a very promising option. Figure 6b shows the effect of gate length downscaling on the I_{ON}/I_{OFF} current ratio for the two types of JL CNT-TFET, revealing that use of the dilated L_{SP} spacing results in a significant increase in the current ratio (by about three orders of magnitude) over the whole scaling range.

It is noteworthy that the effects of defects, contact resistance, scattering, and random doping fluctuations are not considered in this work. These kinds of effects could be the subject of further investigations, where full three-dimensional (3D) quantum simulations (real-space NEGF and 3D Poisson equation) may be required. The highly improved switching characteristics obtained in this work, together with the benefits associated with the junctionless paradigm [15], gate-all-around structure [38, 39], and realization of a simple longitudinal spacing between the auxiliary and control gates, make the proposed JL CNT-TFET (with adjusted ungated spacing) a highly promising candidate for sub-5-nm technology. A similar methodology might also be applicable to improve identical ultrascaled JL tunnel FETs based on

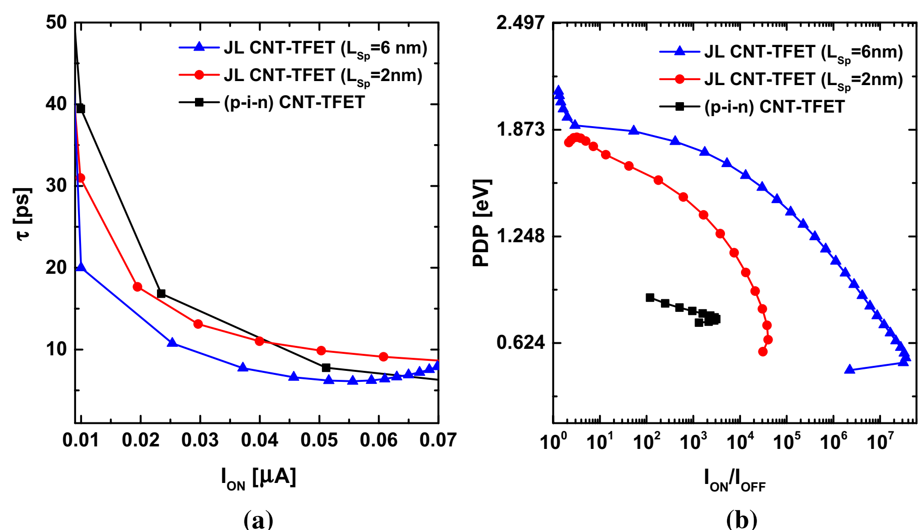

Fig. 5 **a** The intrinsic delay as a function of the on-state current for the three CNT-TFETs under investigation. **b** The power–delay product versus the current ratio for the three nanotransistors

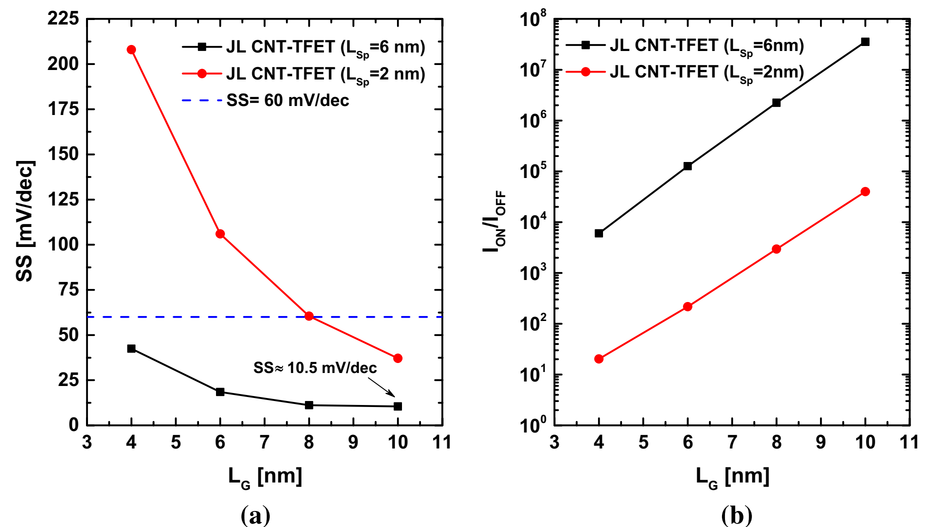

Fig. 6 **a** The subthreshold swing and **b** maximum reachable current ratio as functions of the control gate length over a sub-10-nm range for the JL CNT-TFET with two different L_{SP} spacings of 2 nm and 6 nm

emerging nanomaterials [40–44]. Moreover, metaheuristic techniques could be employed to determine the optimum parameter values that would lead to the maximum possible ultimate switching performance [45, 46].

5 Conclusions

A new strategy based on adjustment of the ungated longitudinal spacing between the auxiliary gate and control gate is proposed to boost the performance of nanoscale junctionless carbon nanotube tunnel field-effect transistors. The device is investigated using quantum simulations based on self-consistent solution of the Schrödinger and Poisson equations in the NEGF formation. An exhaustive investigation is presented, including the $I_{DS}-V_{GS}$ transfer characteristics, electron density spectrum, on-state current, subthreshold swing, I_{ON}/I_{OFF} current ratio, PDP, and intrinsic delay. Except for the on-state current, the switching characteristics are improved when using the proposed strategy. In addition, the impact of downscaling of the control gate on the swing factor and current ratio is studied, revealing a substantial enhancement when using the proposed JL CNT-TFET. The benefits of the proposed design in terms of ease of elaboration and substantial performance enhancement make the presented strategy a promising approach to improve similar ultrascaled JL TFETs based on emerging 2D nanomaterials.

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