Journal of Computational Electronics (2019) 18:1182–1191
https://doi.org/10.1007/s10825-019-01382-8

Reduction of the kink effect in a SELBOX tunnel FET and its RF/analog performance

Puja Ghosh[1] · **Brinda Bhowmick**[1]

Published online: 25 July 2019

Abstract
The kink effect in a fully depleted silicon-on-insulator (SOI) tunnel field-effect transistor (TFET) is studied and compared with the results for a SOI metal–oxide–semiconductor field-effect transistor (MOSFET) using a model that is calibrated against experimental results available in literature. A technique for eliminating the kink effect is proposed. The structure with a small gap in the buried oxide, known as the selective buried oxide (SELBOX) structure, is capable of reducing the kink effect. The impact of the kink effect on the device performance for different gap positions, thicknesses, and buried oxide thicknesses is examined. A better current–voltage characteristic is obtained for a position of the gap near the source. The effect of varying the temperature and the presence of a uniform trap charge on the kink effect for the SOI TFET, SOI MOSFET, and SELBOX structures is also studied. Various electrical parameters such as the subthreshold swing and I_{ON}/I_{OFF} ratio are investigated for the TFET in the presence and absence of uniform trap charge. Although the SELBOX structure can minimize the kink effect, it is still present for such devices with narrow and wider gaps. Therefore, the gap thickness is optimized based on technology computer-aided design (TCAD) simulations. Furthermore, radio frequency (RF)/analog performance parameters such as the transconductance (g_m), cutoff frequency (f_t), transconductance generation factor (TGF = g_m/I_D), transconductance frequency product, gain transconductance frequency product, and 1-dB compression point are investigated using TCAD simulations and compared between the SELBOX MOSFET and SELBOX TFET devices.

Keywords TFET · SOI · SELBOX · TGF · TFP · GTFP

1 Introduction

Performance concerns related to the downscaling of MOSFETs have increased interest in the use of tunnel field-effect transistors (TFETs) [1–5]. Silicon-on-insulator (SOI) devices consist of a silicon layer separated from the bulk substrate by a SiO_2 layer [6–9]. These devices are potentially competitive with bulk complementary metal–oxide–semiconductor (CMOS) devices due to their improved latch-up-free operation, improved operation speed due to the reduced gate–substrate capacitance [10, 11], and short-channel effects. They also show reduced drain-to-body and source-to-body leakage currents and thus OFF current. SOI devices can be fully depleted (FD) or partially depleted (PD) [12]. In partially depleted SOI devices, all the charges in the body do not get depleted, whereas in fully depleted SOI devices, the depletion region extends throughout the entire silicon body region [12]. The threshold voltage of fully depleted SOI devices depends on the thickness of the Si film [13].

However, several undesirable effects are associated with the use of PD SOI MOS devices, such as the kink effect in the output current–voltage characteristic [14], where the increased drain current increases the number of holes, which further increases the drain current. In the work presented herein, the kink effect for a fully depleted SOI TFET is analyzed and compared with results for a PD SOI MOSFET. In the case of the FD SOI TFET, the kink effect is observed. This effect is due to the band-to-band tunneling conduction mechanism and high source doping [15]. The conduction mechanism in the TFET is completely different. The drain current is based on the band-to-band tunneling mechanism. In the PD SOI MOSFET, a similar kink effect is

✉ Puja Ghosh
puja.ghosh93@gmail.com

Brinda Bhowmick
brindabhowmick@gmail.com

[1] Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Silchar 788010, India

observed, viz. due to the accumulation of holes in the floating body, the body potential rises and there is a reduction in the threshold voltage, which increases the drain current. Despite the remarkable improvements in FD SOI processing by foundries, PD SOI technology is still attracting much attention from foundries due to its mature process, low cost, and high performance [16]. However, in FD SOI TFETs, the kink effect is present. To investigate the kink effect in the L-shaped TFET structure, the band-to-band tunneling (BTBT) rates have been examined by two-dimensional contour plots under various front-gate voltages [17]. The kink effect is mostly due to the abrupt source doping. The kink is induced by electric field crowding around the sharp edge of the source corner [15, 18]. The problematic kink effect can be eliminated by using a SELBOX structure with a gap in the buried oxide [12]. A solution for the kink effect is discussed herein.

The remainder of this manuscript is organized as follows: Sect. 2 describes the device structure and simulation methodology. The results are depicted in Sect. 3, and Sect. 4 presents the conclusions of the work.

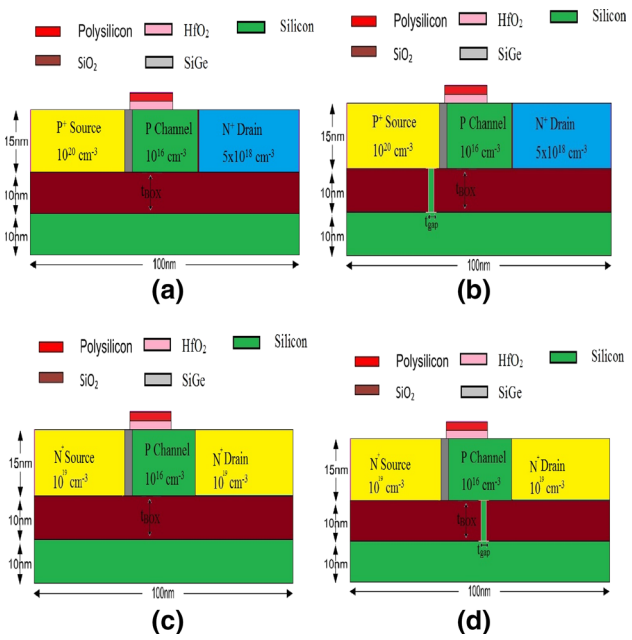

Fig. 1 A two-dimensional (2D) schematic of the proposed geometry with a SiGe (δp^+) layer near the source–channel junction

2 Device structure and simulation setup

The proposed structure of the SOI and SELBOX TFET is shown in Fig. 1a and b, respectively, while that of the MOSFET is shown in Fig. 1c and d, respectively. The devices with a δp^+ $Si_{1-x}Ge_x$ layer near the source–channel junction are designed on a SELBOX substrate. This SiGe layer can modulate the energy bandgap and tunnel width, improving the ON current [19]. Furthermore, the ON current is improved by utilizing a high-k dielectric material (HfO_2) with thickness of 2 nm as the gate oxide. The high-k dielectric material provides a higher lateral electric field at the source–channel junction, which reduces the minimum tunneling distance and improves the ON current [20]. The length of the device is 100 nm, with a source and drain of 35 nm each on a buried oxide layer with thickness of 10 nm. The channel length is 30 nm, with a 3-nm-long δp^+ $Si_{1-x}Ge_x$ layer near the source–channel junction.

The various doping specifications for the TFET are: source (1×10^{20}), channel (1×10^{16}), drain (5×10^{18}), and δp^+ layer (1×10^{18}). The doping specifications for the MOSFET are: source (1×10^{19}), channel (1×10^{16}), drain (1×10^{19}), and δp^+ layer (1×10^{18}). A gap of 2 nm is created in the buried oxide, whence the SELBOX name, as shown in Fig. 1b, d.

The Sentaurus TCAD tool is used to perform all the simulations presented herein. The high doping concentration leads to tunneling of carriers through the narrow tunneling barrier region in the TFET. Due to this bandgap narrowing, the OldSlotBoom model is activated [21]. For the highly doped source and drain, Fermi–Dirac instead of Boltzmann statistics is considered. By employing the doping-dependent mobility model, the impact of the different doping concentrations on the mobility of carriers is taken into account. The Shockley–Read–Hall recombination model as well as Schenk's band-to-band tunneling model and avalanche generation model are also considered [22]. At lower gate bias near the OFF state, Shockley–Read–Hall (SRH) generation–recombination is responsible for the exponential rise of the drain current. Further increase of the gate bias thermally excites carriers into the conduction band. However, in the enhanced gate-bias region, BTBT contributes to the drain current. Therefore, the BTBT and SRH models are the basic physics models required when simulating the TFET devices. Figure 2a and b show the effect of impact ionization (II) on the SOI TFET and SOI MOSFET, respectively. It has been suggested that impact ionization alone is responsible for the kink effect in SOI MOSFETs. However, in a TFET, BTBT makes the major contribution, as the kink is already present in a TFET even without II. Figure 2c and d depict the effects of trap-assisted tunneling (TAT) in the SOI TFET and SOI MOSFET, respectively. The current below the threshold voltage is dominated by TAT in the case of the SOI TFET [23]. In the case of the MOSFET, the TAT further enhances the kink effect with the presence of interface trap charge, due to the boosting of the electric field.

The fabrication process flow for the proposed SELBOX structure is illustrated in Fig. 3. Wafer bonding between an oxidized silicon wafer and a normal Si handle wafer

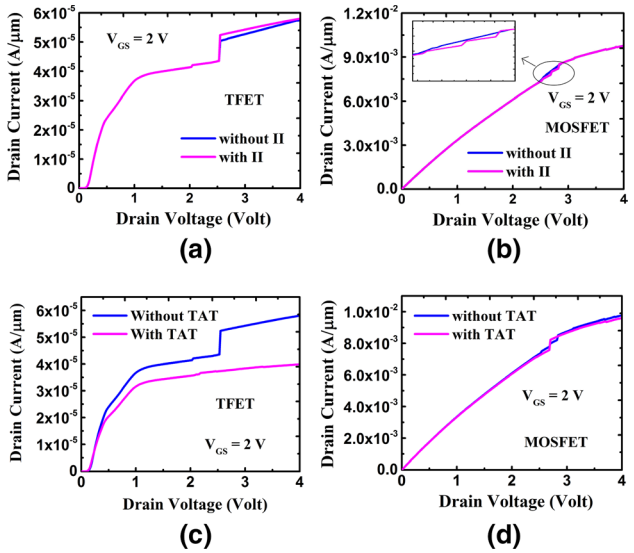

Fig. 2 The effects of impact ionization (II) in **a** the SOI TFET and **b** the SOI MOSFET, and trap-assisted tunneling (TAT) in **c** the SOI TFET and **d** the SOI MOSFET

followed by an etch-back process is used to obtain the normal SOI substrates. However, in the case of the SELBOX structures, a gap in the buried oxide is required. Such a gap can be created by using photolithography to specify the position and thickness of the gap in the oxide layer. The resulting gap can then be filled epitaxially with silicon after etching out the unwanted oxide. Extremely thin films are widely recognized for their potential for end-of-roadmap transistors projected in the International Technology Roadmap for Semiconductors (ITRS). SOI substrate fabrication based on Smart Cut™ technology has been developed to ensure that high-quality substrates are commercially available [24]. After this step, the already processed wafer can be bonded with the handle wafer. The silicon grown epitaxially on the very narrow trenches will definitely create defects in the gap, and these defects will result in electron trapping and detrapping mechanisms, which will further reduce the current in the device. Calibration of the numerical simulation models is performed using the experimental results obtained for a fabricated SOI TFET by Biswas et al. [25] and an SOI MOSFET by Toshiaki et al. [26]. The calibration graphs are plotted at $V_{DS}=0.5$, 1, and 1.2 V for the SOI TFET in Fig. 4a and at $V_{DS}=0.5$ V for the SOI MOSFET in Fig. 4b.

3 Results and discussion

3.1 The kink effect in the SELBOX structure

The output characteristics are plotted for various thickness of the SELBOX while keeping the gap thickness fixed at 0.5 nm. There is a significant dependence of the kink effect on the thickness of the SELBOX, as observed in Fig. 5a. When the thickness of the SELBOX is varied, there is a variation in the gap resistance, where the SELBOX thickness (t_{BOX}) is the length of the resistance and the gap thickness is the width of the resistance. With an increase in t_{BOX}, there is an increment in the gap resistance, which increases the body potential. As a result, the kink effect occurs at lower drain voltage. The maximum kink effect is observed for t_{BOX} of 15 nm, and it reduces with a reduction of t_{BOX}.

Figure 5b shows the output characteristics of the proposed structure for various positions of the gap in the SELBOX while keeping the gap thickness fixed at 0.5 nm. The kink effect is mostly observed when the gap is near the drain, while it is almost negligible when the gap is near the source.

In an *n*-TFET, the source is *p*-type and the conduction mechanism is band-to-band tunneling of electrons from the source to channel. The holes (generated by band-to-band tunneling of holes at the channel–drain junction) near the tunneling junction can easily flow through the narrow gap near the source compared with that near the drain. A gap near the source (25–27 nm), away from the tunneling junction, results in a greater kink effect compared with a position of the gap near the source (31–33 nm), close to the tunneling junction, due to the easy flow of holes in the latter compared with the former case. Thus, a gap near the drain provides high resistance with a sharp kink in the output characteristics. The gap in the SELBOX provides a conduction path for holes from the tunneling junction to the substrate. As the thickness of the gap is increased, more holes created near the tunneling junction can flow to the substrate, which reduces the potential drop across the gap, so the associated threshold voltage increases. Thus, with an increment in the thickness of the gap, the kink effect is reduced. As the gap thickness is reduced, the device behaves as a fully depleted SOI structure with no gap in the SELBOX. Figure 5c shows that the minimum kink effect is observed for the device with a gap thickness of 2 or 4 nm. The drain current reduces for a gap thickness of 4 nm, as the device behaves as a bulk TFET for larger gap thickness. Thus, the best result is obtained for a gap thickness of 2 nm. For the structure with no gap in the buried oxide, the accumulated holes in the floating body increase the body potential and reduce the threshold voltage, which increases the drain current.

The output characteristics of the SOI TFET and SELBOX TFET are shown in Fig. 6a. It is noted that the kink effect is present for the SOI TFET but not the SELBOX TFET, similar to the MOSFET, as shown in Fig. 6b. The presence of the kink in the output characteristics of the SOI MOSFET is clearly visible. There is no kink effect for the SELBOX device with a gap of 2 nm at various gate-to-source voltages, as shown by the dotted lines. The voltage at which the kink effect is observed, i.e., the kink voltage, increases with an

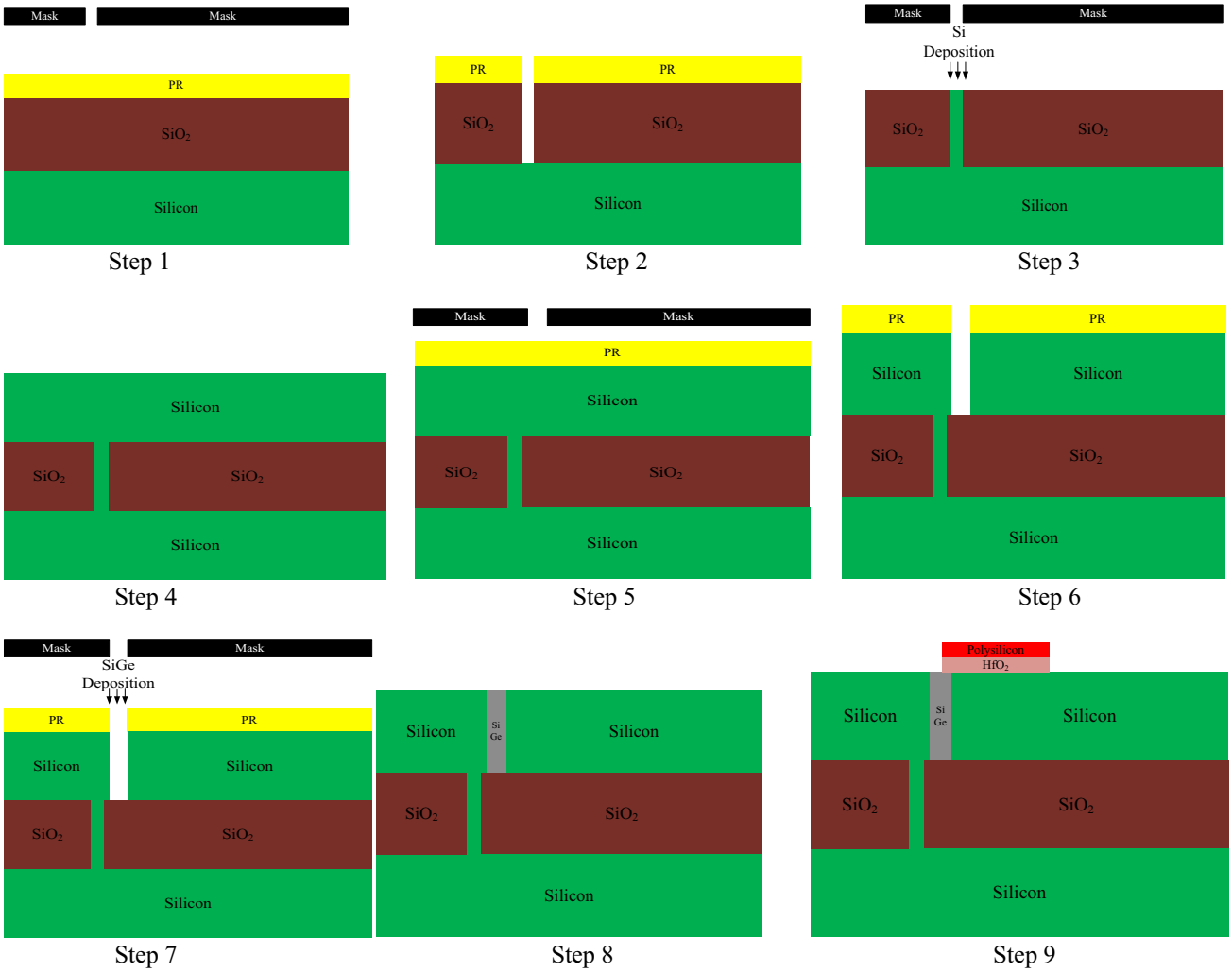

Fig. 3 The fabrication process flow for the proposed SELBOX device

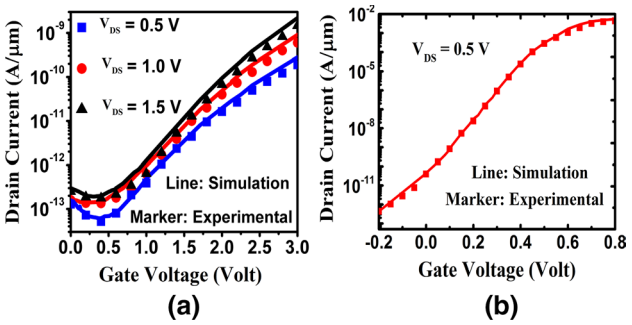

Fig. 4 The calibration of the simulated graph versus an experimental graph for **a** the SOI TFET and **b** the SOI MOSFET

increase in the gate-to-source voltage in the case of the SOI MOSFET.

Figure 7a shows the band-to-band (BTB) generation rate at $V_{GS} = 1.4$ V and $V_{DS} = 2.5$ V for the SELBOX TFET, while Fig. 7b shows the band-to-band generation rate for the SOI TFET at the same values of V_{GS} and V_{DS}. The kink is mostly induced by electric field crowding around the sharp edge of the source corner [15, 18] of the SOI TFET, which is clearly observed due to the high BTB generation rate. Therefore, the crowding of the electric field at the source corner of the source–channel junction of the TFET is the main reason for the kink effect.

The hole current density is used to measure the hole current across the gap region in the SELBOX device. With an increase in the drain voltage, the electric field increases and holes near the drain can easily tunnel through the barrier near the drain–channel junction. Thus, the hole current increases with an increase in the drain voltage, as shown in Fig. 8a. The resistance of the narrow gap region is greater compared with that of the body region of the device. A potential is developed across the narrow gap in the SELBOX as holes flow through this gap resistance.

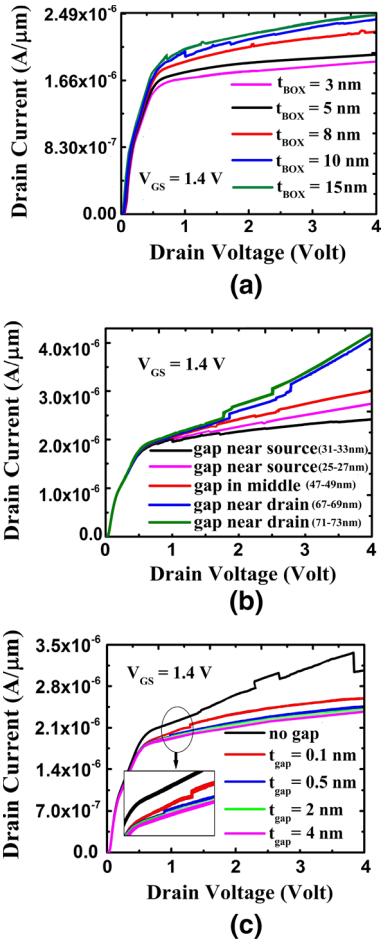

Fig. 5 The output characteristics for different thicknesses of SELBOX, and the position and thickness of the gap at $V_{GS} = 1.4$ V

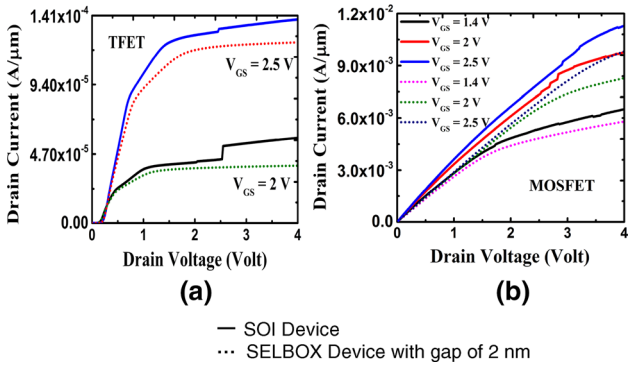

Fig. 6 The output characteristics of the TFET and MOSFET for different gate voltages

This potential leads to an increment in the body potential, as shown in Fig. 8b.

Figure 9a shows the hole current density which leads to the kink in the current–voltage characteristics. The device

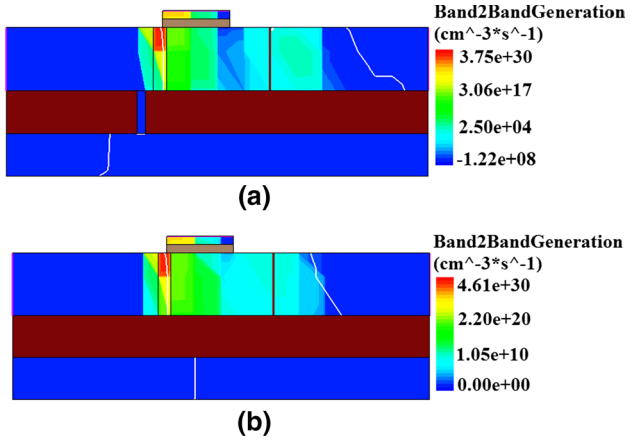

Fig. 7 Two-dimensional contour plots of the BTBT rates at $V_{GS} = 1.4$ V and $V_{DS} = 2.5$ V for **a** the SELBOX (2 nm gap) TFET and **b** the SOI TFET

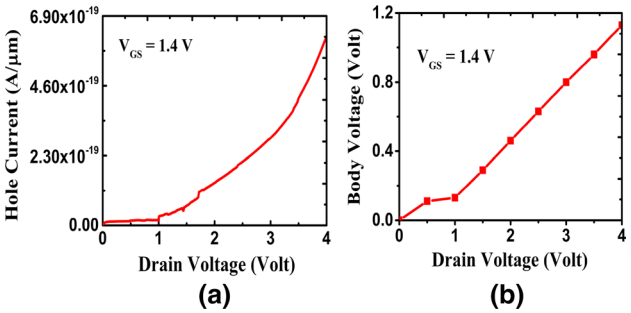

Fig. 8 The kink effect in the SELBOX TFET

with a very small gap width behaves like a SOI device, as the holes are unable to drain to the substrate. It is observed from Fig. 9b that, as the gap width increases in the SELBOX, the hole density near the source region reduces, a greater number of holes drain to the substrate, and the kink voltage increases. The BTBT generation rate for different thicknesses of the gap is shown in Fig. 9c. At a kink voltage of 1 V, the BTBT rate of the device with a gap thickness of 0.5 nm is greater than that with a gap thickness of 2 nm, indicating an enhancement of the current for a gap with thickness of 0.5 nm.

For different gap thicknesses, the change in the body potential with the hole current density is plotted in Fig. 10a. The reduction in the slope of the line with an increment in the gap thickness indicates a lowering of the gap resistance. The rise in the body potential is reduced, and the kink effect is eliminated. The gap resistance is plotted versus t_{box}/t_{gap}, where t_{box} is the oxide thickness and t_{gap} is the oxide gap thickness, in Fig. 10b. For large oxide gap thickness, the resistances across the gap have reduced values, which do not increase the body voltage by

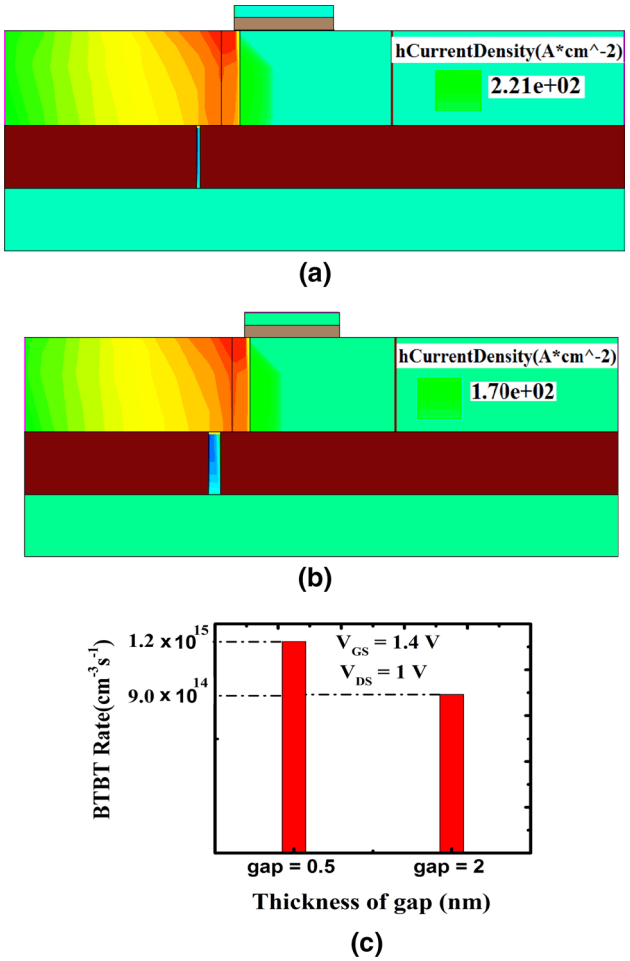

Fig. 9 The hole current density in the SELBOX TFET for a gap of width **a** 0.5 nm and **b** 2 nm, and **c** the BTBT rate at the tunneling junction

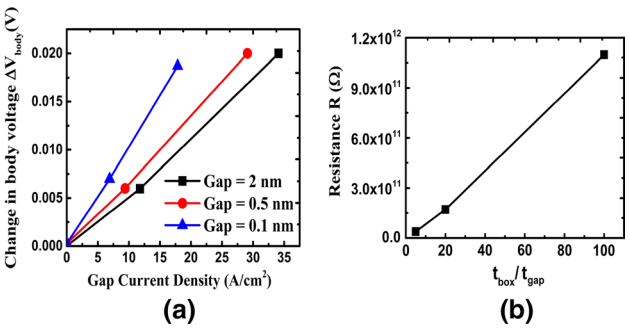

Fig. 10 Plots of **a** the change in the body potential versus the gap current density and **b** the gap resistance versus t_{box}/t_{gap}

a considerable amount, thus the kink effect is reduced. A reduction in the oxide gap thickness leads to an increment in the gap resistance, and the hole transport increases the body potential. The kink effect is observed at lower drain voltages. The flow through the gap to the substrate leads to a change in the body potential ΔV_{body}, which is related to the hole current by Eq. (1):

$$\Delta V_{body} = R_{gap} I_h, \tag{1}$$

where R_{gap} is the gap resistance.

3.2 The impact of the temperature on the kink effect

There is a weak dependence of the TFET on temperature because the conduction mechanism is BTBT. The drain current is related to temperature through the energy bandgap term in the expression for the tunneling current [27]:

$$I_{DS} = A \frac{|E|^2}{E_g^{1/2}} \exp\left(-\frac{B E_g^{3/2}}{|E|}\right), \tag{2}$$

where E is the electric field, E_g is the bandgap, and A and B are material-dependent parameters whose default values are defined in the simulator [27]. The bandgap (E_g) is related to temperature as

$$E_g(T) = E_g(300) - \frac{\alpha T^2}{T + \beta}, \tag{3}$$

where $\alpha = 4.73 \times 10^{-4}$ eV/K and $\beta = 636$ K and $E_g(300) = 1.08$ eV for silicon.

With an increase of the temperature, bandgap narrowing occurs and the tunneling current increases. The kink voltage increases with increase of the temperature; i.e., at the low temperature of 300 K, the kink occurs at low drain voltage, whereas at higher temperatures, the kink occurs at high drain voltage, as shown in Fig. 11a. As the temperature is increased, the kink voltage shifts towards higher drain voltage values.

In the MOSFET at low gate voltage, the drain current depends on the temperature through the square of the intrinsic carrier concentration term [27]:

$$n_i = N_a N_d \exp\left(-\frac{E_g}{2KT}\right). \tag{4}$$

At high gate voltage, with an increase of the temperature, the mobility is reduced due to lattice scattering and the drain current decreases. As the temperature is increased, the kink effect increases and the abnormality due to the kink effect occurs at high drain voltage, as observed in Fig. 11b.

3.3 The impact of traps on the kink effect

Acceptor-type charge traps at the source–channel junction pull the energy bands and reduce the band-to-band tunneling (BTBT) current [28].

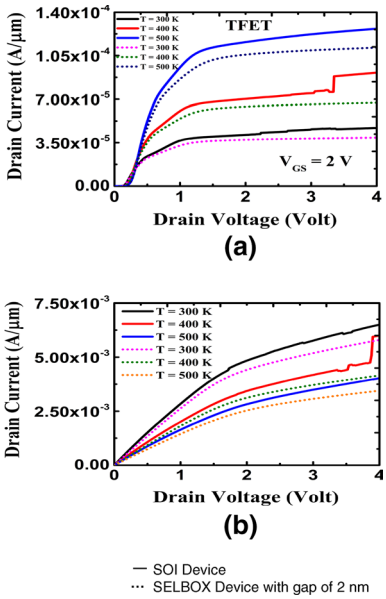

Fig. 11 The impact of the temperature on the I_D–V_{DS} characteristics of **a** the TFET and **b** the MOSFET

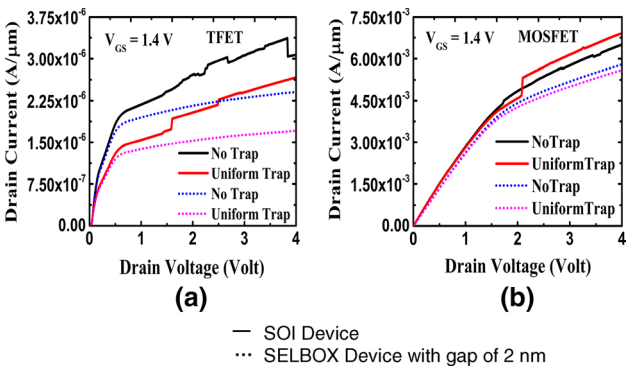

Fig. 12 The I_D–V_{DS} characteristics of **a** the TFET and **b** the MOSFET in the presence and absence of uniform traps

In the presence of traps, the drain current decreases in the case of both the SOI and SELBOX TFET, as shown in Fig. 12a. Due to the traps, more carriers are accumulated, which increases the body voltage and the kink effect occurs at low drain voltage in the SOI structure. In the presence of traps, the kink effect increases in the MOSFET, as observed in Fig. 12b, similar to the TFET. Comparing Fig. 12a and b, the kink effect is enhanced in the SOI MOSFET compared with the SOI TFET in the presence of uniform traps. The subthreshold swing (SS) and I_{ON}/I_{OFF} ratio of the SELBOX TFET in the presence and absence of uniform traps are compared with the values for the SOI TFET in Table 1.

Table 1 The extracted parameter values

	Device	No traps	Uniform traps
SS	SOI TFET	49	67
	SELBOX TFET	48	65
I_{ON}/I_{OFF}	SOI MOSFET	3.05×10^{13}	1.35×10^{12}
	SELBOX TFET	6×10^{13}	1.5×10^{12}

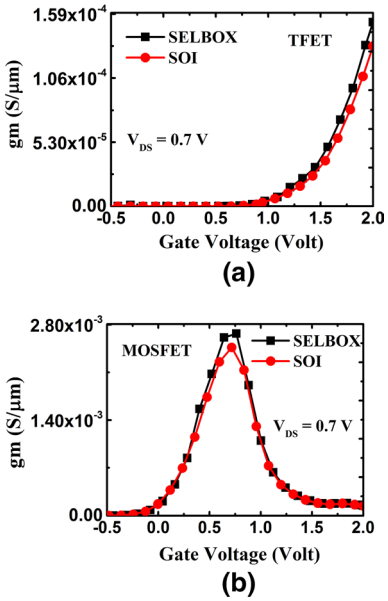

Fig. 13 The variation of the transconductance with the gate voltage for **a** the TFET and **b** the MOSFET

3.4 RF analysis

The transconductance $\left(g_m = \partial I_D / \partial V_{GS}\right)$ of all the proposed structures is shown in Fig. 13a, b. In the TFET, due to the better electrical coupling of the gate and tunneling region, the electron tunneling through the source–channel junction increases, which leads to an enhancement of g_m with the gate voltage. After attaining a certain peak, g_m reduces with the gate voltage due to degradation of the mobility caused by enhanced scattering in the MOSFET. The influence of the mobility is more significant in the MOSFET compared with the TFET. For both the SELBOX and SOI structures, the variation in g_m is not observable.

An important RF parameter is the cutoff frequency (f_T) at which the short-circuit current gain becomes unity [29]. It is related to the transconductance (g_m) and the gate-to-gate capacitance (C_{gg}) as [30]

$$f_T = \frac{g_m}{2\pi C_{gg}}. \tag{5}$$

The variation of the cutoff frequency (f_T) with the gate voltage for the TFET and MOSFET is shown in Fig. 14a and b, respectively. For both the TFET and MOSFET structures, the cutoff frequency of the SELBOX device is slightly greater compared with the SOI device, because f_T is proportional to g_m, which is slightly higher in the SELBOX devices.

One of the significant RF parameters is the transconductance generation factor (TGF) or transconductance-to-current ratio (g_m/I_{ds}). It can be observed from Fig. 15 that, with an increase in the gate voltage, the TGF reduces, as at higher gate voltages, the drain current saturates to a particular value and the change in the drain current is insignificant. At low gate voltages, the TGF of the SELBOX structure is higher than that of the SOI structure because the OFF current of the SOI is greater due to the presence of floating body effects [31]. At high gate voltages, the TGF of the two structures is comparable.

The transconductance frequency product $\left(\text{TFP} = g_m f_t / I_D\right)$ is a very significant parameter for high-speed applications [32–34]. The variation of the TFP with the gate voltage is shown in Fig. 16. As for g_m and f_T, the TFP is also enhanced with the gate voltage in the TFET. The TFP shifts towards high gate voltage in the SOI MOSFET, indicating lesser mobility degradation.

A unique figure of merit to determine the overall performance of the device is the GTFP, i.e., the product of the gain, transconductance, and frequency: $\left(\text{GTFP} = \left(g_m / g_d\right) \times \left(g_m / I_D\right) \times f_t\right)$. The change in the GTFP with the gate voltage is shown in Fig. 17. The SELBOX structure exhibits a higher GTFP compared with the SOI device.

To describe the capability of a device fully, it is essential to analyze its linearity. The distortion at the output will be lesser if the linear parameters have high values. Use of a physics-based TCAD device simulator supports detailed

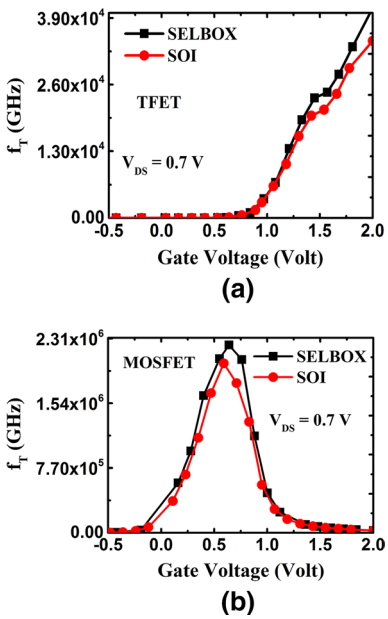

Fig. 14 The variation of the cutoff frequency with the gate voltage for **a** the TFET and **b** the MOSFET

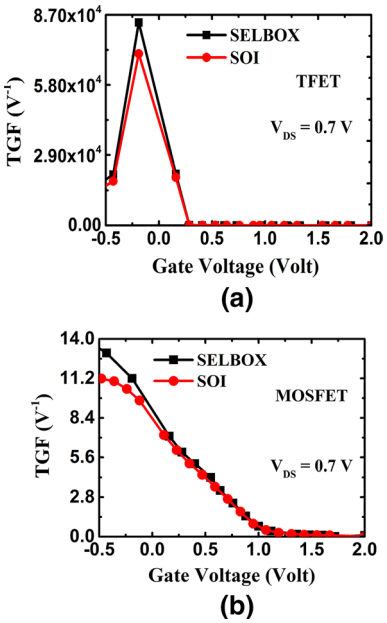

Fig. 15 The variation of the TGF with the gate voltage for **a** the TFET and **b** the MOSFET

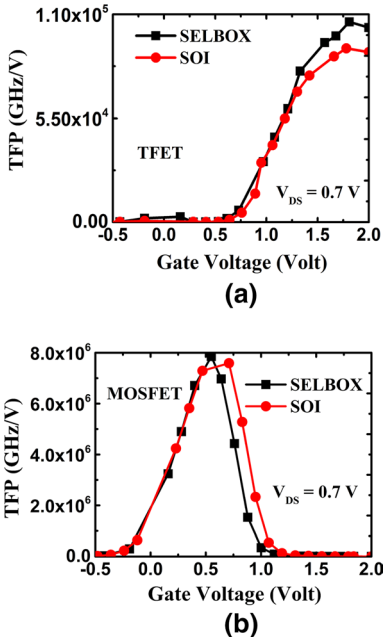

Fig. 16 The variation of the TFP with the gate voltage for **a** the TFET and **b** the MOSFET

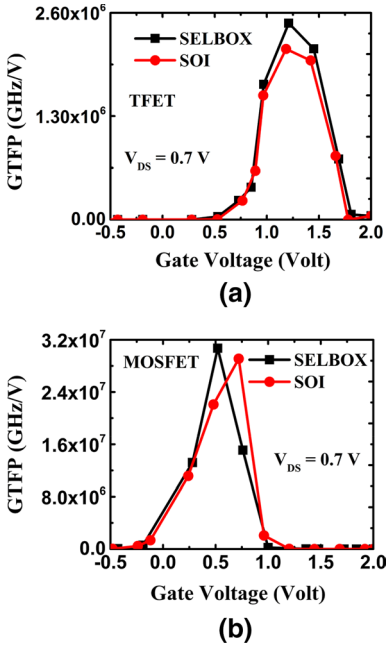

Fig. 17 The variation of the GTFP with the gate voltage for **a** the TFET and **b** the MOSFET

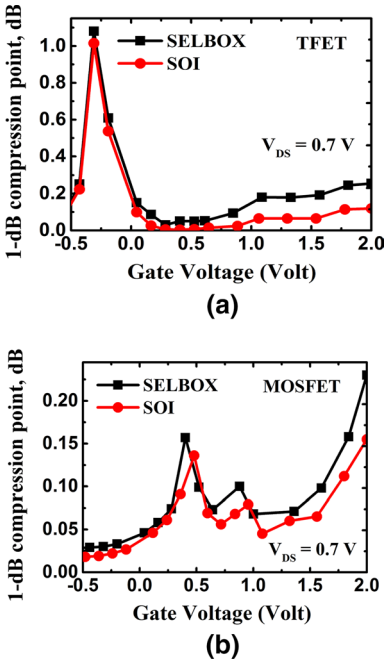

Fig. 18 The 1-dB compression point of **a** the TFET and **b** the MOSFET

analysis of newly used models for linearity [35]. The higher-order derivatives of the transfer characteristic (I_D–V_G) with respect to the gate voltage are used to measure the nonlinearity of the device. The 1-dB compression point is a significant figure of merit to measure the upper limit of linear operation [36]. It indicates the input power at which the output power deviates from linearity by 1 dB, expressed as

$$1\,\text{dB compression point} = 0.22\sqrt{g_m/g_{m3}}. \quad (6)$$

The effect of the device structure on the 1-dB compression point is shown in Fig. 18. The SELBOX structure of both devices at high gate biases shows higher values of the 1-dB compression point compared with the SOI structure, indicating superior linearity performance of the SELBOX structure. High values of the 1-dB compression point improve the high input power capability of such devices for use in amplifier applications.

4 Conclusions

A kink is observed in the output current–voltage characteristics of the FD SOI TFET. Due to the accumulation of holes in the floating body of the device, there in an abrupt rise in the drain current, known as a kink. In the FD SOI TFET, the kink effect arises due to abrupt source doping as BTBT is the conduction mechanism in the TFET. The abnormality observed in the output characteristics can be eliminated by using a very narrow gap in a SELBOX layer. The variations in the kink effect with the SELBOX thickness and gap thickness are investigated. The dependence of the gap resistance and the body potential on the gap thickness is investigated. For large gap thickness in the SELBOX, the gap resistance reduces and holes can be transported easily through the gap without increasing the body potential to a considerable value, thus minimizing floating body effects. Furthermore, the effects of temperature and traps are examined. It is observed that the kink voltage increases with an increase of the temperature and the effect of uniform traps degrades the drain current. Moreover, the kink effect increases in the SOI devices (TFET and MOSFET) in the presence of traps. Furthermore, the cutoff frequency of the SELBOX MOSFET is greater compared with the TFET. The TGF and GTFP of the SELBOX structures are better, indicating superior linearity performance. The region of best analog/RF performance is obtained near the ON state for the TFET and in close vicinity to the threshold voltage for the MOSFET.

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