Journal of Computational Electronics (2019) 18:856–863
https://doi.org/10.1007/s10825-019-01345-z

Design and performance analysis of low-power SRAM based on electrostatically doped tunnel CNTFETs

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Published online: 11 May 2019

Abstract
An electrostatically doped (ED) tunnel carbon nanotube field-effect transistor (CNTFET)-based six-transistor (6T) static random-access memory (SRAM) cell is designed and simulated in HSPICE. The performance of the ED tunnel CNTFET 6T SRAM cell is analyzed based on various figures of merit (FOMs), viz. the read/write noise margin, power dissipation, and read/write delay. Simulation results for the ED tunnel CNTFET-based 6T SRAM are compared with those for a conventional CNTFET-based 6T SRAM cell, revealing that the former shows improved FOMs without losing stability. The read noise margin is improved by 9.2% and 7.5% at V_{DD} of 0.9 V and 0.5 V, while the write noise margin is improved by 16% and 14% at V_{DD} of 0.9 V and 0.5 V, respectively. The power dissipation is reduced by 9 pW at V_{DD} of 0.9 V and by 4 pW at V_{DD} of 0.5 V. The results demonstrate the stability of the proposed ED tunnel CNTFET SRAM for low-power applications.

Keywords Carbon nanotube field-effect transistor (CNTFET) · Static RAM (SRAM) · HSPICE · Low power · Read noise margin · Write noise margin

1 Introduction

Power consumption due to leakage in memory is a major issue in nanometer-scale technologies. As most of the area of a processor chip is occupied by SRAM, its dissipation is significant. Thus, extensive research has been performed to develop low-power on-chip memory to reduce the total power dissipation. The dynamic power has a quadratic dependence on the supply voltage. Hence, to reduce the dynamic power dissipation, the supply voltage must be scaled down. However, according to the International Technology Roadmap for Semiconductors (ITRS) standard, along with the supply voltage, the threshold voltage must also be scaled down. To reduce the threshold voltage, thinner gate oxide can be employed, but this also increases the gate oxide tunneling and subthreshold leakage currents [1–6]. To address this issue, several materials and new devices have been explored to provide steep subthreshold slope (SS) and lower leakage current. A steep subthreshold slope increases the switching speed of the transistor and enables low-voltage operation. The tunnel CNTFET offers a steep subthreshold slope and thus can work efficiently at low voltages [7, 8]. The structure of the tunnel CNTFET is similar to that of an Si-based tunnel FET, with the only difference being the channel material [9, 10]. The best feature of CNTs is their variable bandgap, which makes them suitable for use in various applications [11]. Conventional doping is not possible in tunnel CNTFETs, because if any carbon atom is replaced with a dopant, the overall properties of the CNT change. Therefore, fabrication of tunnel CNTFETs is a difficult task with considerably higher costs [12]. To reduce this difficulty in fabrication, a dopingless approach was introduced in 2005 [13, 14]. This technique offers the supplementary advantage of dynamic configuration [15, 16], allowing the same device to be used as both *n*-type and *p*-type by reversing the bias applied at the polarity gates (PGs). An overview of work done on such electrostatically doped devices is presented in Ref. [17].

In the literature, SRAM circuits have been designed using both complementary metal–oxide–semiconductor (CMOS) and conventional CNTFET technologies [14, 18–21]. Herein, an electrostatically doped tunnel CNTFET-based SRAM cell is subjected to exhaustive analysis to determine the impact on its performance parameter, viz. read/write

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noise margin, power dissipation, and read/write delay. The *I–V* transfer characteristics of the ED tunnel CNTFET are compared with those of a conventionally doped CNTFET to confirm its suitability for use in circuit applications. The 6T SRAM cell is designed and simulated in HSPICE using both conventionally doped and ED tunnel CNTFETs. The conventional CNTFET 6T SRAM cell is designed using the model file from Stanford University [22], whereas the proposed ED tunnel CNTFET-based SRAM cell is designed using the model in Ref. [23], revealing improvements compared with the conventional CNTFET-based SRAM in terms of the power dissipation, read/write delay, and static noise margins (SNMs) without losing stability.

2 ED tunnel CNTFET

A schematic of the ED tunnel CNTFET is shown in Fig. 1, with two polarity gates (PG-1 at the source region, PG-2 at the drain region) and primary gates at the top and bottom. The doping is controlled electrostatically by varying the voltages applied at the polarity gates PG-1 and PG-2. The polarity gates help to create a *p*-region at the drain when applying a polarity voltage of −0.75 V and an *n*-region at the source side when applying a polarity voltage of 0.75 V. The purpose of the primary gates is to control the flow of current. The device configuration can thus be changed from *p*-type to *n*-type by reversing the voltages applied at the polarity gates. Figure 2 shows the I_{DS}–V_{GS} characteristics of the *n*-type (Fig. 2a) and *p*-type (Fig. 2b) ED tunnel and conventionally doped CNTFETs [8, 23]. The simulation results for both models show that the ED tunnel CNTFET exhibits improved I_{DS}–V_{GS} performance compared with the conventionally doped CNTFET in terms of low OFF-current, steep SS, and high ON/OFF-current as compared with the conventional CNTFET (Table 1).

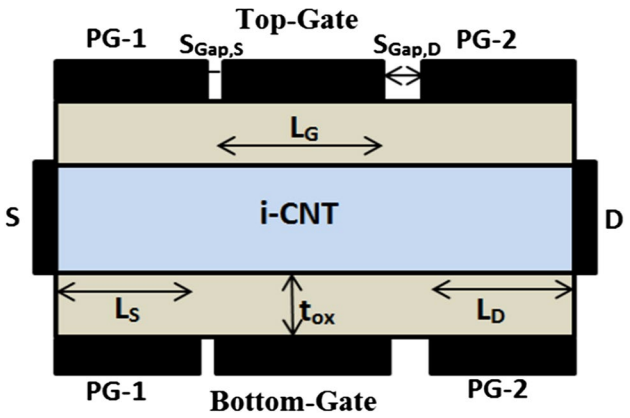
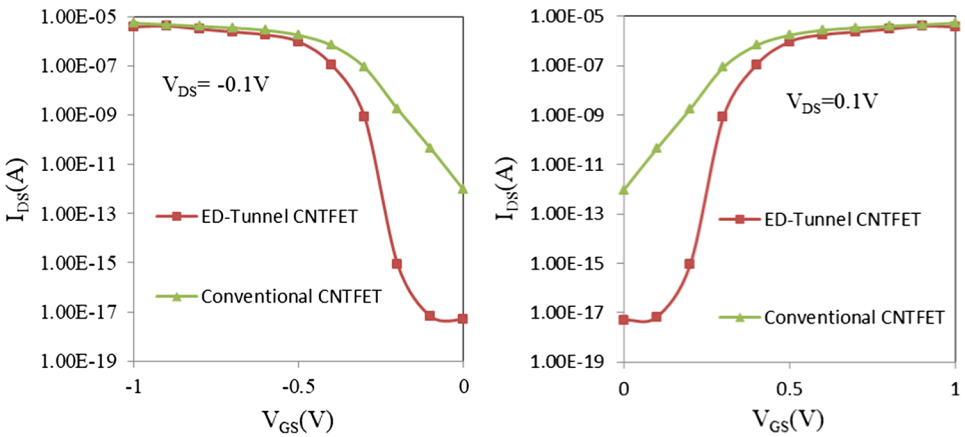


Fig. 1 The structure of the ED tunnel CNTFET with polarity gates

Table 1 Values of the device parameters for the ED tunnel CNTFET [8]

Parameter	Value in the ED tunnel CNTFET
Diameter (d)	1 nm
Oxide thickness (t_{ox})	1 nm
Metal workfunction	4.1 eV
Channel length (L_G)	20 nm
Source (L_S)	20 nm
Drain (L_D)	20 nm
Polarity gate voltage (PG-1)	0.75 V
Polarity gate voltage (PG-2)	−0.75 V
Drain spacer gap ($S_{GAP,D}$)	10 nm
Source spacer gap ($S_{GAP,S}$)	2 nm

Fig. 2 The I_{DS}–V_{GS} characteristics of the ED tunnel CNTFET [23]



(a) P-type ED-Tunnel CNTFET **(b)** N-type ED-Tunnel CNTFET

3 CNTFET and ED tunnel CNTFET 6T SRAM cells

The basic 6T SRAM cell consists of two cross-coupled inverter pairs in which the output node of one inverter pair is connected to the input node of the second inverter pair. The inverter pairs M1, M2 and M3, M4 are further connected to two access transistors, M5 and M6. The read or write operation is performed by applying appropriate voltages to the word lines (WL) and bit lines (BL) of the access transistors. The gate terminals of these access transistors are connected to the WL, while the drain terminals are connected to the bit lines (BL and BLB). The original and complementary data values are stored at the nodes Q and QB. A schematic diagram of the 6T SRAM cell using conventional CNTFETs is shown in Fig. 3.

Figure 4 shows a schematic diagram of the 6T SRAM cell using ED tunnel CNTFETs, adopted from Ref. [24] by replacing all the Si-based TFETs with ED tunnel CNTFETs. It includes both inward and outward access transistors. The inward access configuration is adopted to obtain an acceptable read noise margin for the device, whereas the outward access configuration is used to increase the write noise margin of the device. The inward access transistor couples the internal node Q to BL, while the outward access transistor couples the internal node Q to BLB. The write enable signal (WR_A) is used to provide virtual grounding to an inverter pair in order to obtain an acceptable write noise margin. The conventional CNTFET-based 6T SRAM cell is designed and simulated as reported in Ref. [18], then to further reduce fabrication issues, the novel dopingless tunnel CNTFET is used to design the model for the 6T SRAM design. The cell design of the 6T SRAM using ED tunnel CNTFETs is

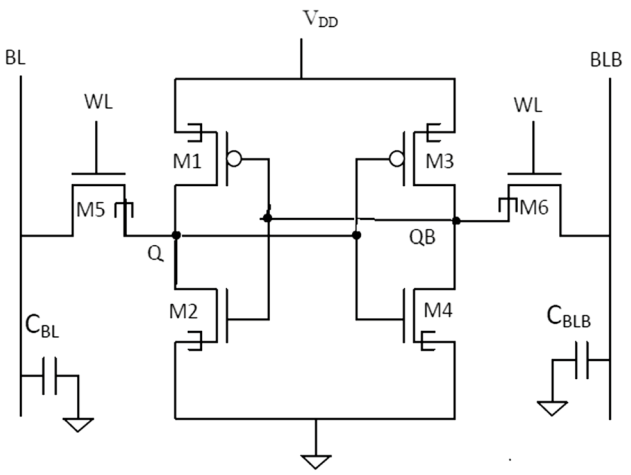


Fig. 3 A schematic diagram of the 6T SRAM cell using conventional CNTFETs

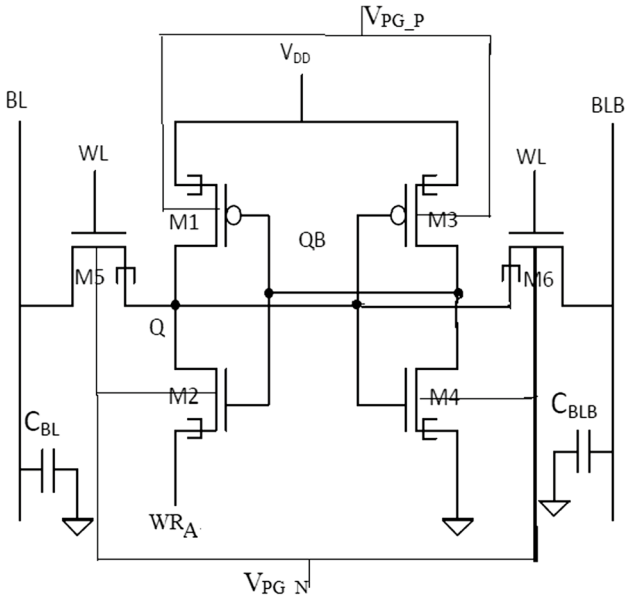


Fig. 4 A schematic diagram of the 6T SRAM cell using ED tunnel CNTFETs

the same as that of the conventional SRAM cell but with additional polarity gate biases (BL and BLB), both of which are connected to node Q through M5 and M6. The voltage applied at the polarity gates is V_{PG_p} (for p-type) = −0.75 V and V_{PG_p} (for n-type) = 0.75 V.

4 The read operation in SRAM

For the read operation, both bit lines (BL and BLB) are precharged to the supply voltage, i.e., V_{DD}, while the word line is activated. If the value stored at Q is 1, then it will remain at 1 because a discharge path is absent. If the storage node (Q) is storing a value of 0, then it will immediately switch to an intermediate voltage because a current path now exists between the bit line and ground. The value of this intermediate voltage is determined by the voltage dividers, which are constructed by using one access transistor and one pull-down transistor. The intermediate voltage should not cross the threshold voltage of the inverter, otherwise the voltage at the internal node will flip, which is undesired. So, for a successful read operation, the pull-down transistor must be stronger than the access transistor. In other words, the cell ratio (β) should be high, as expressed in Eq. (1). The difference between the bit line (BL) and Q is sensed by the sense amplifier and will indicate that the read 0 operation has been performed. The read operation of the 6T SRAM cell using ED tunnel CNTFETs is similar to that for the 6T CNTFET SRAM cell. During the read operation, WR_A is

driven to ground and the read current path is the same as illustrated in Fig. 5.

$$\beta = \frac{\left(\frac{W}{L}\right)\text{ratio of } N/P \text{ transistor}}{\left(\frac{W}{L}\right)\text{ratio of access transistor}}. \quad (1)$$

5 The write operation in SRAM

The write operation in the ED tunnel CNTFET SRAM cell is shown in Fig. 6. The write operation is performed through the access transistors M1 and M5. The voltage levels are applied to the bit lines according to the data that is to be written.

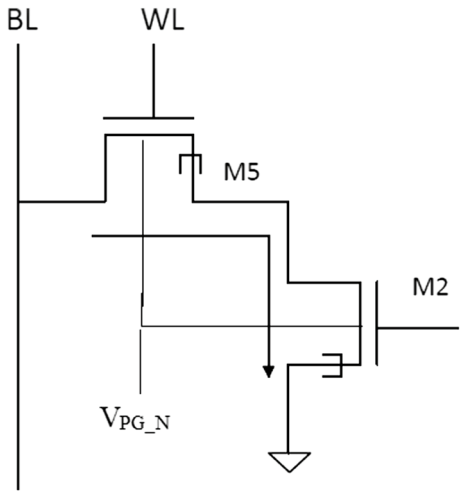


Fig. 5 The read current path

To write a value of 1 onto the internal node Q, BL and BLB are raised to V_{DD}, then the word line is activated. To weaken the first inverter, WR_A is raised simultaneously as well. The WR_A signal is sent in the form of a short pulse whose magnitude is less than the supply voltage but greater than the ground voltage. When Q settles to 1 and QB settles to 0, WR_A is linked to the ground line, which enables cross-coupling between the two signals. Figure 6a shows the write 1 operation.

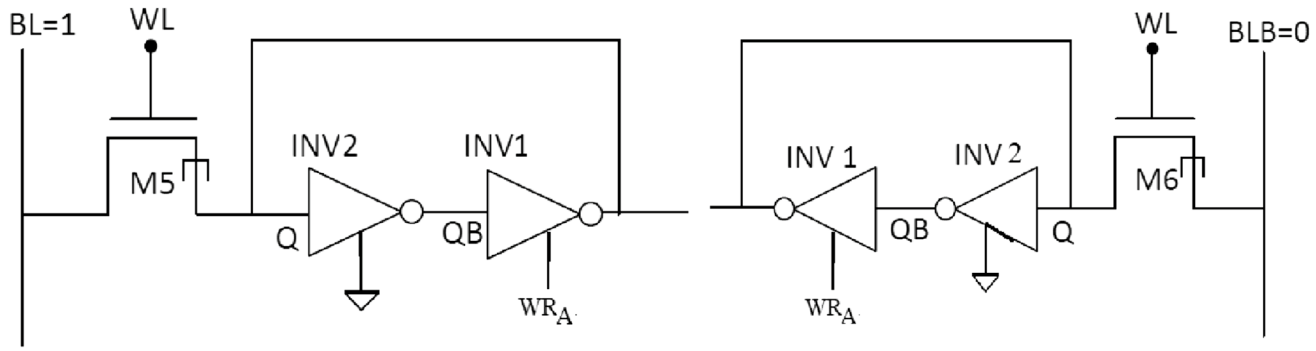
To write a value of 0 onto Q, both bit lines are pulled to the ground voltage and the access transistors are activated. WR_A is raised to break the cross-coupling of the inverters. Q is discharged to 0 by the access transistor M6. Figure 6b shows the write 0 operation.

6 SRAM performance parameters

The performance of SRAM is generally compared on the basis of the read and write margins, power dissipation, and read and write delays.

6.1 Read SNM

The read noise margin is calculated using the read voltage transfer characteristic (VTC), which is measured by sweeping the direct-current (DC) voltage at node Q while monitoring the voltage at node QB. It is then calculated based on the largest square that fits within the lobes of the read butterfly curve. The read margin of the conventional CNTFET SRAM cell and the proposed ED tunnel CNTFET SRAM cell at V_{DD} of 0.9 V is illustrated in Fig. 7a, b, and at V_{DD} of 0.5 V in Fig. 8a, b. Note that the VTC of the proposed structure is very sharp compared with that of the conventional CNTFET SRAM, leading to an enhancement of the read margin. A 9.2% improvement in the read margin is seen at 0.9 V, and 7.5% at 0.5 V.



(a) Write '1' operation **(b)** Write '0' operation

Fig. 6 The write operation of the 6T SRAM cell using ED tunnel CNTFETs

6.2 Write SNM

The write noise margin is measured based on the smallest square that fits within the lower part of the VTC between Q and QB under the condition of WL = V_{DD}, BL = 0, and BLB = V_{DD} [25]. The write margin of the conventional CNTFET 6T SRAM and ED tunnel CNTFET 6T SRAM at V_{DD} of 0.9 V is shown in Fig. 9a, b, and at V_{DD} of 0.5 V in Fig. 10a, b. The ED tunnel CNTFET 6T SRAM exhibits a sharp transition in the VTC, which improves the write

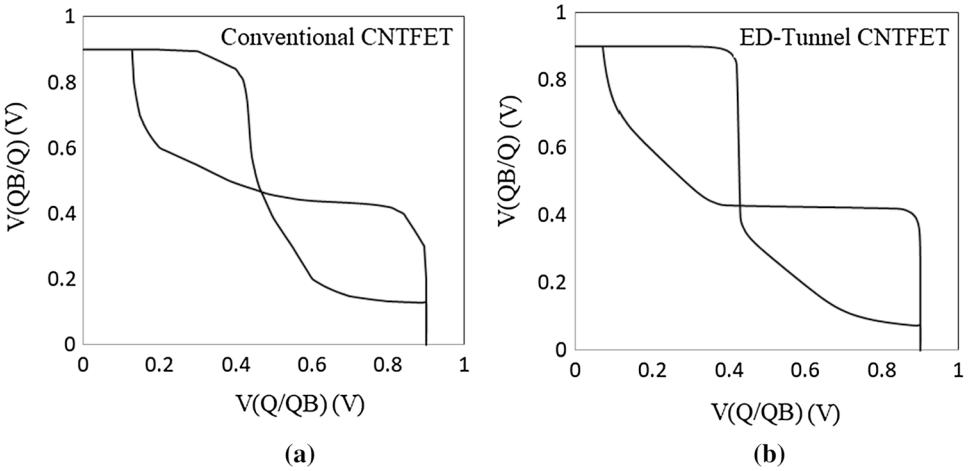


Fig. 7 A comparison of the read SNM between the **a** conventional CNTFET and **b** ED tunnel CNTFET at V_{DD} = 0.9 V

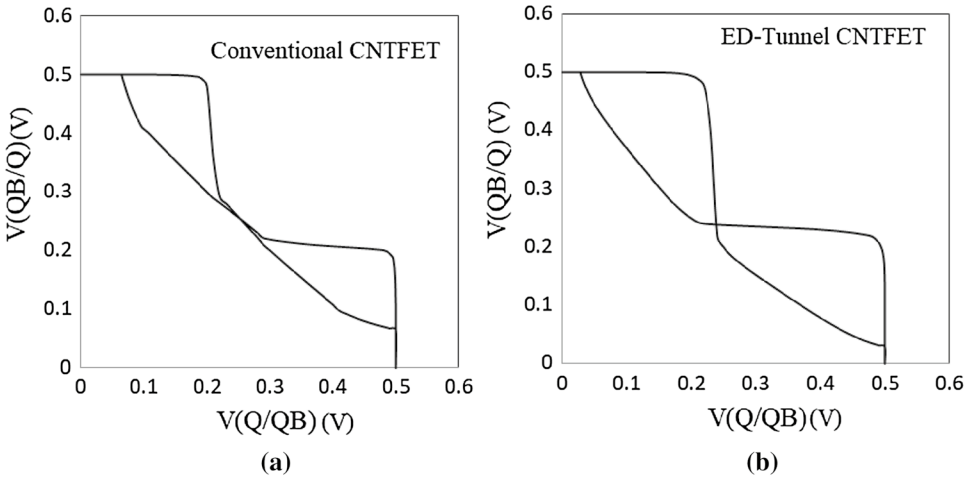


Fig. 8 A comparison of the read SNM between the **a** conventional CNTFET 6T SRAM and **b** ED tunnel CNTFET 6T SRAM at V_{DD} = 0.5 V

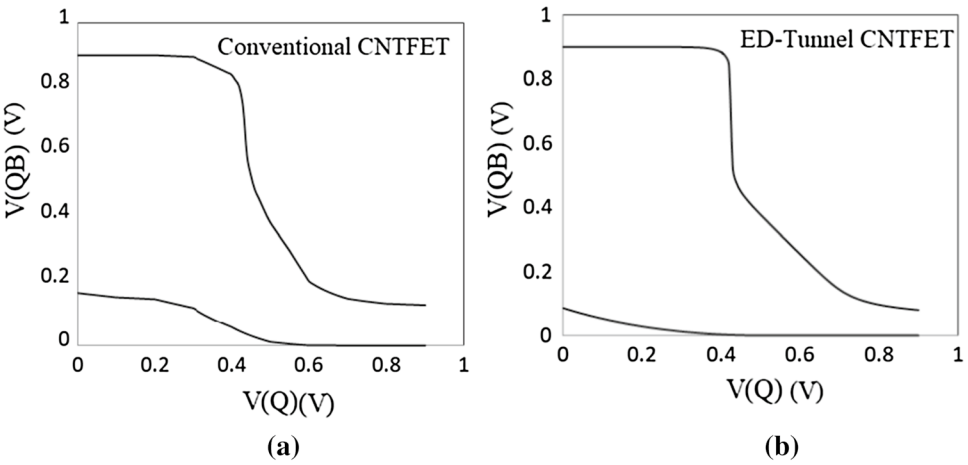


Fig. 9 A comparison of the write SNM between the **a** conventional CNTFET 6T SRAM and **b** ED tunnel CNTFET 6T SRAM at V_{DD} = 0.9 V

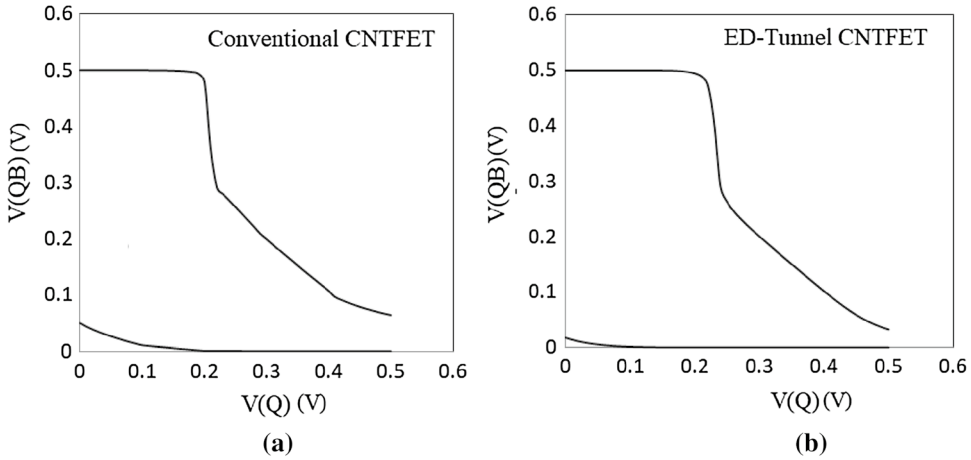


Fig. 10 A comparison of the write SNM between the **a** conventional CNTFET 6T SRAM and **b** ED tunnel CNTFET 6T SRAM at $V_{DD}=0.9$ V

Table 2 A comparison of the performance parameters of the proposed ED tunnel CNTFET SRAM with the conventional CNTFET SRAM at $V_{DD}=0.9$ V

Parameter/device	Conventional CNTFET 6T SRAM	ED tunnel CNTFET 6T SRAM
Read SNM (mV)	165	182
Write SNM (mV)	400	480
Static power (pW)	27	18

Table 3 A comparison of the performance parameters of the proposed ED tunnel CNTFET SRAM with the conventional CNTFET SRAM at $V_{DD}=0.5$ V

Parameter/device	Conventional CNTFET 6T SRAM	ED tunnel CNTFET 6T SRAM
Read SNM (mV)	83	90
Write SNM (mV)	220	255
Static power (pW)	9	5

margin of the cell by 16% at $V_{DD}=0.9$ V and by 14% at $V_{DD}=0.5$ V.

Tables 2 and 3 show a comparison of the performance parameters of the proposed ED tunnel CNTFET versus the conventional CNTFET SRAM at V_{DD} of 0.9 V and 0.5 V. The calculated values of the read noise margin, write noise margin, and static power dissipation are improved in the ED tunnel CNTFET SRAM cell. The power reduction for a single SRAM cell is 9 pW at 0.9 V and 4 pW at 0.5 V. Such power reductions are significant for large memory applications, showing that the ED tunnel CNTFET SRAM is suitable for use in low-power applications.

Figure 11a shows the read noise margin for various V_{DD} values; on increasing the value of V_{DD}, the proposed structure shows an improvement in the read margin. Figure 11b shows the write noise margin at various V_{DD} values, revealing an increase with higher V_{DD}. The proposed ED tunnel CNTFET SRAM cell shows a lesser improvement of the read noise margin compared with the write noise margin, for the reason that only one access transistor is used to conduct the read operation whereas the other access transistor does not conduct due to its unidirectionality.

6.3 Delay

A comparison of the read and write delays of the proposed ED tunnel CNTFET SRAM cell with the conventional CNTFET SRAM cells at $V_{DD}=0.5$ V is presented in Table 4. It is observed that both the read and write delays are reduced in the proposed ED tunnel CNTFET 6T SRAM as compared with the conventional CNTFET 6T SRAM, when using the same feature size. Meanwhile, the write delay of the proposed ED tunnel CNTFET 6T SRAM is 31% and 25% shorter compared with the conventional CNTFET 6T SRAM when writing 0 and 1, respectively. The read delay is also reduced by 16% compared with the conventional CNTFET 6T SRAM cell.

7 Conclusions

A 6T SRAM cell using ED tunnel CNTFETs is designed and investigated. The results show that the ED tunnel CNTFET 6T SRAM cell exhibits lower power consumption, shorter delays, and higher read and write noise margins compared with the CNTFET 6T SRAM. The ED tunnel CNTFET-based 6T SRAM shows a read delay of 0.35 ps and a write delay of 2.43 ps, being 16% and 25% shorter than those of the CNTFET 6T SRAM, and moreover consumes 20% less power. This study finds a major power reduction over the whole voltage range, making the ED tunnel CNTFET an

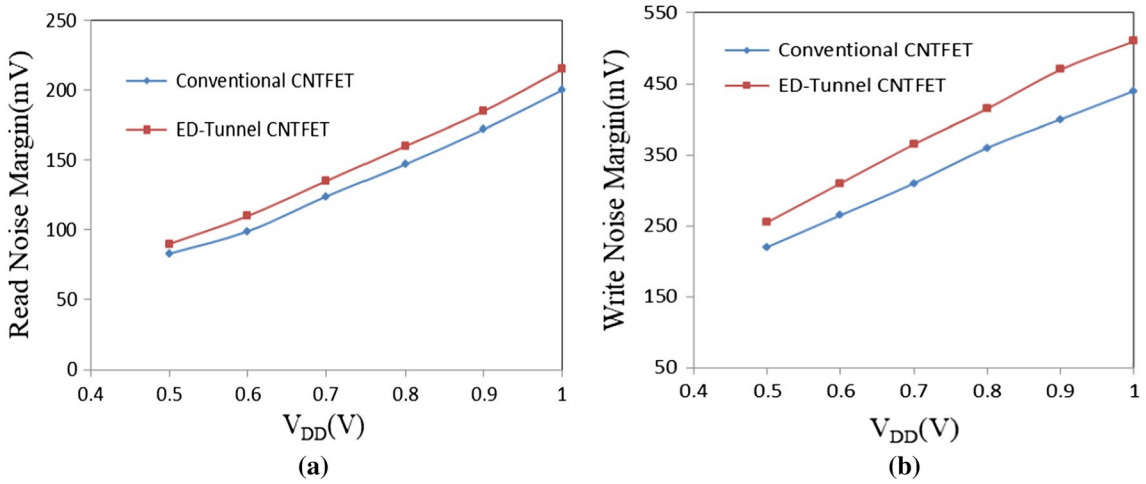


Fig. 11 A comparison of the read noise margin (**a**) and write noise margin (**b**) of the conventional CNTFET 6T SRAM and ED tunnel CNTFET 6T SRAM at different V_{DD} values

Table 4 A comparison of the read and write delays of the proposed ED tunnel CNTFET SRAM cell with the conventional CNTFET SRAM cells at $V_{DD} = 0.5$ V

Structure	Read delay (pS)	Write delay (pS)	
		Write 0	Write 1
Conventional CNTFET 6T SRAM	0.42	2.74	3.05
Proposed ED tunnel CNTFET 6T SRAM	0.35	1.89	2.23

appropriate candidate for use in the design of low-power SRAM.

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