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Simulation of the influence of the gate dielectric on amorphous indium-gallium-zinc oxide thin-film transistor reliability

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Abstract
Indium-gallium-zinc oxide (IGZO) thin films have attracted significant attention for application in thin-film transistors (TFTs) due to their specific characteristics, such as high mobility and transparency. The performance of a-IGZO TFTs with four different insulators (SiO_2 Si_3N_4, Al_2O_3 and HfO_2) is examined using a numerical simulator (Silvaco Atlas). It is found that the output performance is significantly enhanced with high relative permittivity of the insulator. HfO_2 gives the best performance: lower threshold voltage 0.23 V and subthreshold 0.09 V dec^{-1}, higher field-effect mobility 13.73 $cm^2\ s^{-1}\ V^{-1}$ and on current (I_{on}) and I_{on}/I_{off} ratio 2.81×10^{-6} A, 5.06×10^{12}, respectively. Therefore, HfO_2 gate showed high stability compared with other gate insulator materials.

Keywords a-IGZO · TFT · Simulation · Insulators · Stability

1 Introduction

Transparent amorphous oxide semiconductors (TAOS) have attracted more attention compared to conventional transparent oxide semiconductor (TOS) such as zinc oxide (ZnO), indium oxide (In_2O_3) and indium-doped zinc oxide (IZO). Amorphous indium-gallium-zinc oxide (a-IGZO) is the most promising TAOS due to several good properties such as higher mobility, larger band gap, better transparency and room temperature deposition. a-IGZO has a wide application, especially in thin-film transistors (TFT). TFT based on a-IGZO replaced the conventional TFTs based on amorphous silicon (a-Si), zinc oxide (ZnO) or organic semiconductors (OSC) [1, 2]. Enhancing the performance of a-IGZO was the objective of several groups [3–5]. The instability of a-IGZO TFTs following a stress by bias, light, temperature or mechanical is a serious drawback and a sensitive issue in application and industry. Also, a considerable work is ongoing to understand the reasons for this instability following a negative bias illumination stress [6, 7] or a positive bias stress [8, 9]. Several ways are implemented in order to reduce the impact of this instability such as finding an optimal structure [10], using a passivation layer [11], physical and chemical treatments after deposition [3] and finding an optimal insulator of the gate from the channel of the a-IGZO TFT [12]. Various gate insulators, such as silicon dioxide (SiO_2) [13], silicon nitride (Si_3N_4) [14, 15], aluminum oxide (Al_2O_3) [16, 17] and hafnium oxide (HfO_2) [12, 18], have been investigated for use in TFTs.

In this paper, numerical simulation is used to understand the effect of the insulator type on the operation of a-IGZO TFT and the threshold (V_{th}) instability. The insulators compared are SiO_2, Si_3N_4, Al_2O_3 and HfO_2. The other parameters evaluated are: on-current (I_{on}), field-effect mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold swing (SS), on-to-off current ratio (I_{on}/I_{off}) and threshold shift (ΔV_{th}). The numerical simulation is carried out using TCAD of SILVACO-ATLAS software which is a very powerful tool to simulate and study electronic devices. TCAD permits to vary many parameters which model the experimentally observed phenomenon. The numerical study explains the effect of insulators separately from the contribution of other parameters such as interface states between the semiconductor and the insulator or the fixed charge in insulator material. This separation is not achievable in experimental work. Furthermore, numerical simulation decreases the cost and time required by measurement and it is obvious that a rigorous study of insulators and instability effects is very difficult to be achieved experimentally .

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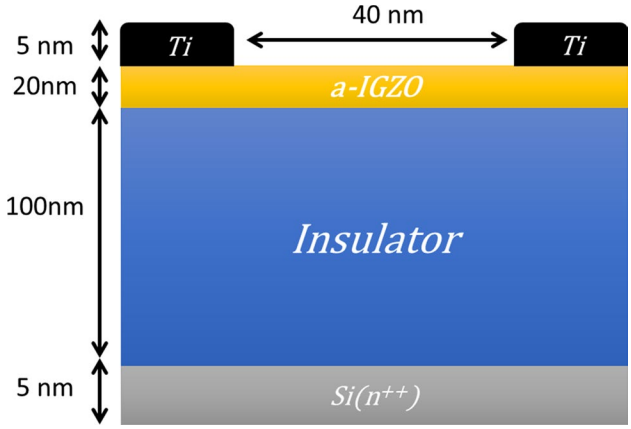

Fig. 1 A 2D schematic view of the a-IGZO TFT structure used in this work

2 TFT structure

We have designed four structures with the same parameters. The difference in the four structures is the insulator layer. SiO_2, Si_3N_4, Al_2O_3 and HfO_2 are the four different insulators. The schematic a-IGZO TFT structure studied in this work is shown in Fig. 1. It consists of an a-IGZO active channel; 20 nm thick, an insulator layer whose thickness is 100 nm and a poly crystalline silicon wafer substrate (n^{++}) as a gate. The length (L) and the width (W) of the channel are 30 and 180 µm, respectively. The source and the drain are 5 nm thick and are made of titanium (Ti).

3 Physical model

Numerical simulation is a powerful tool to understand the physics of electronic devices and materials. It is also a cheap and effective tool to optimize the semiconductor device conception and operating mode. The Poisson and the continuity equations describe the electronic phenomena inside the semiconductor and the electrical transport mechanism involved. Numerical resolution is the best way to solve the nonlinear Poisson and continuity equation system and get information about the effect of various parameters (physical and technological) included in the device operation.

It is well known that a-IGZO density of gap states is formed by donor tail state $g_{vt}^{D}(E)$ with exponential decay from E_V, and a donor Gaussian distribution $g_{G}^{D}(E)$ with a maximum located at 2.9 eV (from E_V) with width 0.1 eV and another narrow acceptor tail state $g_{ct}^{A}(E)$ near E_C. These distributions are expressed as follows [19–22]:

$$g_{vt}^{D}(E) = N_{td} \times \exp\left(\frac{E_v - E}{W_{td}}\right) \tag{1}$$

$$g_{G}^{D}(E) = N_{gd} \times \exp\left(\frac{-(E - egd)^2}{Wgd}\right) \tag{2}$$

$$g_{ct}^{A}(E) = N_{ta} \times \exp\left(\frac{E - E_c}{W_{ta}}\right) \tag{3}$$

Figure 2 shows a plot of the different components usually used to describe the density of states in a-IGZO. Poisson's equation relates the electrostatic potential to the space charge density and is given by [23]:

$$\mathrm{div}(\varepsilon \nabla \psi) = -\rho = -q\left(p - n + n_{tail} - p_{tail} + n_{gd} - p_{ga} + N_d\right) \tag{4}$$

where ψ is the electrostatic potential,ε is the local permittivity,ρ is the local space charge density, n and p are the free carrier's densities, N_d is the n-channel doping concentration and n_{tail}, p_{tail} and n_{gd} are charge states in the band gap.

The continuity equations for both electrons and holes are expressed in the dynamic mode as [23].

$$\frac{\partial n}{\partial t} = \frac{1}{q}\mathrm{div}\overrightarrow{J_n} + G_n - R_n \tag{5}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\mathrm{div}\overrightarrow{J_p} + G_p - R_p \tag{6}$$

In steady state, $\frac{\partial n}{\partial t} = \frac{\partial p}{\partial t} = 0$.

$\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes which are neglected in this study. R_n and R_p are the total recombination rates for electrons and holes in Gaussian and tail states, and q is the electron charge. In the drift–diffusion model, the current densities are expressed in terms of the quasi-Fermi levels ϕ_n and ϕ_p as

$$\overrightarrow{J_n} = -q\mu_n n \nabla \phi_n \tag{7}$$

$$\overrightarrow{J_n} = -q\mu_p p \nabla \phi_p \tag{8}$$

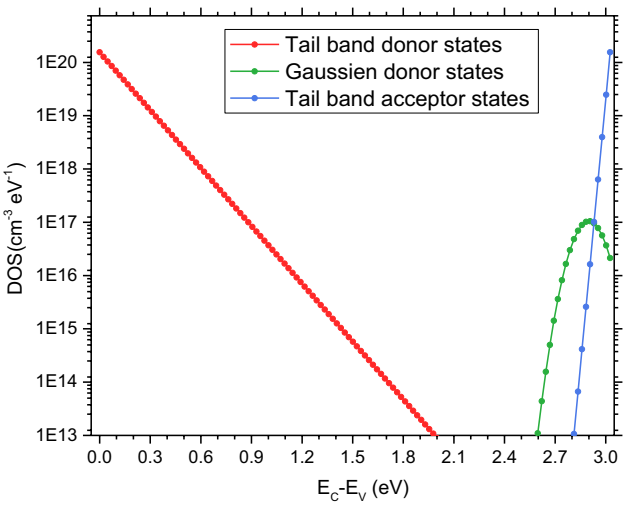

Fig. 2 The density of states in a-IGZO

where μ_n and μ_p are electron and hole mobilities, respectively. The quasi-Fermi levels are linked to the carrier's concentration and the potential through $n = n_i \exp\left(\frac{\psi-\phi_n}{K_B T}\right)$ and $p = n_i \exp\left(\frac{\psi-\phi_p}{K_B T}\right)$ where n_i is the effective intrinsic concentration and T is the absolute temperature.

The physical parameters are presented in Table 1 and applied to the continuity equation. The latter is solved for different applied gate voltages ranging from − 15 to 20 V. The drain voltage was fixed 0.1 V, and the transfer characteristics ($I_{DS} - V_{GS}$) are plotted on a semi-logarithmic scale.

4 Results and discussion

To understand the effect of the insulator on operation a-IGZO TFTs, the Poisson and continuity equations are solved by TCAD using the material properties presented in Table 1. The defects in the band gap have values of 1.55×10^{20} cm^{-3} eV^{-1} for tail band acceptors, and donors and Gaussian donor states have a density/per energy of 5×10^{17} cm^{-3} eV^{-1} for an applied gate voltage ranging from − 10 to 20 V for 0.1 V drain voltage. The transfer characteristics (I_{DS}–V_{GS}) are shown on a linear and semi-logarithmic scale in Fig. 3.

The threshold voltage (V_{th}) and the field-effect mobility μ_{eff} were extracted from the linear plot based on the standard equation of metal-oxide-semiconductor field-effect transistor [24] given by:

$$I_d = \frac{\mu_{eff} C_{ox} W}{L}(V_{gs} - V_{th})V_{ds} \quad (9)$$

where I_d is the drain current, V_{gs} is the gate bias voltage, V_{ds} is the drain bias voltage, C_{ox} is the gate insulator capacitance

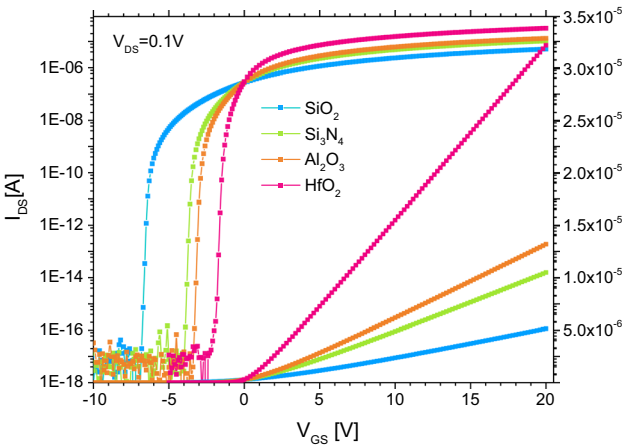

Fig. 3 The transfer characteristics for different insulators layers

Table 1 The physical parameters of the different layers of the a-IGZO TFT used in this work

Layer	Parameters	Designation	Value	Reference
a-IGZO (channel, *n*-type)	N_C(cm^{-3})	Effective DOS in the conduction band	5×10^{18}	[32]
	N_V (cm^{-3})	Effective DOS in the valence band	5×10^{18}	[32]
	E_g(eV)	Band gap	3.05	[32]
	χ(eV)	Electronic affinity	4.16	[33]
	ε	Relative permittivity	10	[33]
	L(μm)	Length	40	
	W(μm)	Width	180	
	T(nm)	Thickness	20	
	$\mu_n\left(\frac{cm^2}{V\,s}\right)$	Free electron mobility	15	[20]
	$\mu_p\left(\frac{cm^2}{V\,s}\right)$	Free hole mobility	0.1	[20]
SiO_2	E_g(eV)	Band gap	9.0	[34]
	ε_{ox}	Relative permittivity	3.9	[34]
Si_3N_4	E_g(eV)	Band gap	5.3	[34]
	ε_{ox}	Relative permittivity	7.5	[34]
Al_2O_3	E_g(eV)	Band gap	8.8	[35]
	ε_{ox}	Relative permittivity	9.3	[35]
HfO_2	E_g(eV)	Band gap	6.0	[36]
	ε_{ox}	Relative permittivity	22.0	[36]
Source and drain contacts (Ti)	d(nm)	Thickness	5	
	Φ_{Ti}(eV)	Work function	4.33	[33]
Gate ploy-Si (n^{++})	d(nm)	Thickness	5	
	$\Phi_{p\text{-}Si}$(eV)	Work function	4.58	[33]

Table 2 The effect of different insulators layer on the output parameters of the TFT

	SiO_2	Si_3N_4	Al_2O_3	HfO_2
V_{th} (V)	−1.7	−0.6	−0.43	0.23
μ_{FE} ($cm^2\ V^{-1}\ s^{-1}$)	7.87	8.21	9.50	13.73
I_{on}(A)	4.44×10^{-06}	9.10×10^{-06}	1.15×10^{-05}	2.81×10^{-05}
I_{on}/I_{off}	5.87×10^{11}	1.43×10^{12}	2.07×10^{12}	5.06×10^{12}
ss ($V\ dec^{-1}$)	0.13	0.11	0.10	0.09

per unit area and W and L are the TFT channel width and length, respectively.

The extrapolated threshold voltages values were −1.07; −0.68; −0.43 and 0.23 V for SiO_2, Si_3N_4, Al_2O_3 and HfO_2, respectively. All insulators in this work show low V_{th} value. A relatively low gate voltage is, therefore, required. The negative value of V_{th} is due to high donor concentration near the conduction band which is around 5×10^{17} cm^{-3} eV^{-1}. The most important parameter describing the TFT performance is the channel mobility. Effective channel mobilities, μ_{eff}, are calculated from the linear region of the transfer characteristics using (9). The field-effect mobility for SiO_2, Si_3N_4, Al_2O_3 and HfO_2 is found to be 7.87, 8.21, 9.50 and 13.73 $cm^2\ s^{-1}\ V^{-1}$, respectively. It is obvious that high value of the field-effect mobility means fast and better performance of the TFT. Low threshold voltage and high field-effect mobility are required and attractive for high-speed TFT application.

The subthreshold swing (SS) was calculated by using the following relation [24]:

$$SS = \left(\frac{d\log(I_d)}{dV_{gs}}\right)^{-1} \tag{10}$$

Subthreshold swings of a-IGZO TFTs with SiO_2, Si_3N_4, Al_2O_3 and HfO_2 are estimated as 0.13, 0.11, 0.10 and 0.09 V dec^{-1}, respectively. SS shows a small variation with the type of the insulator. SS is related to interface and bulk defects. This variation can be explained by dielectric constants for each layer. I_{on} and I_{on}/I_{off} values are: for IGZO/SiO_2 TFT; $I_{on} = 4.44 \times 10^{-6}$ A and $I_{on}/I_{off} = 5.87 \times 10^{11}$, for a-IGZO/$Si_3N_4$ TFT; $I_{on} = 9.10 \times 10^{-6}$ A and $I_{on}/I_{off} = 1.43 \times 10^{12}$, for a-IGZO/$Al_2O_3$ TFT; $I_{on} = 1.5 \times 10^{-5}$ A and $I_{on}/I_{off} = 2.07 \times 10^{12}$, for a-IGZO/$HfO_2$; $I_{on} = 2.81 \times 10^{-6}$ A and $I_{on}/I_{off} = 5.06 \times 10^{12}$. Both a-IGZO/$Al_2O_3$ and a-IGZO/HfO_2 TFTs show high values of I_{on} and I_{on}/I_{off} which make Al_2O_3 and HfO_2 better choices than SiO_2 and Si_3N_4. The high I_{on} for high k insulators is expected due to high μ_{eff} as given by (9). The TFT with the HfO_2 dielectric shows superior electrical characteristics compared to the other insulators TFTs, such as field-effect mobility, I_{on}/I_{off}-current ratio, and subthreshold swing, which are seen in Table 2.

It is observed that the insulator-type influence on the TFT performance depends on the relative permittivity. When the relative permittivity is higher, the TFT performance is better. To understand this influence, internal parameters such the electron concentration and the electric field are extracted. The electron concentration is extracted, for different V_{GS} and $V_{DS} = 0.1$ V, for the different insulators. The electric field is extracted, for different V_{GS} and $V_{DS} = 0.1$ V at the gate–insulator interface, for the different insulators. The extracted electron concentration and field electric are shown in Figs. 4 and 5, respectively.

Figure 4 represents the electron concentration in the transistor channel for the four insulators, for several gate voltages and a drain voltage of $V_{DS} = 0.1$ V. The effect of the insulator type on electron accumulation at the interface between the semiconductor (a-IGZO) and the insulators (all types) is very apparent. Hence, it is expected that it will, evidently, have an effect on the threshold (V_{th}) and the on current (I_{on}). When the electron concentration surpasses 1×10^{14} cm^{-3}, the TFT passes to an on regime. For SiO_2 insulator, −3 V was enough to make electrons accumulate at the interface between the a-IGZO channel and the insulator due to a low electric field as shown in Fig. 5. This may force the a-IGZO/SiO_2 TFT to work in the negative bias region. At 3 V, a low electron concentration at the interface is obtained which gives a smaller I_{on} compared with the other TFTs. The a-IGZO/Si_3N_4 TFT is in the on regime at −2 V gate voltage when the electron concentration surpasses 1×10^{14} cm^{-3}. It is noticed that the electric field shows a higher value than the a-IGZO/SiO_2. At 3 V, the a-IGZO/Si_3N_4 has a higher concentration than the a-IGZO/SiO_2 TFT and less than both a-IGZO/Al_2O_3 and a-IGZO/HfO_2 TFTs. For the a-IGZO/Al_2O_3, TFT works at −1 V which makes it performing better than the a-IGZO/SiO_2 and the a-IGZO/Si_3N_4. The a-IGZO/HfO_2 TFT showed the optimal performance with higher electron concentration at the interface for a positive gate voltage. The low concentration for negative gate voltage may be due to the high electric field. These different values of the electron concentration are related to the effect of the electric flied. The high electric field causes a high electron concentration and makes I_{on} higher, while a low electric filed causes electrons to accumulate near the interface between the semiconductor and the insulator. This makes the TFT

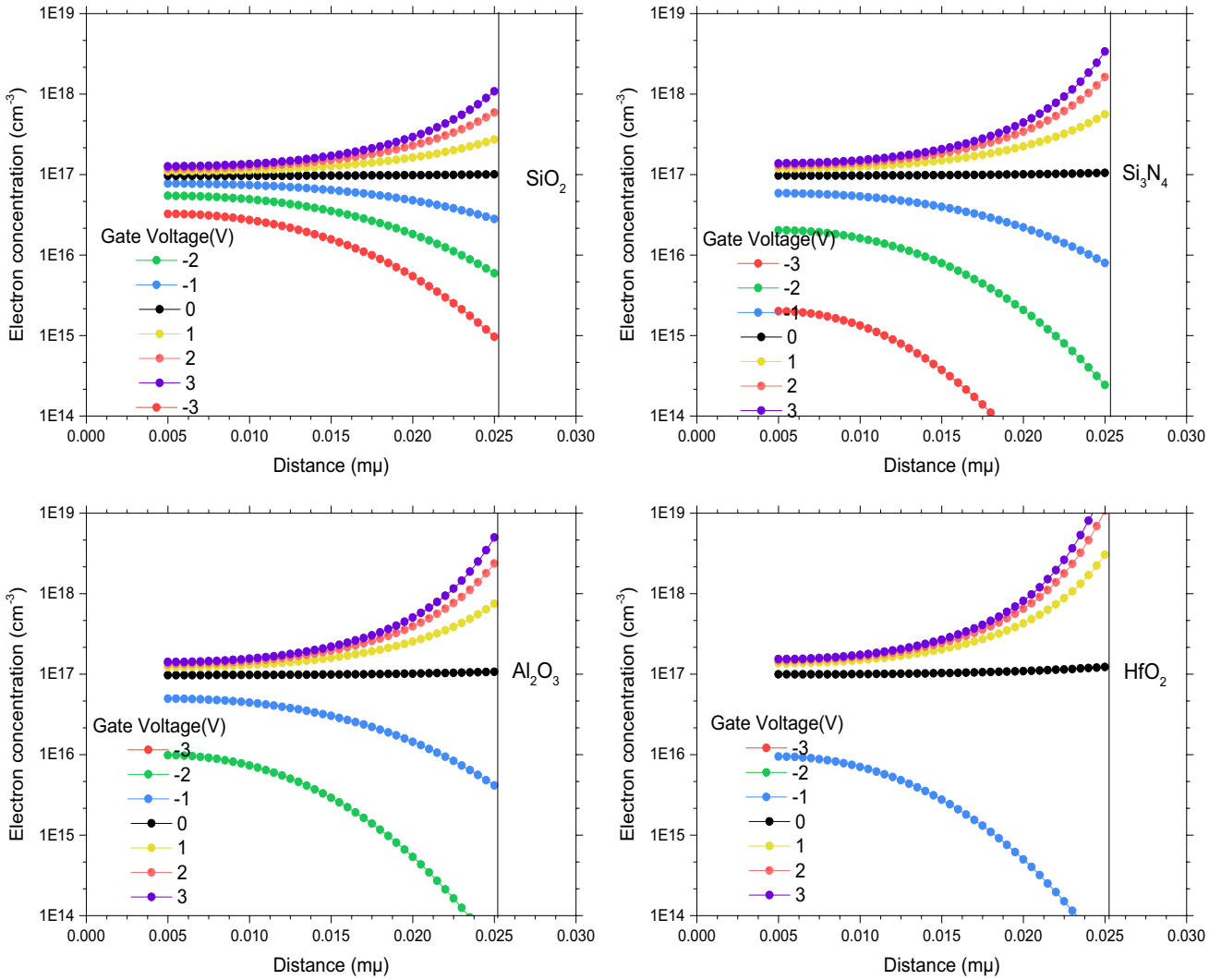

Fig. 4 The electron concentration, for different gate voltages and $V_{DS}=0.1$ V, for the insulators used in this work

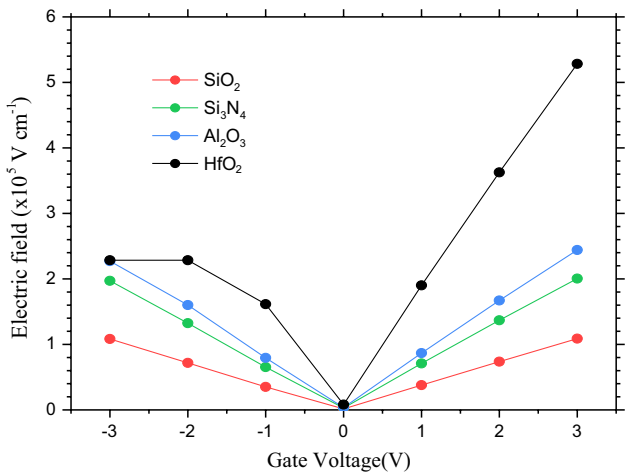

Fig. 5 The electric field for different gate insulators

work in the negative gate bias region and this in turn means the TFT is useless for electronic devices.

The calculation of conduction band offsets is illustrated in Fig. 6. The conduction band offset for a-IGZO/SiO_2 and a-IGZO/Si_3N_4 is 3.26 and 1.56 eV, respectively. Si_3N_4 has a smaller band gap compared with SiO_2, but Si_3N_4 shows better performance due to high relative permittivity. Al_2O_3 has a wide band gap (8 eV) which approaches that of SiO_2 but with a higher relative permittivity (9.3) than SiO_2. a-IGZO/Al_2O_3 shows a better performance than SiO_2 and Si_3N_4. The conduction band offset a-IGZO/HfO_2 is 4.19 eV. a-IGZO/HfO_2 TFT shows good performance compared with other insulators in this work. The offset band calculation shows that insulators were used in this paper suitable for TFT application. We concern the band offsets of semiconductors/insulators. The major problem with the choosing insulators is that some have quite small band gaps. The barrier at each

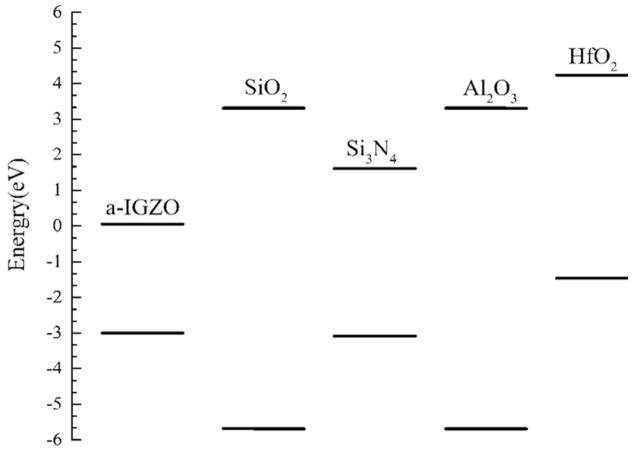

Fig. 6 Band offsets for dielectrics on a-IGZO

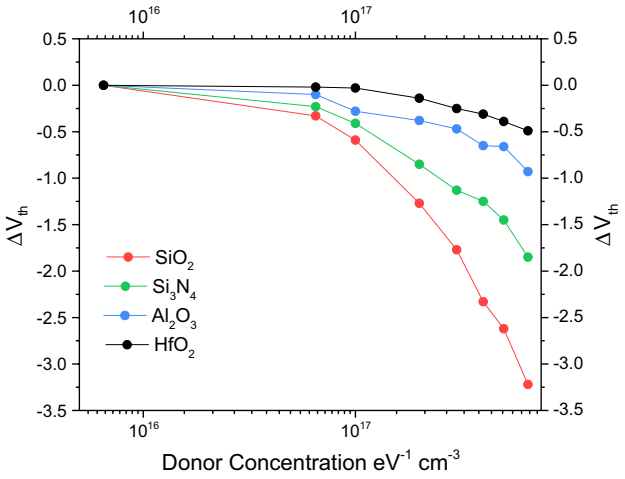

Fig. 7 The threshold shift ΔV_{th} versus the Gaussian donor density per unit energy for different insulator layers

band must be over 1 eV to inhibit conduction by Schottky emission of electrons or holes into their bands [25]. Al_2O_3 and HfO_2 have large band gaps and high k which make them ideal for TFT application. It must be taken into account when a dielectric material is used into a TFT structure; the structure-related requirement includes low defect density, few interfacial trap sites, low fringing capacitive effect and band engineering possibility.

4.1 Impact of insulators on TFTs V_{th} degradation

V_{th} instability is a serious problem in a-IGZO application. The negative bias illumination stress (NBIS) is an important case to the degradation a-IGZO TFT. It is believed that this stress generates defects in a-IGZO or at the interface with the insulator. To clarify the origin of V_{th} instability, we test the assumption of bulk defect generation. The NBIS is modulated by the donor Gaussian states near the conduction band when its increase leads to a negative threshold voltage shift [7, 26–28]. The variation in the transfer characteristics is simulated under increasing donor defects to evaluate the device stability. The density of the Gaussian donor is varied from 6.5×10^{15} to 6.5×10^{17} cm^{-3} eV^{-1}, and V_{th} is extracted for different insulator layers. Figure 7 represents the threshold shift (ΔV_{th}) versus the Gaussian donor density per unit energy for different insulator layers. The a-IGZO/SiO_2 TFT shows a sensitive behavior to the increasing in the donor Gaussian density per unit energy where it is degraded by a shift from 0 to −3.22 V. The a-IGZO/Si_3N_4 TFT was less sensitive compared to the a-IGZO/SiO_2 TFT. IGZO/Si_3N_4 TFT is degraded by a shift from 0 to -1.85 V. The a-IGZO/Al_2O_3-TFT is more stable than the a-IGZO/Si_3N_4 and the a-IGZO/SiO_2 TFTs where it shows a shift from 0 to −0.93 V. The a-IGZO/HfO_2 TFT presents a superior performance compared to other gate insulators materials for which the shift in V_{th} was 0 to −0.43 V. V_{th} instability was significantly different for the different gate dielectric materials, even though all devices have an identical structure including a same physical parameter of the a-IGZO layer. This means that using high k dielectrics layers makes a-IGZO TFT more stable. It is obvious that that all insulators show same behavior which demonstrate that NBIS is independent on the type of the insulator where all TFTs show a negative shift. On the other hand, it can be said that the generation of defects occurs in the semiconductor channel and not at the semiconductor/insulators interface as suggested in some works [29, 30]. But the dominant reason of V_{th} instability in a-IGZO is the generation of free carriers in the channel region [26, 31]. It may be due to the fact that the strong electric filed in high k dielectric controls the electron diffusion in the a-IGZO layer. For a high electron concentration, low k dielectric cannot control the electron diffusion which creates the channel between the source and the drain. This later makes the current flow even without applied gate voltage. In case of the high k dielectric, the strong filed electric control electron diffusion makes it more stable. Figure 8 shows the total current density in a-IGZO channel for two insulator layers: SiO_2 and HfO_2. This indicates that a channel is formed between the source and the drain for SiO_2 and HfO_2. In case of SiO_2, the formed channel is larger, while in the case of HfO_2 it is thinner. This means that the low k dielectric leads to an easier degradation of V_{th} (toward a more negative value).

4.2 Effect of fixed charge in HfO_2 insulator

During HfO_2 fabrication, there might be the possibility of defect creation. Generally, these defects are a fixed charge. It is well known that an MOS (metal–oxide–semiconductor) structure is very sensitive to the fixed charge in the

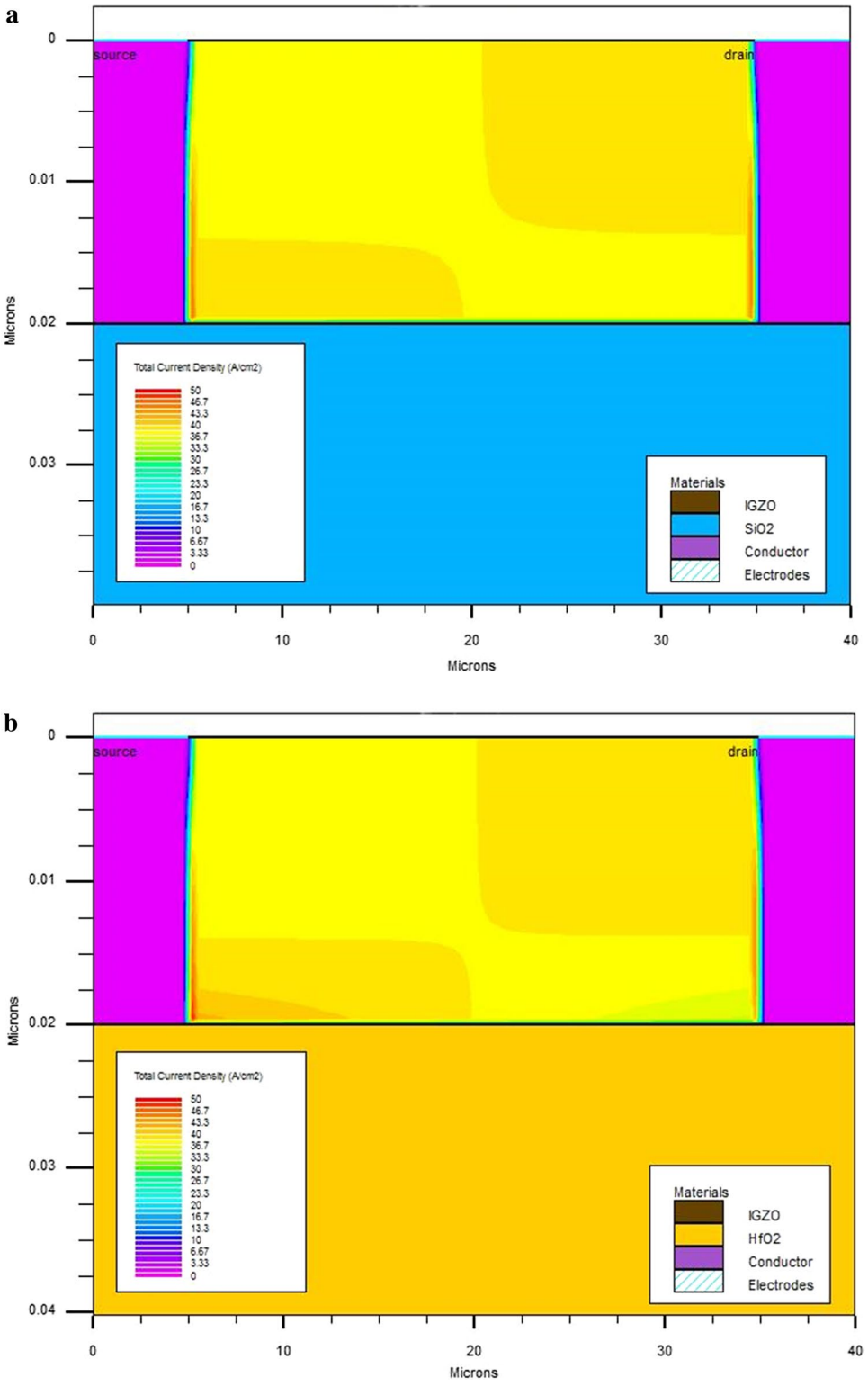

Fig. 8 The total current density for **a** SiO_2 insulator layers and **b** HfO_2 insulator layers

gate insulator. To understand the effect of the fixed charge in HfO_2/a-IGZO TFT, the negative and positive fixed charges are studied. The fixed charge practically is related to oxygen loss and contamination during fabrication. The fixed charge is varied from -3×10^{12} to 3×10^{12} cm^{-2}. Figure 9 shows the TFT transfer characteristics with increasing charge density. The transfer characteristics curve moves toward positive for negative fixed charge, while

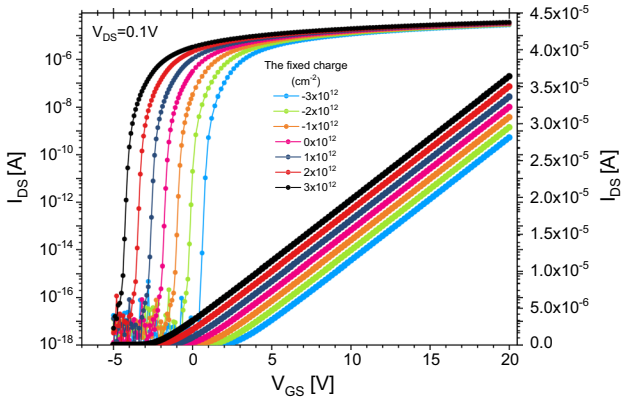

Fig. 9 Transfer characteristics of the TFT with the fixed charge states in the insulator dielectric (HfO_2)

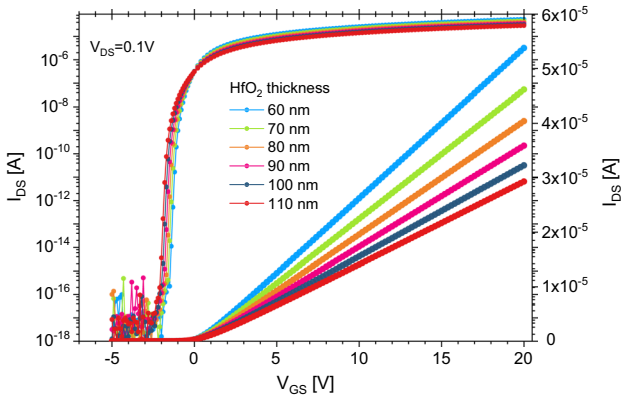

Fig. 10 The transfer characteristics for different thicknesses of HfO_2

the opposite trend is observed for a positive fixed charge. The output parameters do not show any variation with fixed charge except I_{on} and V_{th}. The I_{on} variation is due to the curve shift. V_{th} changes from 0.2 to 3.2 V for a fixed charge changing from 0 to -3×10^{12}. The positive charge leads to a negative V_{th} shift. When the density of the fixed charge is positive and changes from 1×10^{12} to 3×10^{12}, V_{th} changes from -0.1 to -1.7 V. The negative charge in the oxide reduces the electron density that accumulates at the interface between a-IGZO and HfO_2. This makes the TFT requiring a more positive voltage to turn on, while the positive charge in the oxide produces an electron accumulation at the interface even for a negative gate voltage. This requires a more negative voltage to switch OFF the transistor.

4.3 Effect of HfO_2 thickness

In this part, the effect of HfO_2 thickness on the a-IGZO TFT performance is investigated. The thickness was varied from 60 to 110 nm. Figure 10 shows the TFT transfer characteristics for different thicknesses. V_{th} decreases slightly from 0.26 to 0.22 V, which is a negative shift. The field-effect mobility decreases from 26.32 to 11.98 $cm^2\ s^{-1}\ V^{-1}$. It is clear that the field-effect mobility increases when the thickness is reduced. SS on the other hand does not show any variation with thickness. I_{on} increases with decreasing insulator thickness. This is obvious because the field-effect mobility is higher for a thinner insulator. As a result, with thinner gate insulator, the channel area at the same applied gate voltage will induce more carriers. So, even at lower applied gate voltage the conduction channel could be formed in the TFT device and a low driving voltage TFT device would be the result. Devices with thick oxide layer have less gate control on the channel carriers.

5 Conclusion

The performance and stability of a-IGZO TFTs with SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as the gate dielectrics have been investigated and compared using numerical simulation. The simulation results have shown a superior performance that has been achieved for a-IGZO TFTs with the HfO_2 dielectric, such as small threshold voltage, improved subthreshold swing, increased mobility and I_{on} current. The HfO_2 insulator achieved a high stability compared with SiO_2, Si_3N_4 and Al_2O_3, while the instability of a-IGZO is found to be independent of the gate insulator material. SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as the gate insulators show degradation with increasing donor Gaussian density of states. The proper choice of the gate dielectric can provide better device reliability in oxide TFTs. Therefore, the optimization of gate dielectrics materials will be helpful in reducing the instability.

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