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Continuous semianalytical modeling of vertical surrounding-gate tunnel FET: analog/RF performance evaluation

Nidhal Abdelmalek[1] · Fayçal Djeffal[1,2] · Toufik Bentrcia[2]

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Abstract
A continuous and accurate model based on the two-dimensional (2D) potential solution of a tunnel field-effect transistor (TFET) with undoped vertical surrounding-gate (VSG) structure is proposed. Both ambipolarity and dual modulation effects are included to obtain a more accurate analytical model, whose validity is demonstrated by comparison with two-dimensional numerical simulations using ATLAS-2D. The continuity of the proposed model enables extraction of analog/radiofrequency (RF) parameters and device figures of merit. Moreover, the effect of introducing a high-κ layer on the gate oxide in improving the behavior of the VSG-TFET is explored for use in high-performance analog/RF applications. The proposed continuous analytical model can be easily implemented in commercial simulators to study and investigate VSG-TFET-based nanoelectronic circuits.

Keywords Continuous model · Surrounding gate · High-κ · Tunneling FET · Analog/RF · Linearity

1 Introduction

As complementary metal–oxide–semiconductor (CMOS) downscaling approaches its physical limits due to the emergence of major degradation mechanisms, new transistor structures using multiple gates, novel materials, and doping engineering have been successfully employed to extend performance [1–4]. However, to follow the technology roadmap, and the growing requirements for low operating and leakage powers, as well as reliability against short-channel effects (SCEs) and process fluctuations, use of nonconventional devices based on different physical phenomena that overcome classical limitations is highly desired, especially tunneling field-effect transistors (TFETs). The TFET is considered to be an emerging logic device, representing a potential alternative for use in future high-performance and low-power processor chips [5]. Experiments have confirmed the viability of the complementary TFET architecture [6], including fabrication of a fully functional low-power Si gate-all-around (GAA) nanowire tunnel field-effect transistor (NWTFET) inverter with suppressed ambipolarity and large noise margin. Enhanced electrostatic control of the gate-all-around structure compared with planar TFETs has also been demonstrated [7]. The ambipolar behavior of a TFET depends on the drain doping concentration. Generally, such devices are characterized by low leakage current, steep subthreshold slope, efficient transconductance, and high intrinsic gain. Experiments and studies have shown the potential of tunneling transistors for use in low-power amplifiers, logic devices, and analog/RF and sensing applications [6–9]. At circuit level, various new mixed CMOS–TFET designs with different reliability issues have been presented [8,10]. The main difficulty with such mixed designs is how to align the operating voltage of both devices and keep it as low as possible, thus lowering power consumption. Even if TFETs have better immunity against SCEs than conventional metal–oxide–semiconductor field-effect transistors (MOSFETs), this feature is drastically degraded beyond 30 nm, where drain-induced barrier thinning (DIBT) exponentially increases [11,12]. Moreover, the analog/RF performance and linearity are also affected by SCEs [13]. Therefore, new practical design solutions such as high-κ dielectric materials, drain underlap, source/drain doping, gate material engineering, heterojunctions, and III–V materials have been proposed to overcome these physical limitations [11–14]. On the other

✉ Fayçal Djeffal
faycal.djeffal@univ-batna2.dz

[1] LEA, Department of Electronics, University Mostefa Benboulaid Batna-2, 05000 Batna, Algeria

[2] LEPCM, Department of Physics, University of Batna-1, 05000 Batna, Algeria

hand, compact and continuous models that can be applied in both sub- and superthreshold operating domains are useful for understanding both types of device and for circuit simulation. Tunneling phenomena in semiconductor materials are well understood and can be efficiently modeled in Zener diodes and p–i–n junction or tunneling transistors, for which several approaches have been proposed to investigate the quantum and tunnel transport mechanisms in semiconductor devices [15–20]. All these models are directly dependent on the potential profile as a basis to calculate the current, by means of energy bands for nonlocal models or electric field for local ones. In TFETs, the tunneling effect occurs at both channel junctions, viz. source/channel and drain/channel, if ambipolarity is considered. In this case, development of an accurate potential profile model is complex due to the additional processes that have to be taken into account, such as depletion, the fringing effect on source–drain extensions (SDEs), and the impact of the high lateral field near the junctions [21–26]. In addition, the assumption of a constant electric field used in local tunneling models overestimates the current and produces a nonzero current at equilibrium, although this can be resolved by introducing a Fermi occupancy factor difference between the source and drain [26]. The complex barrier shape in TFET devices indicates that a nonlocal approach based on the Wentzel–Kramers–Brillouin (WKB) approximation and Landauer formula is more appropriate [18,27,28]. Nevertheless, the exact barrier profile cannot be used when elaborating such analytical models, so an arbitrary shape is adopted. The assumption of the simplest triangular barrier is equivalent to the Kane approach (i.e., constant electric field) and thus results in the same overestimation [9,27]. On the other hand, the exponential shape is more accurate, but unfortunately the resulting expression for the tunneling probability cannot be integrated analytically, requiring use of numerical integration methods [28].

Recently, several analytical models were developed to investigate TFET devices [24–30]. However, in these models, the simplified Kane's generation rate is used to replace the total electric field by an average one based on the tunneling distance or tunneling window. This approach does not evaluate the generation rate over the entire tunneling barrier and thus fails to reproduce the characteristic response profile. Besides, these models produce complex expressions, making their mathematical differentiation intractable. The derivatives of such formulas are primarily used for extraction of various parameters and figures of merit (FOMs) for assessment of device performance. Furthermore, most of these elaborated models do not take into account drain modulation. In this context, new analytical and continuous models that capture the physics of tunneling transport accurately and efficiently and are suitable for implementation in commercial simulators are required to study and design TFET-based nanoelectronic circuits.

In this work, an undoped vertical surrounding-gate TFET device with high-κ dielectric stack is considered. A continuous semianalytical model is developed by mathematical integration over the channel length of the complete Kane generation rate expression for direct local tunneling. This integral has the merit of preserving the spatial distribution of the generation rate, yielding an accurate response. Both ambipolarity and dual modulation effects are investigated. The electric field expression is derived from an accurate solution of Poisson's equation using Bessel–Fourier series. The analog/RF parameters and various FOMs of the device are deduced from the proposed drain-current model. Moreover, the role of such gate dielectric material engineering in improving the analog/RF performance is investigated. The analytical results are validated against numerical simulations, revealing good agreement for a wide range of design parameters [31].

The remainder of this manuscript is organized as follows: Section 2 is devoted to a description of the various steps for the derivation of the drain-current model. The main simulation results are provided in Sect. 3, where both analog/RF parameters and linearity criteria are treated. We complete this work in Sect. 4 with a summary and some guidelines for future work.

2 Current model derivation

The device considered is a vertical surrounding-gate structure as presented in Fig. 1. The source/drain extensions are symmetric and heavily doped to around $10^{20}\,\mathrm{cm}^{-3}$. The introduction of this high dopant concentration is motivated by attenuation of the depletion effect [32] and attaining a high built-in potential, which in turn will lead to significant tunneling generation. With the channel length of 100 nm, short-channel effects are considerably reduced and the assumption of an intrinsic body is well justified, where only mobile charges define the electrostatic distribution [12]. However, both charge types have to be taken into account to obtain a high transfer characteristic over both positive and negative gate supply values. The dielectric gate stack is composed of silicon oxide with thickness of 2 nm and a high-κ dielectric material with thickness of 1 nm to reduce gate current leakage. Two-dimensional numerical simulations were performed to validate the current model based on Boltzmann statistics and drift–diffusion transport. In addition, we adopted the Kane direct tunneling model to support the tunneling generation phenomenon.

The first step in the derivation of the model is to extract the potential profile over the channel by solving the 2D Poisson's equation, which can be expressed in cylindrical coordinates as

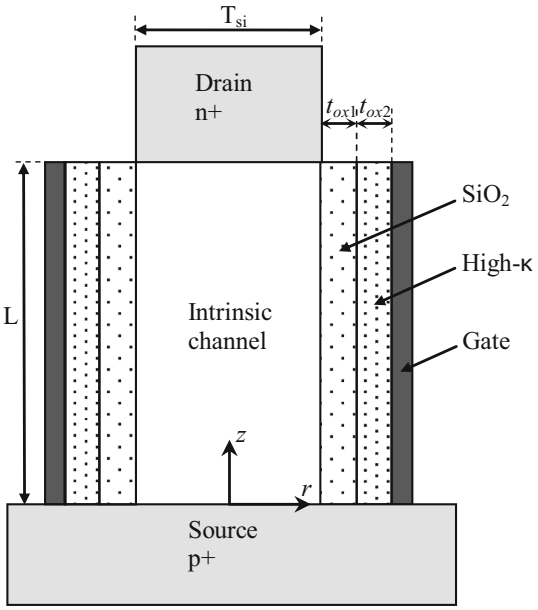

Fig. 1 Cross-sectional view of vertical surrounding-gate TFET structure ($L = 100\,\text{nm}$, $N_{AS} = N_{DD} = 10^{20}\,\text{cm}^{-3}$, $t_{ox1} = 2\,\text{nm}$, $t_{ox1} = 1\,\text{nm}$)

$$\frac{\partial^2\psi}{\partial r^2} + \frac{1}{r}\cdot\frac{\partial\psi}{\partial r} + \frac{\partial^2\psi}{\partial z^2} = -\frac{q}{\varepsilon_{Si}}\rho \tag{1a}$$

$$\rho = \begin{cases} -n_i e^{\left(\frac{\psi - V_{qn}}{V_t}\right)} & \text{for } V_{gs} \geq 0 \\ n_i e^{\left(\frac{-\psi + V_{qp}}{V_t}\right)} & \text{for } V_{gs} < 0 \end{cases}, \tag{1b}$$

where ψ represents the 2D electrostatic potential, ε_{Si} is the silicon dielectric constant, q is the electron charge, n_i is the intrinsic carrier concentration, V_t is the thermal voltage, and ρ is the channel mobile charge concentration.

Depending on the polarity of the gate supply, current transport by only the majority carriers in the channel are considered. Indeed, such neglect of the minority carriers has no consequence even near charge equilibrium, where the center channel potential varies linearly. The quasi-Fermi level V_q included in the boundary conditions is assumed to be constant over the radius and varies from 0 at the source side to V_{ds} at the drain side [33]. At the channel center, the quasi-Fermi levels associated with both carrier types (V_{qn}, V_{qp}) equal, respectively, V_{ds} and 0. To solve Poisson's equation, it must be projected onto two components [33], i.e., a one-dimensional (1D) Poisson equation where the potential $V_c(r)$ represents the solution of Gauss's law in a disk of finite charge density, while the potential $U(z, r)$ in the 2D Laplace equation represents the solution of Gauss's law in a finite cylinder of null charge density. The sum of these two terms gives the total potential distribution in the channel and is expressed with boundary conditions as

$$\frac{\partial^2 V_c}{\partial r^2} + \frac{1}{r}\cdot\frac{\partial V_c}{\partial r} = -\frac{q}{\varepsilon_{Si}}\rho \tag{2a}$$

$$\begin{cases} \left.\frac{\partial V_c(r)}{\partial r}\right|_{r=a} = \frac{C_{ox}}{\varepsilon_{Si}}\left[V_g^* - V_c(a)\right] \\ \left.\frac{\partial V_c(r)}{\partial r}\right|_{r=0} = 0 \end{cases} \quad \text{with} \quad V_g^* = V_{gs} - V_{fb} \tag{2b}$$

$$\frac{\partial^2 U}{\partial r^2} + \frac{1}{r}\cdot\frac{\partial U}{\partial r} + \frac{\partial^2 U}{\partial z^2} = 0 \tag{3a}$$

$$\begin{cases} \left.\frac{\partial U(z,r)}{\partial r}\right|_{r=a} = \frac{C_{ox}}{\varepsilon_{Si}}\left[-U(z,a)\right] \\ \left.\frac{\partial U(z,r)}{\partial r}\right|_{r=0} = 0 \end{cases} \tag{3b}$$

$$\begin{cases} U(0,r) = V_{biS} - V_c = -Vt\ln\left(\frac{N_{AS}}{n_i}\right) - V_c \\ U(L,r) = V_{biD} + V_{ds} - V_c = Vt\ln\left(\frac{N_{DD}}{n_i}\right) + V_{ds} - V_c \end{cases} \tag{3c}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{a\ln(1 + t_{oxeff}/a)} \text{ with } t_{oxeff} = t_{ox1} + t_{ox2}\varepsilon_{ox1}/\varepsilon_{ox2} \text{ and } a = t_{Si}/2, \tag{3d}$$

where V_{fb} represents the flat-band voltage, C_{ox} is the oxide capacitance, ε_{ox} is the silicon oxide dielectric constant, and t_{oxeff} is the effective oxide stack thickness (EOT) depending on the thicknesses of the two (oxide and high-κ) layers and their dielectric constants. Note that, near the channel center, the 2D potential component is neglected so that only the 1D component is involved in the charge concentration expression. Following the Chambré method [34] for solving the Poisson–Boltzmann equation and using the boundary conditions (2b), the channel center potential depending upon the gate polarity is given by

$$V_c = V_{ds} + V_t\log\left(\frac{8\beta}{\delta(\beta - r^2)^2}\right) \text{ for } V_{gs} \geq 0 \tag{4a}$$

$$V_c = V_t\log\left(\frac{\delta(\beta - r^2)^2}{8\beta}\right) \text{ for } V_{gs} < 0, \tag{4b}$$

where $\delta = qn_i/\varepsilon_{Si}V_t$ and the constant β is obtained by substituting (4) into (2b), resulting in the formulas

$$\frac{C_{ox}}{\varepsilon_{Si}}\left(V_g^* - V_{ds} - V_t\ln\left(\frac{8\beta}{\delta\left(\beta - a^2\right)^2}\right)\right) = \frac{4aV_t}{\left(\beta - a^2\right)} \text{ for } V_{gs} \geq 0 \tag{5a}$$

$$\frac{C_{ox}}{\varepsilon_{Si}}\left(V_g^* - V_t\ln\left(\frac{\delta\left(\beta - a^2\right)^2}{8\beta}\right)\right) = \frac{4aV_t}{\left(a^2 - \beta\right)} \text{ for } V_{gs} < 0. \tag{5b}$$

Using the boundary conditions in (3b) and (3c), the solution of the 2D Laplace equation can be expressed based on Bessel–Fourier series as [35]

$$U(z,r) = \sum_{n=1}^{\infty} \frac{J_0(\lambda_n r)}{\sinh(\lambda_n L)} \left[A_n \sinh(\lambda_n (L-z)) + B_n \sinh(\lambda_n z)\right] \tag{6}$$

where λ_n is the nth root of the Robin condition $\lambda_n/C = J_0(\lambda_n a)/J_1(\lambda_n a)$ and $C = C_{ox}/\varepsilon_{Si}$ [36]. The Bessel coefficients A_n and B_n are given by [35]

$$A_n = \frac{2J_1(\lambda_n a)}{\lambda_n a J_0^2(\lambda_n a)(1 + C^2/\lambda_n^2)} (V_{biS} - V_C) \tag{7a}$$

$$B_n = \frac{2J_1(\lambda_n a)}{\lambda_n a J_0^2(\lambda_n a)(1 + C^2/\lambda_n^2)} (V_{biD} + V_{ds} - V_C)\,. \tag{7b}$$

The expression for the total electric field is then deduced by differentiating the potential expression over the length and radius dimensions. However, the channel potential (4) is neglected in the transversal field component to simplify the subsequent analytical integration. The total electric field expression is divided into two components, corresponding to the source and drain sides, as indicated in (8), to calculate the tunneling current separately for each junction so that the ambipolarity behavior can be obtained.

$$\begin{cases} E_S = \left[\sum_{n=1}^{\infty} \frac{\lambda_n^2 A_n^2 \left(J_0^2(\lambda_n r) + J_1^2(\lambda_n r)\right)}{4\sinh(\lambda_n L)} \exp\left(2\lambda_n (L-z)\right)\right]^{1/2} \\ E_D = \left[\sum_{n=1}^{\infty} \frac{\lambda_n^2 B_n^2 \left(J_0^2(\lambda_n r) + J_1^2(\lambda_n r)\right)}{4\sinh(\lambda_n L)} \exp\left(2\lambda_n z\right)\right]^{1/2} \end{cases}. \tag{8}$$

At this stage, even if the channel potential at the center is accurately modeled, a substantial part of the electrostatic potential at the junctions may be lost due to the numerous assumptions and simplifications applied. The first assumption used to explicitly solve Poisson's equation neglects the 2D potential part in the charge concentration term, which is valid only near the channel center [33–37]. Secondly, simulations show that the quasi-Fermi levels included in the boundary conditions (3c) differ from their ideal values, as shown in Fig. 2. In addition, the channel potential V_c is assumed to be constant over the radius in the expressions for the integrals used to obtain the Bessel coefficients (7).

As mentioned above, the effect of depletion and fringing on the source/drain extensions impacts on the potential of the junctions. These effects depend directly on the voltage supply to both the drain and gate terminals. Note that many studies have included such depletion and fringing field effects when modeling various types of structure [21,22,29,38]. Nevertheless, the remarkable lack of accuracy depicted by the outcomes of the cited works makes addition of fitting parameters inevitable to adjust the boundary potential. Although in our case the depletion effect is neglected due to the high SDE

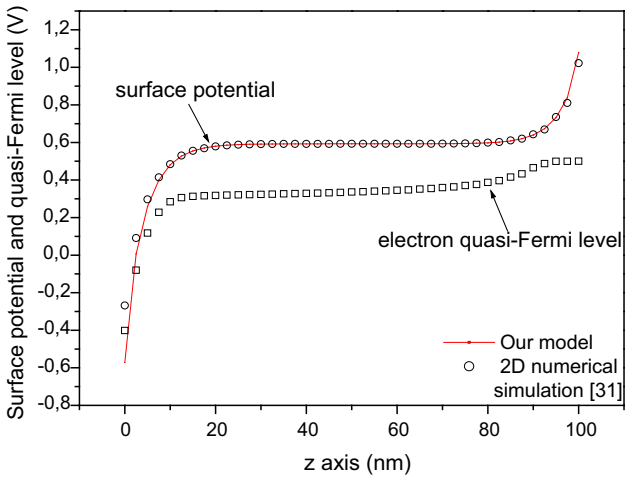

Fig. 2 Surface potential and quasi-Fermi level for $T_{Si} = 10\,\text{nm}$, EOT = 3 nm, $V_{gs} = 0.5\,\text{V}$, and $V_{ds} = 0.5\,\text{V}$

doping, numerical simulations show an important linear variation in the boundary potentials at the silicon interface, which attenuates in depth direction. As use of additional parameters seems necessary, it is preferable to avoid such effects when modeling and rather include fitting parameters and functions directly at the level of the final obtained expressions to simplify their extraction. Consequently, a correction potential V_p is added to the boundary potentials (3c). Guided by the numerical fitting, we observe that this potential depends only on geometrical parameters.

Since analytical integration of the tunneling generation rate over the radius can be difficult under some situations, only the surface total electric field in (8) is considered. Moreover, the process of integrating a long or infinite series is an intractable task, justifying the simplification of expressions (8) by focusing on the first order, given by

$$E_S = A \exp(-\lambda z) \tag{9a}$$

with

$$A = \frac{-\lambda \left(1 + J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}} \exp(\lambda L)}{2\sinh(\lambda L)} \Big(V_p + V_{biS} - V_c \exp\left(V_{cn}\left(1 - \frac{V_c}{V_g^*}\right)\right)\Big)$$

$$E_D = B \exp(\lambda z) \tag{9b}$$

with

$$B = \frac{\lambda \left(1 + J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}}}{2\sinh(\lambda L)} \text{abs}\Big(-V_p + V_{biD} + V_{ds} - V_c \exp\left(V_{cp}\left(1 - \frac{V_c}{V_g^*}\right)\right)\Big).$$

The exponential term describes the dual modulation effect. In the gate modulation regime, one has $V_c = V_g^*$, so the exponential term equals one; otherwise the channel-to-gate potential ratio determines the amount of drain modulation on tunneling generation, corrected using the coefficients V_{cn} and V_{cp}, whose values vary around one and are dependent on geometrical parameters and the drain supply for V_{cn}.

These simplified expressions for the electric field are analogous to the exponential surface potential distribution used in pseudo-2D potential models [18,21,24], as well as the root of the Robin condition, whose inverse is equivalent to the characteristic length. This parameter defines the barrier bending profile, or more specifically the electric field amplitude. Near the junctions, the effect of the high lateral field cannot be neglected, which means that the classical MOSFET interface boundary condition (3b) used to extract the Robin condition roots is no longer valid. In [30], the first-order electric field expression is multiplied by a fitting coefficient to compensate for the truncation of the Fourier series to first order. Moreover, the dependence of the characteristic length on the gate bias was demonstrated and modeled in [23]. To achieve satisfactory accuracy for the potential distribution and reduce the series expression for the total electric field to first order, a dimensionally dependent fitting function is used in the Robin condition as $C_p C/\lambda = J_1(\lambda a)/J_0(\lambda a)$, with C_p defined by

$$C_p = \frac{(\alpha_1 t_{Si} + \beta_1)}{((\alpha_1 t_{Si} + \beta_1)^2 + (\varepsilon_{ox2} + \pi)^2)} + \mu e^{(-\mu(\alpha_2 t_{Si} + \beta_2))} + \nu e^{(\rho(\alpha_2 t_{Si} + \beta_2))}, \quad (10)$$

where all the parameters can be fit numerically. The Kane tunneling generation rate used in this work is given by $G_T = A_k E^{G_k} \exp(-B_k/E)$, where $A_k = 3.3679 \times 10^{21}$, $B_k = 2.5253 \times 10^7$ for silicon material, and $G_k = 2$, since only the direct tunneling process is considered. By replacing the total electric field E by expressions (9a) and (9b), the generation rate for each channel side becomes

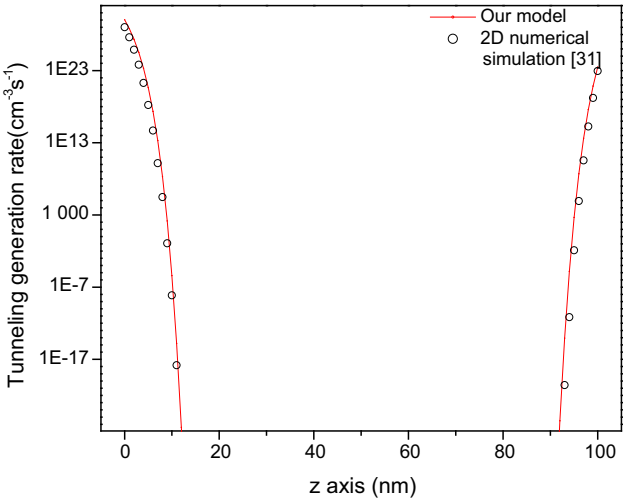

Fig. 3 Tunneling generation rate distribution for $T_{Si} = 10$ nm, EOT = 3 nm, $V_{ds} = 0.5$ V, and $V_{gs} = 0.5$ V

$$G_{TS} = A_k(A^2 \exp(-2\lambda z)) \exp\left(\frac{-B_k \exp(\lambda z)}{A}\right), \quad (11a)$$

$$G_{TD} = A_k(B^2 \exp(2\lambda z)) \exp\left(\frac{-B_k \exp(-\lambda z)}{B}\right). \quad (11b)$$

Figure 3 shows good agreement of the modeled tunneling generation rate with the simulated responses. As expected, the rate is maximum at the junctions, where the major tunneling process occurs, but drops drastically when receding from the channel boundaries. Hence, one can obtain the total tunneling current by summing the integrals of the generation rate equations over the channel length and radius at the junction locations, as illustrated below:

$$I_T = I_{TS} + I_{TD} = q2\pi \int_0^L \int_0^a r\,(G_{TS} + G_{TD})\mathrm{d}r\mathrm{d}z \quad (12)$$

$$I_{TS} = -q\pi a^2 A_k \left(\frac{B_k^2 Ei\left(\frac{-B_k}{A}\right) + A\exp\left(\frac{-B_k}{A}\right)(B_k - A)}{2D\lambda}\right) \quad (13a)$$

$$I_{TD} = -q\pi a^2 A_k \left(\frac{\left(B_k^2 Ei\left(\frac{-B_k e^{-\lambda L}}{B}\right) + B\exp\left(\frac{-B_k e^{-\lambda L}}{B} + 2\lambda L\right)\left(B_k e^{-\lambda L} - B\right)\right)}{2D\lambda}\right) \quad (13b)$$

$$\text{with } D = \left(\frac{\lambda}{(\eta(t_{Si})t_{oxeff} + \sigma(t_{Si}))}\right)^{\tau}\left(1 + \frac{\Delta_r}{\left(1 + \left(\frac{V_g - V_{gm}}{\iota}\right)^2\right)^2}\right) \quad (13c)$$

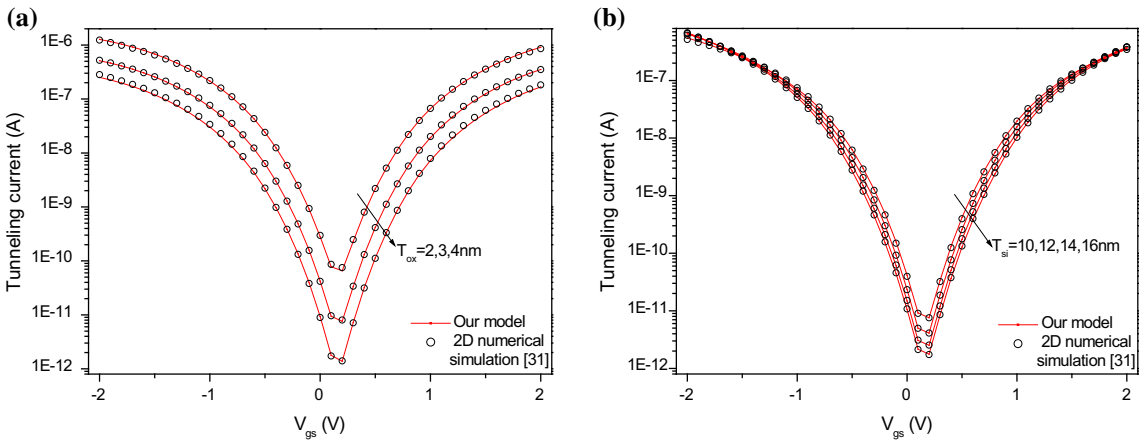

Fig. 4 Tunneling current versus gate bias for **a** different oxide thicknesses ($T_{Si} = 10\,nm$ and $V_{ds} = 0.5\,V$) and **b** different channel diameters (EOT = 3nm and $V_{ds} = 0.5\,V$)

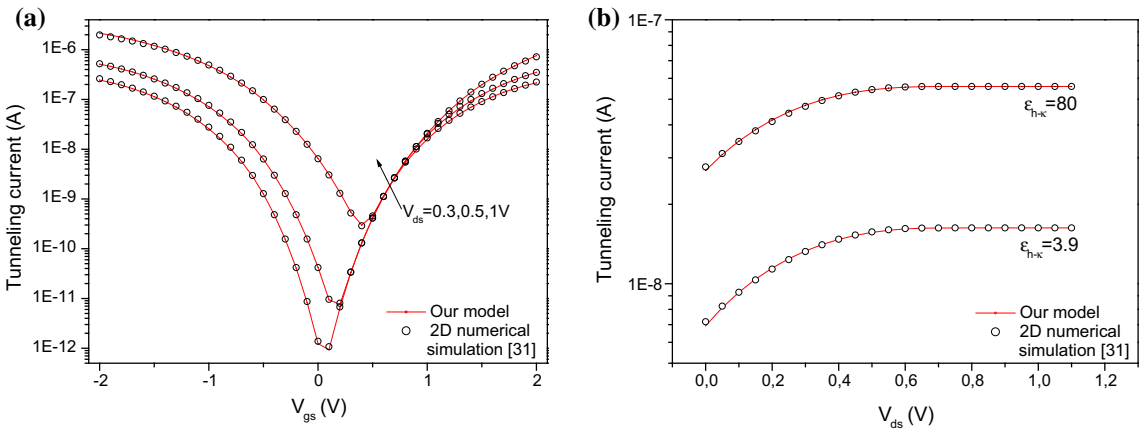

Fig. 5 Tunneling current versus **a** gate bias for different drain biases ($T_{Si} = 10\,nm$ and EOT = 3 nm), and **b** drain bias for different high-κ values ($T_{Si} = 12\,nm$ and $V_{gs} = 1\,V$)

with D a fitting function that evaluates the depth of the tunneling process when only the surface electric field is involved. The second term is a correction function that permits the relative error against numerical simulations to be reduced to around 0.1 % during gate modulation, where V_{gm} is the gate voltage and Δ_r is the relative error corresponding to the minimum current.

The next figures validate the current model for different configurations and voltage supplies. As can be deduced from the model, reducing the oxide layer thickness will increase the oxide capacitance, electric field, and tunneling current in turn, as illustrated in Figs. 4a and 5b. In an analogous manner, reduction of the channel radius leads to an increase in the tunneling current.

The ambipolarity behavior is well described, as well as the dual modulation effect. The tunneling current on the drain side increases relative to the drain bias and shifts the minimum current forward with gate voltage. Furthermore, it is clearly shown that, during gate modulation, the tunneling process on the source side is totally independent of the drain bias. The dual modulation effect is also described in Fig. 5b, where for low drain bias, the tunneling on the source side is controlled by the drain modulation. The channel potential varies linearly with the drain bias until the drain boundary potential exceeds the channel potential. Then, the regime switches to gate modulation, where the constant gate bias fixes the tunneling near the source side and raises its value at the drain side.

The next step is differentiation of the expression for the current with respect to the gate and drain supplies, with the aim of extracting different analog/RF parameters. Note that only the source tunneling current is considered.

$$\frac{\partial I_{TS}}{\partial V_{gs}} = q\pi a^2 A_k \left(\frac{A e^{\left(\frac{-B_k}{A}\right)}}{D\lambda} \frac{\partial A}{\partial V_{gs}} \right) \tag{14}$$

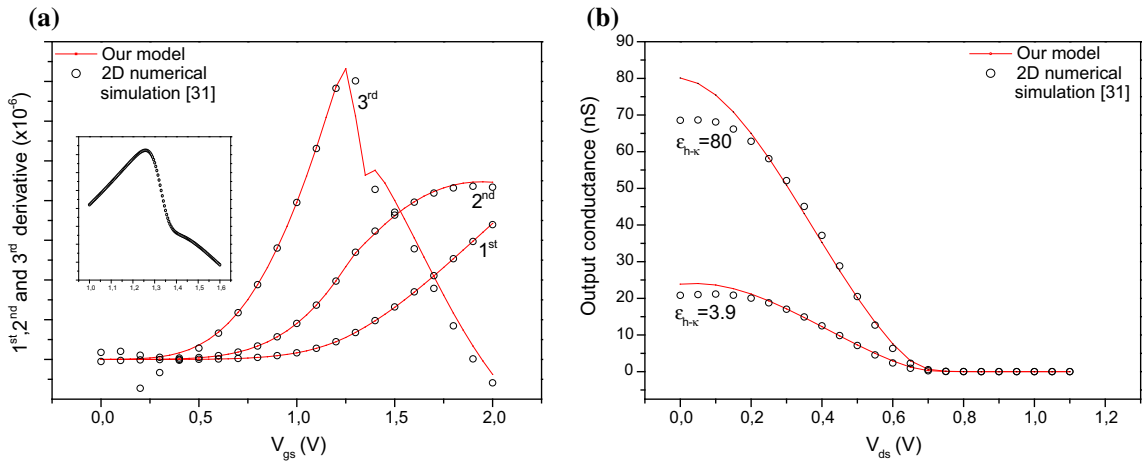

Fig. 6 **a** Multiple derivates of the current with respect to the applied gate voltage ($T_{Si} = 14$ nm, EOT = 3 nm, and $V_{ds} = 1$ V); the inset illustrates the simulated third derivative with more accuracy. **b** First derivative of the current with respect to applied drain voltage ($T_{Si} = 12$ nm and $V_{gs} = 1$ V)

with

$$\frac{\partial A}{\partial V_{gs}} = -\lambda\left(1 + J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}}\left(\frac{V_{cn}V_c\left(V_g^*\frac{\partial V_c}{\partial V_{gs}} - V_c\right)}{V_g^{*2}} - \frac{\partial V_c}{\partial V_{gs}}\right)\exp\left(V_{cn}\left(1 - \frac{V_c}{V_g^*}\right)\right)$$

and

$$\frac{\partial V_c}{\partial V_{gs}} = \left(1 + \frac{4a\beta}{C\left(\beta^2 - a^4\right)}\right)^{-1}.$$

The last equation is obtained by differentiation of expression (4a) then replacing the derivative of β by

$$\frac{\partial \beta}{\partial V_{gs}} = \left(\frac{-\beta\left(\beta - a^2\right)}{V_t\left(\beta + a^2\right)}\right)\frac{\partial V_c}{\partial V_{gs}}.$$

Following the same methodology, the derivative with respect to the drain supply is given by

$$\frac{\partial I_{TS}}{\partial V_{ds}} = q\pi a^2 A_k\left(\frac{Ae^{\left(\frac{-B_k}{A}\right)}}{D\lambda}\frac{\partial A}{\partial V_{ds}}\right), \tag{15}$$

where

$$\frac{\partial A}{\partial V_{ds}} = \lambda\left(1 + J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}}\left(V_c\frac{\partial V_{ce}}{\partial V_{ds}} + V_{ce}\frac{\partial V_c}{\partial V_{ds}}\right)$$

and

$$\frac{\partial V_c}{\partial V_{ds}} = \left(1 + \frac{C\left(\beta^2 - a^4\right)}{4a\beta}\right)^{-1} \text{ and } \frac{\partial \beta}{\partial V_{ds}} = \left(\frac{\left(\beta - a^2\right)^2}{4aV_t}\right)\frac{\partial V_c}{\partial V_{ds}}.$$

Here, the fitting function V_{ce} replaces the exponential term since the drain-bias-dependent parameter V_{cn} is difficult to model and by doing so the derivative expression is simplified. The numerical fitting provides the formula $V_{ce} = 4\left(V_c + c_1\right)^{-1/4} + c_2V_{ds} + c_3$.

The transition from gate to drain modulation of the tunneling barrier is reflected in the third derivative in Fig. 6a. This transition occurs smoothly over an interval of gate bias. The start point corresponds to the maximum of the third derivative, while the end point is revealed by a kink effect. On the basis of the expressions elaborated above, any degree of differentiation can be obtained with good agreement in comparison with its numerical counterpart, especially during the gate modulation, as depicted in Fig. 6. Nevertheless, the exponential term accounting for the drain modulation must be accurately modeled. One of the important parameters obtained from the expression for the derivative of the current to assess TFET performance is the subthreshold slope (SS), expressed as

$$SS = \frac{\partial V_{gs}}{\partial \log_{10}(I_T)} = \log(10)\frac{(I_{TS} + I_{TD})}{\partial I_{TS}/\partial V_{gs} + \partial I_{TD}/\partial V_{gs}} \tag{16}$$

with

$$\frac{\partial I_{TD}}{\partial V_{gs}} = q\pi a^2 A_k\left(\frac{Be^{\left(2\lambda L - \frac{B_k\exp(-\lambda L)}{B}\right)}}{D\lambda}\frac{\partial B}{\partial V_{gs}}\right),$$

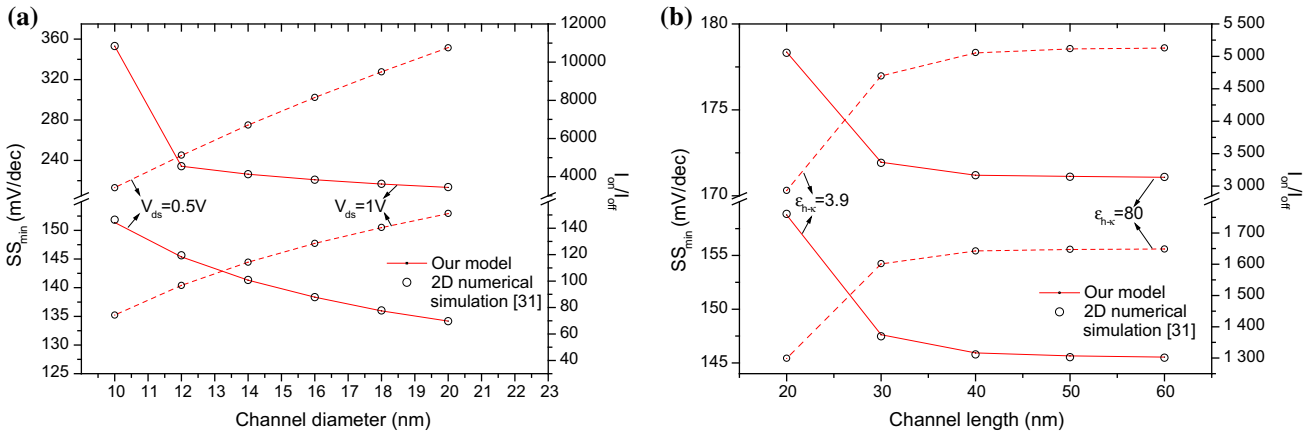

Fig. 7 **a** SS_{min} (solid) and I_{on}/I_{off} (dashed) as functions of channel diameter for different drain biases (EOT = 3 nm and $L = 100$ nm). **b** SS_{min} (solid) and I_{on}/I_{off} (dashed) as functions of channel length for different high-κ dielectric constant ($T_{Si} = 12$ nm and $V_{ds} = 0.5$ V)

where

$$\frac{\partial B}{\partial V_{gs}} = -\frac{\lambda\left(1 + J_1^2(\lambda a)/J_0^2(\lambda a)\right)^{\frac{1}{2}}}{2\sinh(\lambda L)}.$$

Note that the derivative of the term B is limited to the gate modulation regime, where the exponential term equals one. The next figures illustrate the variation of the minimum subthreshold slope and I_{on}/I_{off} current ratio for different dimensions and drain supplies (I_{on} at $V_{gs} = 1$ V and $I_{off} = I_{Tmin}$). As mentioned above, reduction of the channel diameter or oxide thickness enhances the on-current. Unfortunately, the off-current is increased as well, by an amount that exceeds the magnitude of the on-current increase. Consequently, the I_{on}/I_{off} current ratio as well as SS_{min} degrade for reduced channel diameter and oxide thickness (Fig. 7a, b). Furthermore, these degradations are accentuated with drain bias increase. Such major alterations can be attributed to the wide bandgap of silicon and the enhanced ambipolar current. In practice, many solutions are available to improve TFET performance. In this regard, the validity of the developed model for any material may be useful to explore the impact of material engineering. Nevertheless, as our model is based on a local tunneling approach, it is not suitable for heterostructure TFETs, for which a nonlocal model should be applied [18,28].

To obtain a more reliable modeling framework, the model must be adapted to describe SCEs. Indeed, the model is derived based on the assumption that $\sinh(\lambda L) \approx \exp(\lambda L)/2$, which is correct only for long channel lengths. Furthermore, drain-induced barrier thinning will modify the electrostatic distribution, resulting in higher lateral electric field, indicating the need to include the effect of the length on the root of the Robin condition λ [11]. To avoid additional modeling complexity, the impact of length variation is added to the parameters D and V_p by means of a fitting coefficient expressed as $1 + \alpha' \exp(\beta' L)$. This solution gives good agreement of the model with numerical results, as illustrated in Fig. 7b.

As reported in literature [11,12], the TFET exhibits good immunity against SCEs, while this feature is drastically degraded beyond 30 nm, where the subthreshold slope as well as I_{on}/I_{off} ratio are degraded in an exponential manner, as depicted in Fig. 7b. Note that the direct and trap-assisted tunneling from source to drain that become possible for lengths approaching 20 nm are not taken into account but may further degrade device performance [9]. However, the high-κ layer attenuates the SCEs, with SS_{min} varying around 4 % for a layer with dielectric constant of 80 compared with 9 % for a device without a high-dielectric layer.

3 Results and discussion

This section is composed of two parts. The first subsection is dedicated to the presentation of the analog/RF measures, while the second part is reserved for analysis of different linearity criteria.

3.1 Analog/RF parameters

Investigation of the scaling capability, device performance, and linearity in the high-frequency regime is mandatory for circuit design purposes. The TFET paradigm has been considered as a competitive alternative to MOSFET devices for use in analog/RF applications. Device performance can be assessed by compact modeling of the analog/RF parameters jointly with FOM analysis [13,39]. The next figures depict various analog/RF criteria for different geometrical parameters in gate modulation mode ($V_{gs} = V_{ds}$=1 V). The transconductance, defined as $\partial I_{ds}/\partial V_{gs}$, is shown in Fig. 8a as a function of channel diameter for different

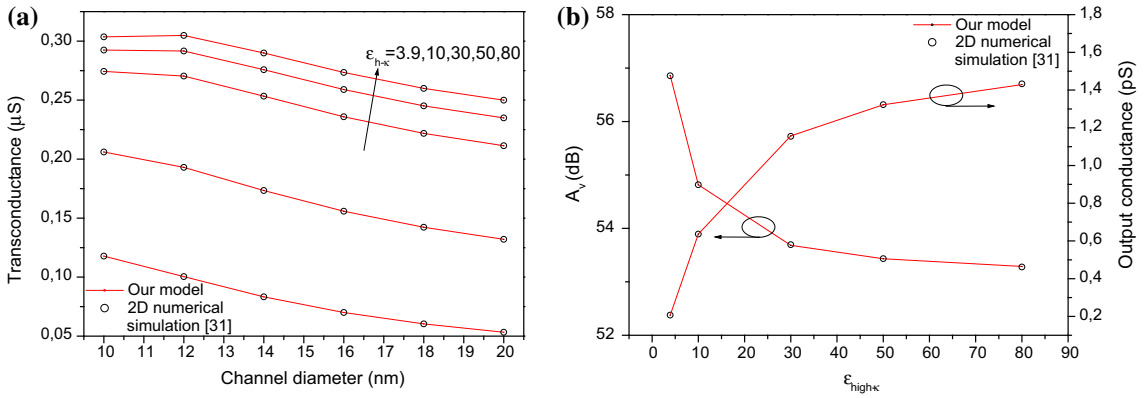

Fig. 8 **a** Transconductance as function of channel diameter. **b** Intrinsic gain and output conductance as functions of high-κ dielectric constant for $T_{\mathrm{Si}} = 12\,\mathrm{nm}$, $V_{\mathrm{ds}} = 1\,\mathrm{V}$, and $V_{\mathrm{gs}} = 1\,\mathrm{V}$

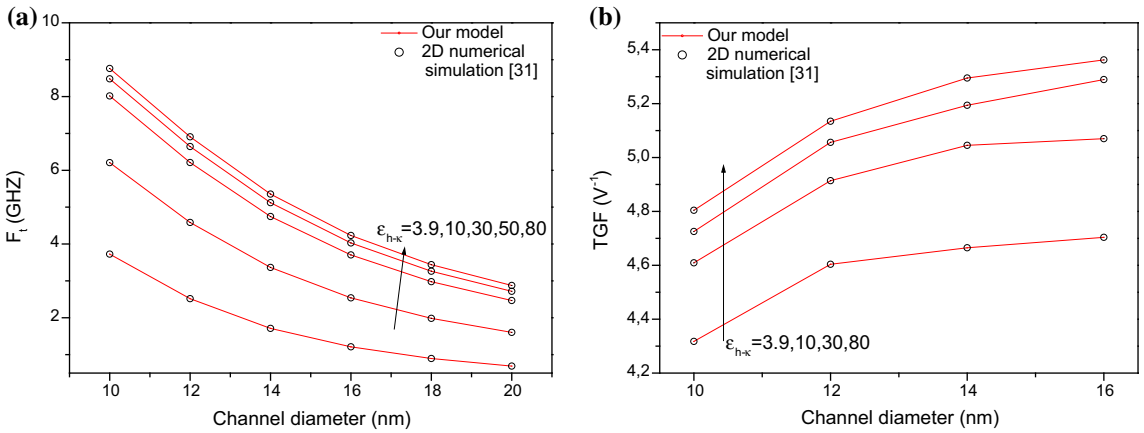

Fig. 9 **a** Cutoff frequency as function of channel diameter ($V_{\mathrm{ds}} = 1\,\mathrm{V}$ and $V_{\mathrm{gs}} = 1\,V$). **b** Transconductance generation factor as function of channel diameter ($V_{\mathrm{ds}} = 1\,\mathrm{V}$ and $G_{\mathrm{m}} = 0.4\,\mu\mathrm{S}$)

high-κ values. Similarly to the case of the current, reducing the channel or the effective oxide thickness increases the transconductance. However, attenuation of the high-κ layer effect is observed for a value of 10 nm. Likewise, the output conductance, defined as $\partial I_{\mathrm{ds}}/\partial V_{\mathrm{ds}}$, shows an increasing tendency with respect to the high-κ dielectric value (Fig. 8b). Note that, even if the transconductance of the TFET is relatively low with respect to MOSFETs, the output conductance is as much lower, leading to an acceptable intrinsic gain expressed as $A_{\mathrm{v}} = G_{\mathrm{m}}/G_{\mathrm{d}}$. However, the impact of the high-κ layer is more pronounced on G_{d} than G_{m}, resulting in degradation of the gain, as highlighted in Fig. 8b.

As a consequence of the transconductance enhancement, the unity-gain cutoff frequency is improved in the same way, as shown in Fig. 9a. It is expressed as $f_{\mathrm{t}} \approx G_{\mathrm{m}}/(2\pi C_{\mathrm{gg}})$, where $C_{\mathrm{gg}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$ represents the total gate capacitance extracted numerically.

The transconductance generation factor, expressed by $\mathrm{TGF} = G_{\mathrm{m}}/I_{\mathrm{d}}$, is another important criterion for analog/RF applications, playing a vital role in the field of RF circuit design [40]. It can be interpreted as the efficiency of a device to convert current (or implicitly power) into transconductance and therefore gain and frequency [41]. To evaluate the effect of the gate stack and radius on the TGF, it is shown at constant transconductance in Fig. 9b. It seems that the TGF drops with reduction of the channel thickness. However, this degradation is largely compensated by the reduction of the effective oxide thickness.

3.2 Linearity analysis

As for MOSFETs, nonlinearity is an inherent TFET characteristic. In analog/RF applications such as low-noise amplifiers (LNAs) or filters, linearity in the operating range must be obtained to preserve circuit performance. Due to high second- and third-order transconductance derivatives, gain compression, distortion, and intermodulation become important, leading to signal corruption and loss of output power [42]. In a nonlinear system, the output can be expressed in a Taylor series expansion as a function of the alternating-

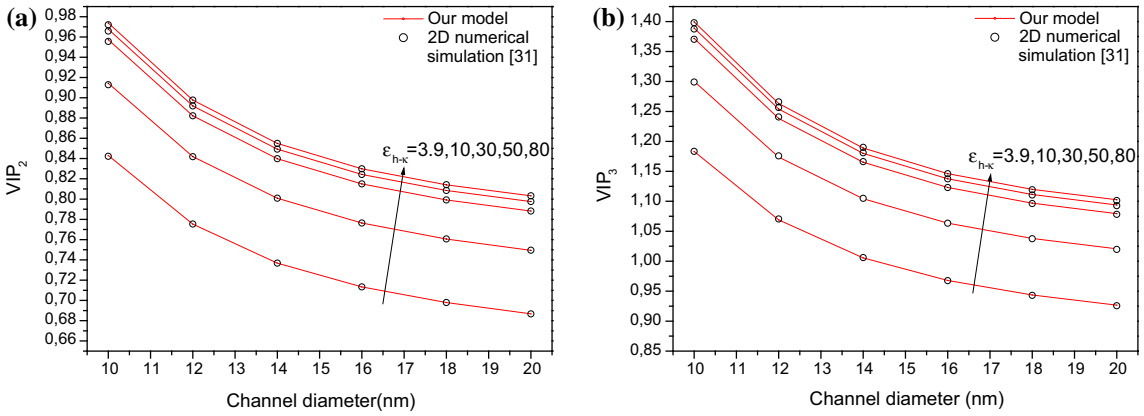

Fig. 10 **a** Second-order voltage intercept point and **b** third-order voltage intercept point as function of channel diameter ($V_{ds} = 1$ V and $V_{gs} = 1$ V)

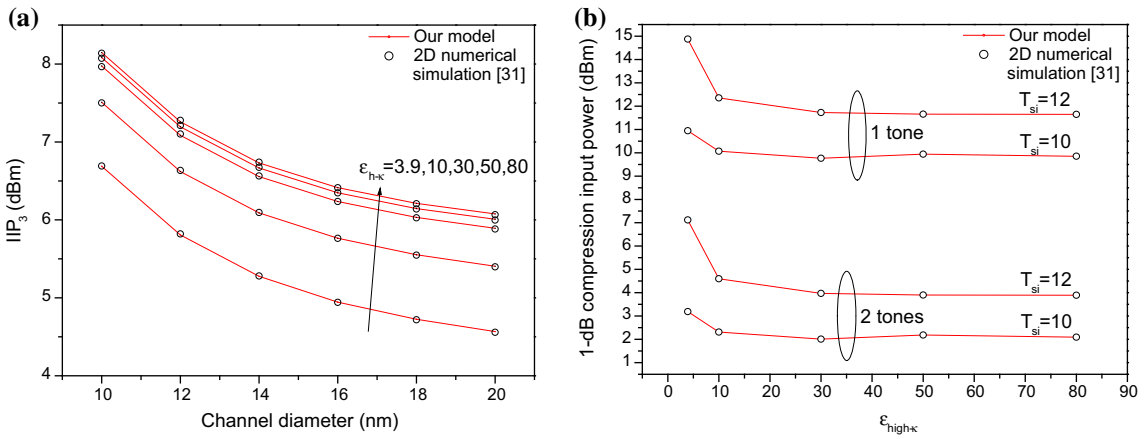

Fig. 11 **a** Third-order input power intermodulation intercept point as function of channel diameter ($V_{ds} = 1$ V and $V_{gs} = 1$ V). **b** 1-dB compression point as function of high-κ dielectric constant ($V_{ds} = 1$ V, $V_{gs} = 1.8$ V)

current (AC) gate voltage as [43]

$$I_{ds} = I_0 + \sum_{i=1} \frac{g_{mi}}{i!} v_{gs}^i, \tag{17}$$

where I_0 is the direct-current (DC) component and $g_{mi} = \frac{\partial^i I_{ds}}{\partial v_{gs}^i}$ is the ith derivative of the drain current. Based on the previous expression, the linearity FOMs can be extracted as follows [44]:

$$\mathrm{VIP}_2 = \frac{4g_{m1}}{g_{m2}}, \tag{18a}$$

$$\mathrm{VIP}_3 = \sqrt{\frac{24g_{m1}}{g_{m3}}}, \tag{18b}$$

$$\mathrm{IIP}_3 = \frac{4g_{m1}}{R_s g_{m3}}. \tag{18c}$$

The second and third voltage intercept points, denoted by VIP_2 and VIP_3, respectively, represent the voltage at which the second and third harmonics reach the fundamental tone and determine the amount of signal distortion [44]. Therefore, higher values of these FOMs indicate a wider linear operating range. Ideally, in a system with odd symmetry, harmonics of even order vanish, while in a real circuit, symmetry corruption yields a finite number of even-order harmonics [42]. As illustrated in Fig. 10, reducing the channel width and effective oxide thickness widens the linear operating range. For an input comprising two tones, additional nonharmonic components are generated from the frequency difference, a phenomenon called intermodulation (IM). In analogy with VIP_3, the third-order intermodulation intercept point IIP_3 represents the input at which the amplitude of the generated third-order IM components equals that of the fundamentals [42,45]. In the case of a differential LNA, the extrapolated voltage input ($\sqrt{8g_{m1}/g_{m3}}$) is squared and divided by twice the ideal input resistance R_s of 50 Ω to yield IIP_3 in terms of power [46]. As for the previous FOMs, IIP_3 (Fig. 11a) exhibits the same improvement trend.

Even if the increase of the signal amplitude worsens the distortion, the second and third harmonics can be filtered, which is not the case for the total amplitude of the fundamen-

tal, for which the increase of the negative second term yields signal compression [45,46]. This term is generated by the third harmonic and is generally neglected for very small signals. Its effect for higher amplitudes can be extrapolated by means of the 1-dB compression point, defined as the input at which the fundamental amplitude drops by 1 dB, expressed as $0.38\sqrt{|6g_{m1}/g_{m3}|}$ for one-tone input and $0.22\sqrt{|6g_{m1}/g_{m3}|}$ for input of two tones with the same amplitude [42,45]. Note that g_{m3} becomes negative above the threshold voltage and during drain modulation. As observed in Fig. 6a, the results computed for the modeled current derivatives show an important error for high V_{gs}. Thus, a more accurate expression for the exponential term describing the drain modulation as $\exp\left(V_{cn}\left(1-\left(\frac{V_c}{V_g^*}\right)^{V'_{cn}}\right)\right)$ is used. Figure 11b shows the 1-dB compression point input power extracted for both one and two tones, respectively, in the case of a single-ended LNA and a differential LNA for 50 Ω input resistance at 1.8 V DC gate bias. It is shown that, by reducing either the channel diameter or effective oxide thickness, the 1-dB compression point can be lowered, thereby reducing the dynamic operating range.

4 Conclusions

A continuous, accurate tunneling current model based on a cylindrical harmonics solution of the 2D potential was developed for a vertical surrounding-gate structure. The model describes the ambipolar tunneling and dual modulation effects remarkably well. The continuity and high transfer characteristic permit evaluation of device scaling capability, analog/RF performance, and linearity. The results show that decreasing either the channel diameter or effective oxide thickness improves the current and the majority of device FOMs. Moreover, the role of introducing a high-κ layer on the gate oxide in improving the behavior of the VSG-TFET is investigated for use in high-performance analog/RF applications, revealing strong effects on the power consumption and dynamic operating range. Thus, the dimensions and operating supply range should be carefully chosen depending upon the device application. Overall, the results demonstrate a comfortable upper limit of the dynamic operating range with high gain and acceptable cutoff frequency, making such TFET structures promising candidates for use in low-power analog/RF applications.

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