Journal of Computational Electronics (2018) 17:756–765
https://doi.org/10.1007/s10825-018-1129-5

Impact of asymmetric dual-k spacers on tunnel field effect transistors

Mohd Adil Raushan[1] · Naushad Alam[1] · Mohd Waseem Akram[2] · Mohd Jawaid Siddiqui[1]

Published online: 3 February 2018
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Abstract

In this paper, we propose a novel device structure for tunneling FETs, based on charge plasma concept, such as junctionless-TFET (JLTFET) and dopingless-TFET (DLTFET) with asymmetric dual-k spacer. Using 2-D simulations, we demonstrate that ON-state current increases significantly with the use of asymmetric dual-k spacers between the gate and p-gate/source in JLTFET and DLTFET. We optimize the spacer length (L_S) between gate and p-gate/source for these transistors having low-k spacer only. We have employed dual-k spacer, which consists of high-k spacer on gate side and low-k spacer on source side, which could also be interchangeably used. We also optimize the inner high-k spacer length for better analog and digital performance and investigate their impacts on the transistor performance. The simulation results for asymmetric dual-k spacers JLTFET (ADK-JLTFET) offer an improvement of two orders in ON-state current, with point subthreshold slope of 40 mV/dec, and a high I_{ON}/I_{OFF} ratio of $\sim 10^8$. We estimate the improvement in digital performance using 'I_o/C_{in}' (I_D/C_{GG}) and analog performance using unity gain frequency 'f_T' as the figure of merit. We observe that the proposed ADK-JLTFET offers 30 times increase in I_o/C_{in} and 24 times increase in f_T as compared to JLTFET with only low-k spacer. Due to similar working mechanism, ADK-DLTFET also shows similar improvements.

Keywords Band-to-band tunneling · High-k · Tunnel field effect transistor · Charge plasma

1 Introduction

The validity of Moore's law is shrinking day by day due to the extreme challenges posed by the shrinking dimensions of the basic metal oxide semiconductor field effect transistor. The need of ultra-sharp doping profiles for decananometer regime is becoming very difficult to achieve [1–3]. Therefore, new technologies such as tunnel field effect transistors (TFETs) are gaining wide attention due to their low subthreshold swing and low leakage current. However, they still suffer from the requirement of abrupt junctions for more efficient band-to-band tunneling mechanism [4–6]. Considering the laws of diffusion and statistical nature of dopant atoms, the fabrication of such junctions is a very challenging task for the semiconductor industry [5–7]. Thus, new transistor such as junctionless field effect transistor (JLFET) which does not have any metallurgical junction is among good options to explore [2,3,8]. Recently, a new device referred to as junctionless tunnel field effect transistor (JLTFET) which employs both the concepts of JLFET and TFET has been proposed [9]. The basic concept behind junctionless structure is charge plasma concept or gate workfunction engineering. According to this phenomenon, the p-i-n structure required for TFET operation can be formed on a silicon bar by choosing different source, drain, gate workfunctions [10]. For the device mentioned in [9], two gates (control gate, fixed source gate or p-gate for hole plasma formation) on a heavily doped n-type silicon bar are used. The formation of hole or electron plasma requires that the device thickness should be less than the Debye length given by $L_D = \sqrt{\varepsilon_{Si} V_T / qN}$, where ε_{Si} is the dielectric constant of silicon bar, V_T is the thermal voltage, and N is the carrier concentration of the body [11]. The increase in Debye length with decrease in carrier con-

✉ Mohd Adil Raushan
adil.raushan02@gmail.com

Naushad Alam
itsnaushad@gmail.com

Mohd Waseem Akram
makram1@jmi.ac.in

Mohd Jawaid Siddiqui
mjsatamu@gmail.com

[1] Electronics Engineering Department, ZHCET, AMU, Aligarh 202002, India

[2] Electronics and Communication Engineering Department, JMI, New Delhi 110025, India

centration N results in greater control of gates. Recently, a new transistor called dopingless transistor has been proposed, which uses the same concept [12]. These transistors are based on the band-to-band tunneling of electrons in valence band of source region to conduction band of the channel. The current due to tunneling phenomenon depends on the tunnel barrier height and p-i-n junction electric field. In TFETs, materials having low band gap such as Ge, SiGe, InAs, InGaAs have been used to lower the tunneling barrier [13,14]. To increase the electric field, techniques such as scaling of gate dielectric, source, and drain doping engineering have been used [15,16].

The impact of high-k spacers has been explored in FinFETs, which can significantly improve the performance of the device [17,18]. The use of dual-k spacers in FinFETs enhances the ON- and OFF-state electrostatics. The reduction in subthreshold leakage current is observed due to shift in conduction band edge with increase in permittivity of inner high-k spacer. The current in ON-state is improved due to gate fringing field lines through the inner high-k spacer, which reduce the barrier in underlap region. Asymmetric underlap dual-k spacers FinFETs show better performance than normal ones due to similar reasons [19]. However, the introduction of dual-k spacers increases the gate fringe field coupling at the cost of increased fringe capacitance. Possible fabrication technologies for symmetric dual-k spacer underlap dual gate FinFETs have also been studied before [17] and for asymmetric dual-k spacers in [19]. The use of dual-k spacers in TFETs has been studied before [20] but their impact on TFETs based on charge plasma concept has not been explored.

The use of high-k spacers for junctionless transistors (JLFET) enhances electrostatic integrity for short-channel operation [21]. In this paper, firstly we have optimized the spacer length (L_S), i.e., SiO_2, between gate and source electrodes as it affects both the drain current and gate capacitance 'C_{GG}.' Secondly, we have analyzed the impact of dual-k spacers on JLTFET and DLTFET while optimizing the inner high-k spacer length. We quantify the performance gain offered by the proposed ADK-JLTFET and ADK-DLTFET in terms of the digital and analog figure of merit I_o/C_{GG} and f_T, respectively.

The rest of the manuscript is organized as follows: Sect. 2 describes the simulation setup and calibration. Section 3 reports the performance gain by spacer length optimization of conventional JLTFET and DLTFET. Section 4 reports the proposed device structure and performance improvement by using dual-k spacers. We present the optimization of dual-k spacers and its impact on the proposed device structure in Sect. 5. Finally, Sect. 6 concludes our manuscript.

2 Device structure and simulation parameters

Figure 1 shows the cross-sectional view of the conventional JLTFET and DLTFET. All simulations are carried out using a 2-D device simulator, Silvaco Atlas [22]. The simulations for the JLTFET are carried out using the device parameters as given in [9]. For tunneling in lateral direction, the nonlocal BTBT model is used. The interface trap effects are also taken into account. The effects of Fermi–Dirac statistics are used in the calculation of intrinsic carrier concentration required in the expressions of SRH (Shockley–Read–Hall) expression. We have assumed a high-k metal gate stack, so a gate leakage current model is not required. Lombardi mobility model and SRH recombination model are used to account for high impurity atom [22]. The quantum confinement model as given by Hansch [23] is used in the same way as in [9], and the band gap narrowing model is used to consider effects of high doping. The impact of high-k spacers on Si channel for JLTFET is taken in the same manner as mentioned in [9], i.e., by considering the defects at the semiconductor and high-k spacer interface. We calibrated model parameters in device simula-

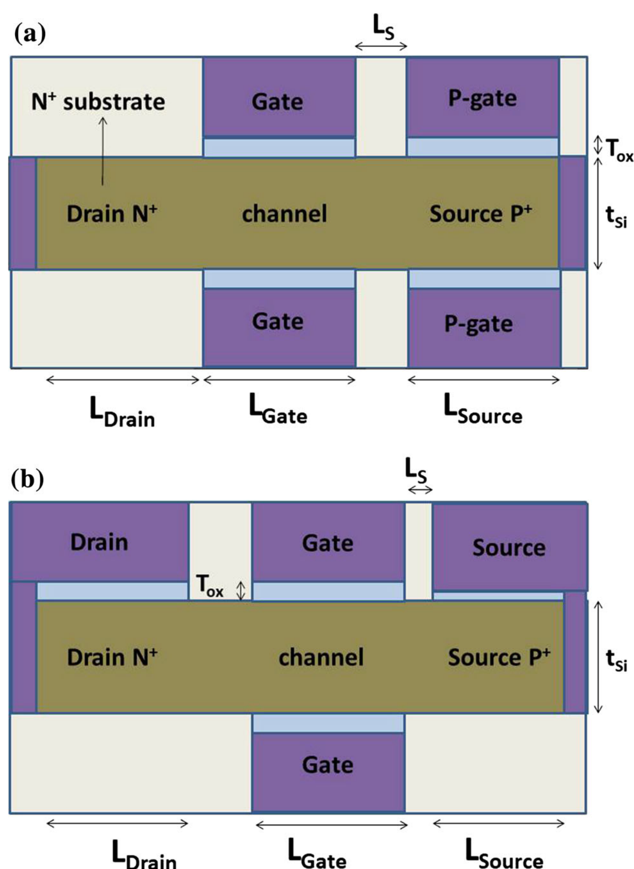

Fig. 1 **a** Cross-sectional view of the JLTFET as used in reference [9], **b** cross-sectional view of the DLTFET, showing gate, source, drain electrodes

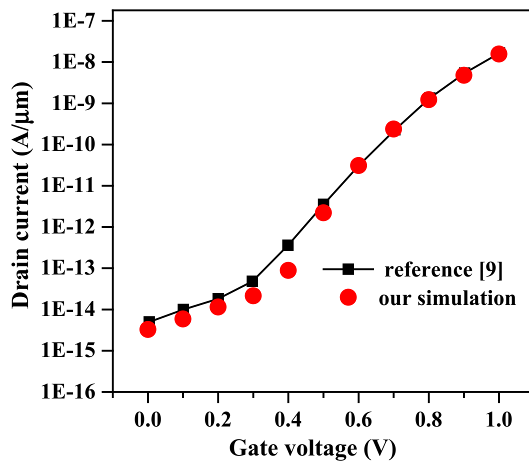

Fig. 2 Simulation setup calibrated by reproducing the experimental results reported in [9]. A reasonable agreement between our simulation models and reference results is achieved

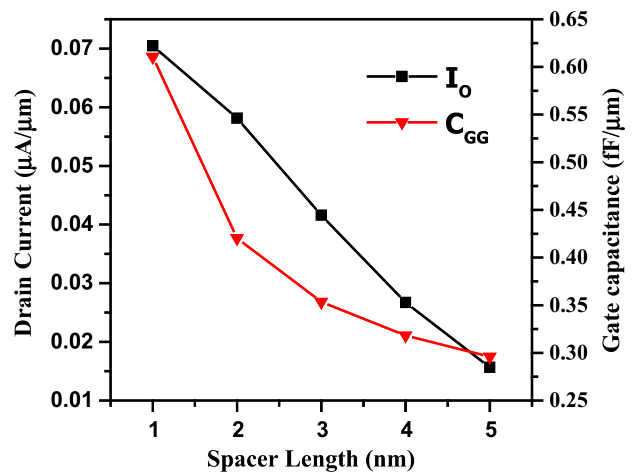

Fig. 3 Effect of spacer length L_S variation on drain current and total gate capacitance at $V_{GS} = V_{DS} = 1$ V

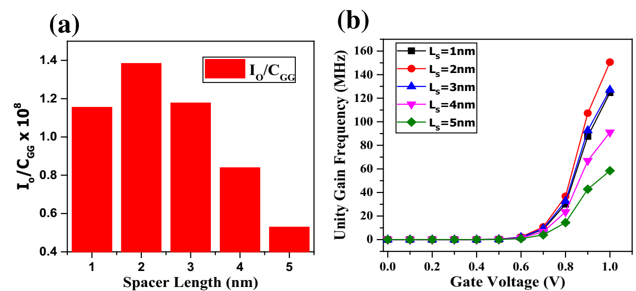

Fig. 4 **a** I_o/C_{GG} ratio versus the spacer length, **b** unity gain frequency is plotted for different spacer lengths for JLTFET

tor to match with the I–V characteristics of [9] as shown in Fig. 2.

In DLTFET, platinum (workfunction = 5.93 eV) is used for creating the 'p' source region by inducing hole plasma on an intrinsic silicon bar ($n_i = 1.0 \times 10^{15}/\text{cm}^{-3}$). The creation of electron plasma is achieved by using hafnium (workfunction = 3.9 eV). The oxide thickness used at gate is 2 and 0.5 nm effective oxide thickness (EOT) at the source electrode is used, to obtain stronger 'p-type' nature required for more efficient tunneling [12]. The spacer at gate–drain interface L_{GD} is fixed at 10 nm, and the spacer at gate–source (L_S) interface is varied. The impact of high-k spacers on semiconductor is taken in same way as mentioned before for JLTFET. The mesh spacing in the tunneling region is sufficiently narrow to effectively account for tunneling. The dual-k spacers are used only between the p-gate and control gate in JLTFET and between the source and gate in DLTFET. In this paper, different spacer architectures for optimization of digital performance (I_o/C_{GG}) and analog performance (f_T) are investigated and all the improvements are shown with respect to conventional JLTFET/DLTFET having same total spacer length (low-k only).

3 Spacer optimization for JLTFETs and DLTFETs

The device parameters such as gate length, film thickness, gate dielectric for JLTFET have been optimized before [24]. The spacer between gate and source gate/electrodes (L_S) is a very important parameter as the reduction in L_S results in increased drain current in both JLTFET and DLTFET[9,12]. However, this increase in current comes at the cost of increased gate capacitance C_{GG} because the capacitance increases when the distance between two electrodes 'L_s' decreases, as shown in Fig. 3. This increase in I_o is due to reduction of tunneling barrier between source and channel in the device. Thus, it is very important to estimate the optimum spacer length for analog and digital applications as C_{GG} plays a very important role. Considering the digital circuit applications, the output current I_o should be highest and the input capacitance C_{in} or C_{GG} should be lowest as it exacerbates the circuit delay. Thus, the ratio I_o/C_{GG} is optimized with spacer length in Fig. 4a. The highest value 1.38×10^8 is obtained for $L_S = 2$ nm. For analog applications, unity gain frequency $f_T = g_m/2\pi C_{GG}$ is a very important parameter as it determines the high-frequency performance. Thus, f_T which is inversely proportional to C_{GG} is plotted for different spacer lengths in Fig. 4b, which yields highest frequency of 150 MHz at $L_S = 2$ nm. We observe that the drive current I_o and transconductance g_m are maximum at $L_S = 1$ nm. However, the improvement in I_o and g_m at $L_S = 1$ nm is subsided by increased C_{GG} at $L_S = 1$ nm. We observe that the optimum spacer length is 2 nm at which the digital and analog performance metrics are maximum, see Fig. 4. The same optimization analysis is also performed for DLTFET, which results in optimum spacer length L_S of 2 nm as its

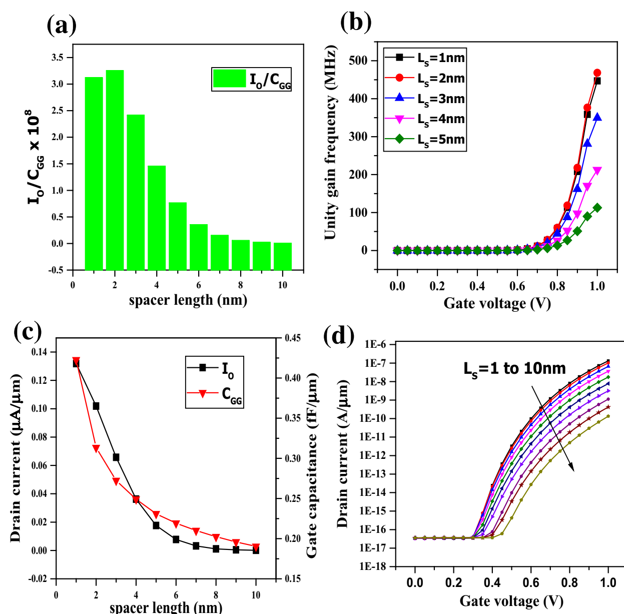

Fig. 5 **a** I_o/C_{GG} ratio versus the spacer length, **b** unity gain frequency is plotted for different spacer lengths for DLTFET, **c** effect of L_S variation on drain current and total gate capacitance at $V_{GS} = V_{DS} = 1$ V. **d** I–V characteristics of DLTFET at different L_S (highest I_o at $L_S = 1$ nm)

performance also suffers at $L_S = 1$ nm due to increased C_{GG} shown in Fig. 5a–c.

4 Impact of dual-k spacers

As we can see in the previous section, to increase I_o we need to reduce the spacer length L_S between gate and source electrodes for TFETs based on charge plasma concept. This happens due to increased gate field control on the source–channel tunneling path, which reduces the tunneling barrier [9,12]. However, the reduction in L_S increases C_{GG} as observed before. Therefore, without compromising on capacitance, we need to increase the gate field control on the junction which can be provided by dual-k spacers as shown in Fig. 6b, c. The high-k spacer used in this paper is HfO_2 (permittivity = 25), and low-k spacer is SiO_2 (permittivity = 3.9) in dual-k spacer unless specified otherwise.

4.1 High-k spacer on control gate side in JLTFETs

We propose here the use of asymmetric dual-k spacers as shown in Fig. 6 with dual-k spacer between gate and source only as in [19], as there is no significant improvement by using them on drain side [20]. The effect of dual-k spacers (high-k spacer on gate side) on tunneling can be explained by band diagrams shown in Fig. 7a. We can see in Fig. 7b that due to the gate fringing fields through the high-k spacer, the peak electric field assisting tunneling shifts toward the

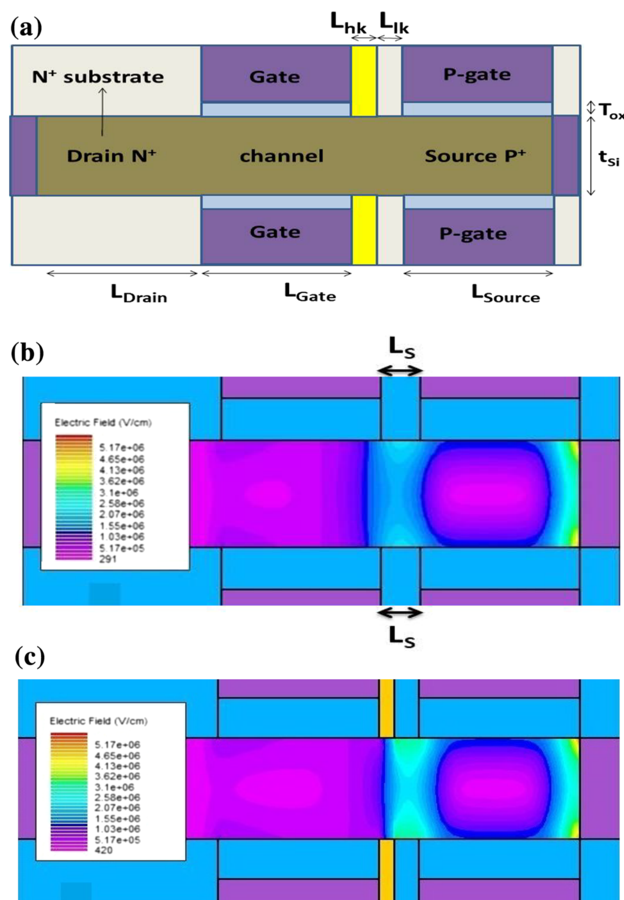

Fig. 6 For JLTFET **a** ADK-JLTFET device architecture, **b** electric field contours in ON-state ($V_{GS} = V_{DS} = 1$V) for low-k spacer only, **c** for dual-k spacer (high-k spacer shown with yellow color) between gate and p-gate (ADK-JLTFET) (Color figure online)

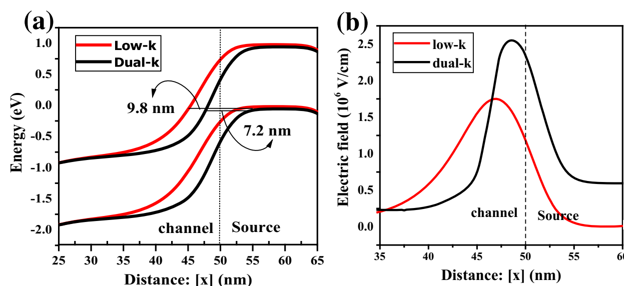

Fig. 7 For ADK-JLTFET **a** band diagram showing reduction in barrier with dual-k spacer (black) as compared with low-k spacer (red). **b** Peak electric field showing improvement with dual-k spacer (black) as compared with only low-k spacer (red) (Color figure online)

source region. There is a 1.45× increase in peak electric field, thereby reducing the tunneling barrier from 9.8 to 7.2 nm (shown in Fig. 7a) for ADK-JLTFET (2 nm high-k spacer on gate side from 45 to 47 nm), which is also consistent with the results in [20].

This reduction in barrier results in increase in drain current for ADK-JLTFET as compared to JLTFET of same

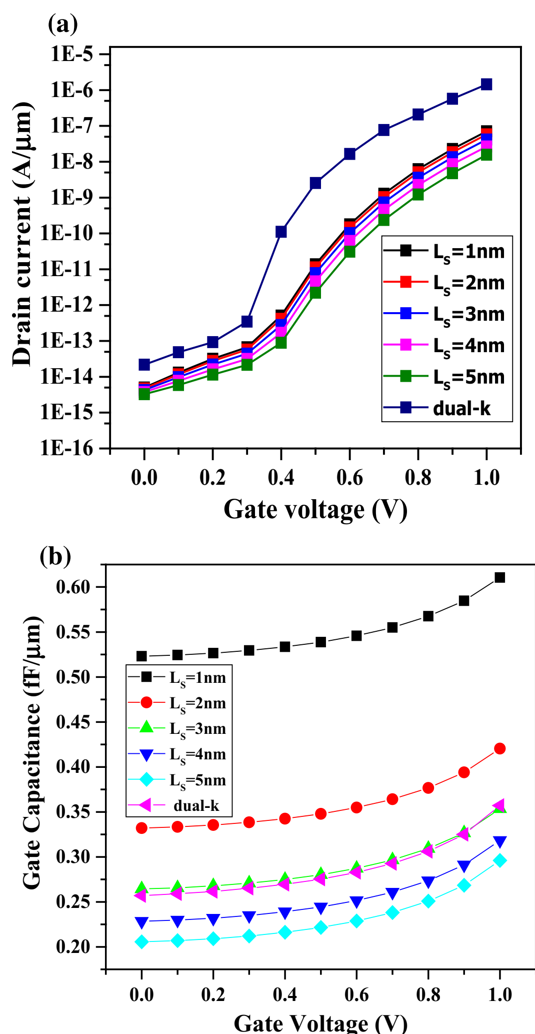

Fig. 8 For ADK-JLTFET **a** $I_D - V_{GS}$ curves for different L_S for low-k spacers compared with $I_D - V_{GS}$ curve for dual-k spacer (dark blue), **b** C–V curves for different L_S for low-k spacers compared with C–V curve for dual-k spacer (pink) (Color figure online)

total spacer length (5 nm) composed of low-k spacer only as shown in Fig. 8a. We can see from Fig. 8a that there are two orders of improvement (90 times) in ON-state current with better I_{ON}/I_{OFF} ratio as compared to JLTFET. The point subthreshold slope has also improved significantly with point SS around 40 mV/decade, which is similar to the reported TFETs (SS< 60 mV/decade) [5]. This improves the subthreshold behavior for ADK-JLTFET as compared to JLTFET. The improvement achieved is significantly higher than improvement achieved by L_S (low-k only) reduction in JLTFET even up to 1 nm as shown in Fig. 8a. From Fig. 8a, b, we can observe that the improvement in ON-state current for $L_{hk} + L_{lk} = 5$ nm is significantly large as compared to increase in capacitance C_{GG}, which is only 1.2 times for the same total spacer length ($L_{hk} = 0$, $L_{lk} = 5$ nm) in JLTFET. But the capacitance with dual-k spacer ($L_{hk} + L_{lk} = 5$ nm) is 40% smaller than the capacitance with (only low-k spacer) $L_S = 1$ nm in JLTFET, and even less than the optimized spacer length ($L_S = 2$ nm) of Sect. 3 in JLTFET.

4.2 High-k spacer on p-gate side in JLTFETs

The position of high-k spacer can be on either gate side or p-gate side. The basic phenomenon here is tunneling, which is due to narrowing of barrier. The improvement due to narrowing of barrier can also be achieved by using the high-k spacer on p-gate side in JLTFETs as shown in Fig. 9a. Due to fringing fields of p-gate through high-k spacer on p-gate side, the peak electric field shifts toward the channel region, which results in narrowing of tunnel barrier shown in Fig. 9b, c. There is significant improvement (11 times) in current shown in Fig. 9d, which is the aim of this work for ADKS-JLTFET ($L_{hk} = 2$ nm, high-k spacer on source side from 48 to 50 nm (Fig. 9b), with a marginal increase in capacitance.

We have taken DLTFET with gate oxide of 2 nm, EOT on source side as 0.5 nm. Due to the conceptually similar nature of DLTFET and JLTFET, the impact of asymmetric dual-k spacers is similar on their behavior. The gate fringing fields through the high-k spacer on gate side (between gate and source) shown in Fig. 10a (source here functions same as p-gate in JLTFET) provide similar results as in JLTFET. The improvement in current (54 times) is shown in Fig. 10b using dual-k spacer ($L_{hk} + L_{lk} = 5$ nm) as compared to low-k spacer ($L_{hk} = 0$, $L_{lk} = 5$ nm) for same total spacer length with a nominal capacitance cost (1.2 times).

4.3 Dual-k spacers from both ends in JLTFET and DLTFET

Another novel device architecture could be the use of dual-k spacers from both the ends (gate and p-gate/source). These transistors could provide the advantages of both the structures mentioned earlier as shown in Fig. 11a, b. As both the electrodes (terminals) are responsible for narrowing of tunnel barrier, thus the high-k spacer could be used from both the ends (source and channel). We have employed this structure in both JLTFET and DLTFET having gate workfunction as mentioned in Table 1 and source with workfunction 5.93 eV. High-k spacers ($L_{hk} = 2$ nm) are used from both the ends with low-k spacer of length $L_{lk} = 5$ nm sandwiched in between. We have been able to achieve significant improvement in drain current 'I_o' for the same low-k spacer length L_{lk} for both the devices (with and without high-k spacers from both ends) as shown in Fig. 11c, e at almost same gate capacitance 'C_{GG}. This increase in current (116×) is due to larger reduction of barrier due to fringe fields through the high-k spacers from both the sides shown in Fig. 11c. The increase in capacitance (only 1.04× increases as compared to JLTFET) is also reduced due to larger total spacer length

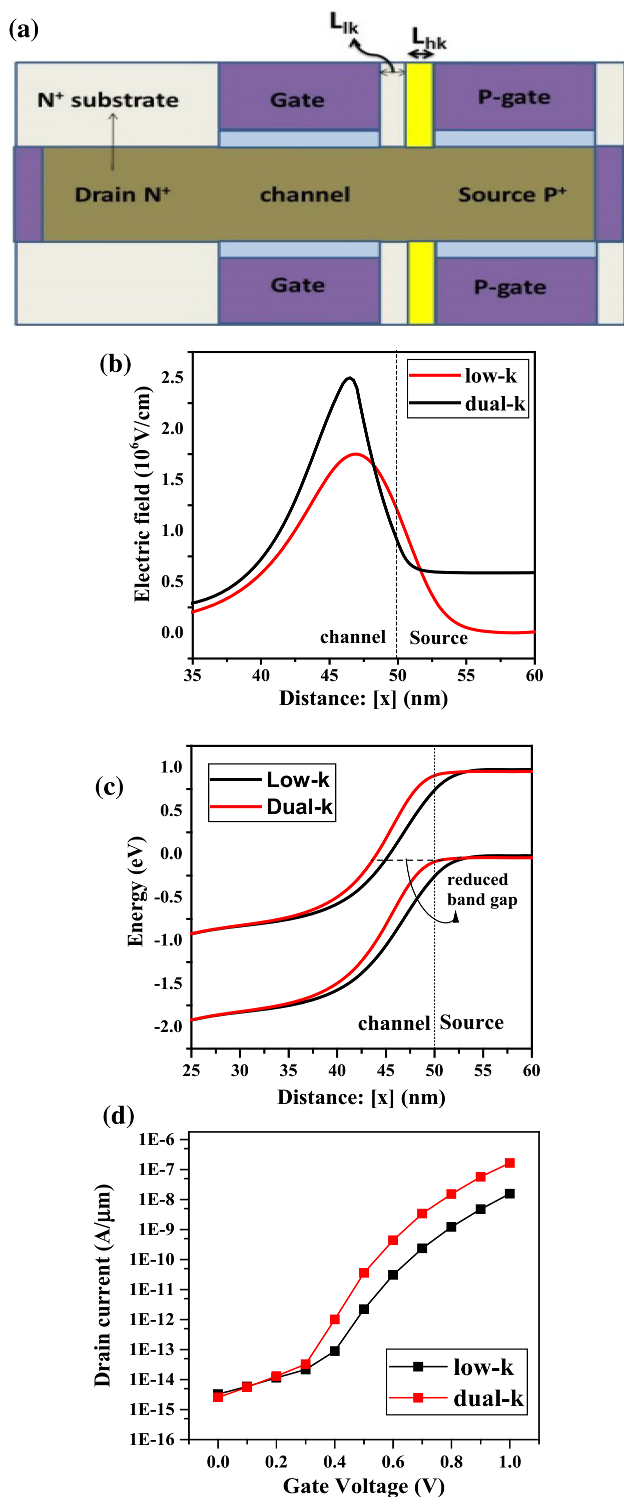

Fig. 9 For ADKS-JLTFET **a** Cross-sectional view of the ADKS-JLTFET having dual-k spacer (high-k spacer on source side), **b** peak electric field showing improvement with dual-k spacer (red) as compared with only low-k spacer (black), **c** band diagram showing reduction in barrier with dual-k spacer (red) as compared with only low-k spacer (black). **d** $I_D - V_{GS}$ curves showing improvement for dual-k spacer (red) compared to low-k spacer only (black) (Color figure online)

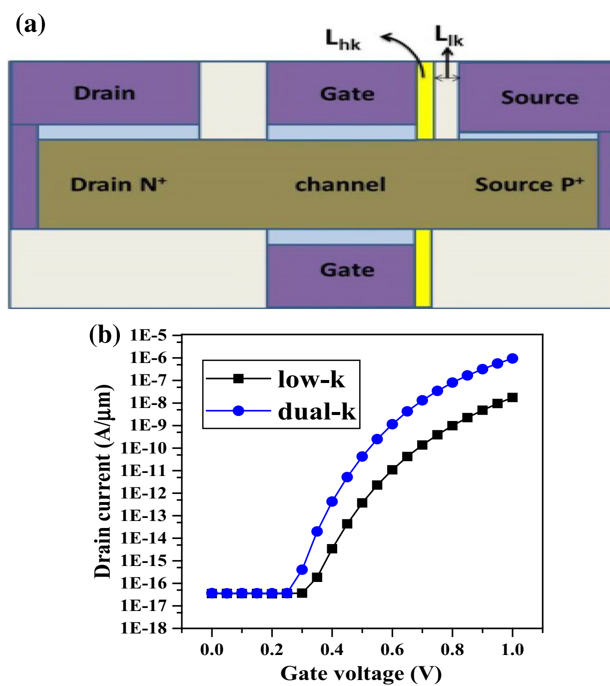

Fig. 10 **a** Cross-sectional view of the ADK-DLTFET having dual-k spacer (high-k spacer on gate side), **b** $I_D - V_{GS}$ curves for DLTFET for only low-k spacers compared with $I_D - V_{GS}$ curve for dual-k spacer ($L_{hk} + L_{lk} = 5\,\text{nm}$) showing significant improvement

($L_{hk1} + L_{lk} + L_{hk2}$), which is possible due to the use of high-k spacers from both the ends as shown in Fig. 11e. Similar improvements are also observed for DLTFET as shown in Fig. 11d, f.

5 Optimization of dual-k spacers

In this section, we have optimized the high-k spacer length in dual-k spacers while keeping the total spacer length constant. The effect of high-k spacer dielectric constant, gate oxide dielectric constant, and interface traps at HfO_2/Si interface has also been studied in this section.

5.1 Effect of high-k spacer length

The spacer between gate and source/p-gate should be composed of both high-k and low-k materials, because the use of only high-k materials deteriorates the performance due to poor HfO_2/Si interface properties. They do not provide any significant improvement in current, but increase the capacitance significantly. Hence, we have taken the dual-k architecture with high-k spacer of length 'L_{hk}' in the dual-k spacer for ADK-JLTFET with total spacer length ($L_{hk} + L_{lk}$) of 5 nm shown in Fig 6a. There are few issues with the use of inner high-k spacer also, such as increased capacitance, which worsens the circuit delay. The other problem is

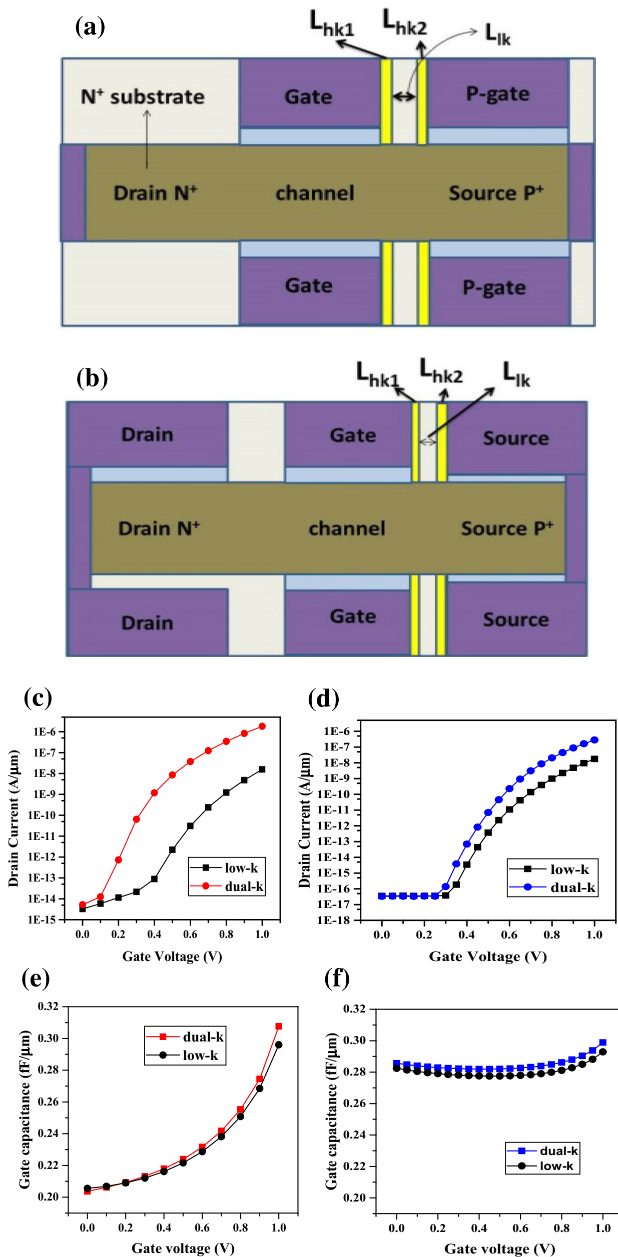

Fig. 11 **a**, **b** showing JLTFET and DLTFET having high-k spacers from both ends (gate and p-gate), **c**, **d** showing improvements in I_o for both JLTFET and DLTFET using high-k spacer from both ends (gate and p-gate), **e**, **f** showing almost equal ON-state C_{GG} for both JLTFET and DLTFET (with and without high-k spacers)

Table 1 Parameters used for device simulation

Parameters	JLTFET	DLTFET
Silicon doping N_D	$1 \times 10^{19} cm^{-3}$	$1 \times 10^{15} cm^{-3}$
Silicon thickness T_{si}	5 nm	10 nm
Gate oxide thickness T_{ox}	2 nm	2 nm
Gate workfunction	4.3 eV	4.5 eV
Oxide spacer at gate–source interface	1–10 nm	1–10 nm
Gate length	20 nm	50 nm
Oxide thickness at fixed source/source gate	2 nm	0.5 nm

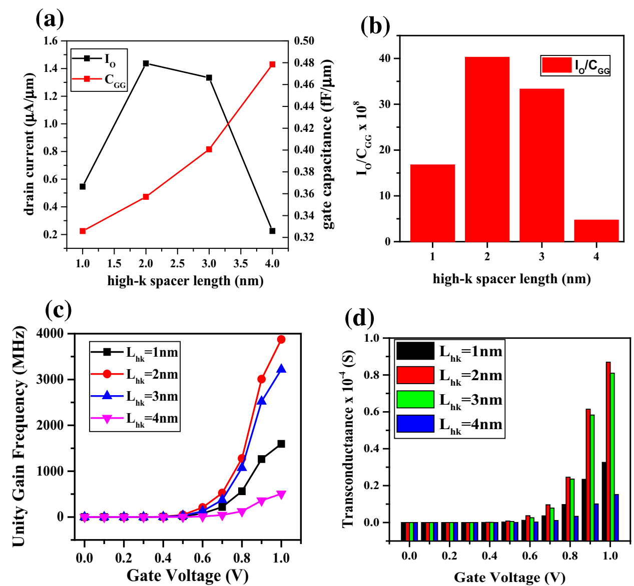

Fig. 12 For ADK-JLTFET, **a** I_o and C_{GG} for different values of L_{hk}. **b** 'I_o/C_{GG}' ratio for different L_{hk}, **c** $f_T = g_m/2\pi C_{GG}$ for different L_{hk}, **d** Transconductance g_m for different L_{hk}. The total spacer length $(L_{lk} + L_{hk}) = 5$ nm

the induced trapped charge and interface defects at HfO_2/Si interface, which further deteriorate the performance. The techniques used for optimization of L_{hk} are similar as used in Sect. 3.

For digital applications, 'I_o/C_{GG}' ratio is an important parameter explained in Sect. 3. The unity gain frequency $f_T = g_m/2\pi C_{GG}$ is considered for analog applications. The high-k spacer length 'L_{hk}' of Fig. 6b is optimized against these parameters in Fig. 12 (ADK-JLTFET). The high-k spacer length 'L_{hk}' of Fig. 9a is optimized against these parameters in Fig. 13 (ADKS-JLTFET). From Fig. 12a–d, we can observe that the optimum results for ADK-JLTFET are for the high-k spacer length $L_{hk} = 2$ nm.

The highest value of I_o/C_{in} and f_T for $L_{hk} = 2$ nm in ADK-JLTFET is 30× and 24× (i.e., 4GHz) higher as compared to JLTFET (only low-k) of same total spacer length. This value of cutoff frequency falls in the targeted RF frequency range of 0.4–30 GHz (ITRS 2015). The reason for indifferent performance for $L_{hk} = 3$, 4nm is attributed to the dominance of the poor interface properties of HfO_2/Si interface. The current I_o, g_m, f_T are highest for $L_{hk} = 2$ nm, and the capacitance is highest for $L_{hk} = 4$ nm as expected. The similar optimization analysis for the length of high-k spacer from p-gate side shown in Fig. 9a (ADKS-JLTFET)

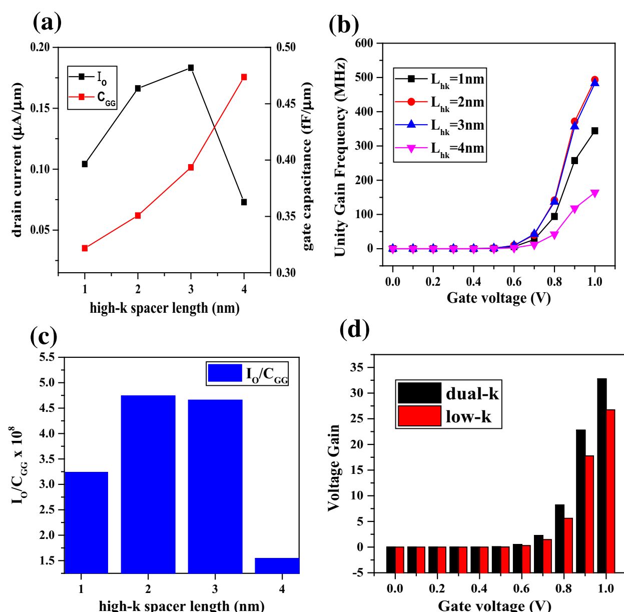

Fig. 13 For ADKS-JLTFET, **a** I_o and C_{GG} values for different L_{hk}, **b** 'I_o/C_{GG}' ratio for different L_{hk}, **c** $f_T = g_m/2\pi C_{GG}$ for different L_{hk}, **d** Improved voltage gain for dual-k spacers (black) as compared for low-k spacers (red) only (Color figure online)

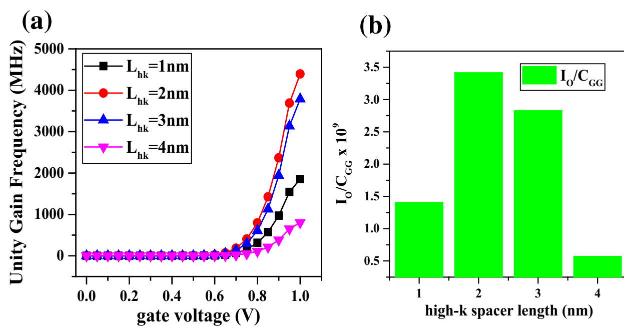

Fig. 14 For ADK-DLTFET, **a** $f_T = g_m/2\pi C_{GG}$ for different L_{hk}. **b** I_o/C_{GG} ratio for different L_{hk}

is performed, which also yields similar results with optimum high-k spacer length of 2nm as shown in Fig. 13. There is a 3× increase in I_o/C_{GG} and 3.3× increase in unity gain frequency f_T as compared to JLTFET as shown in Fig. 13a–c. In Fig. 13d, the voltage gain of ADKS-JLTFET is compared with JLTFET, which has also improved by 1.2 times (at $V_{GS} = 1$ V) due to increased transconductance g_m with dual-k spacers. Finally, we have performed the same analysis for ADK-DLTFET of Fig. 10a (high-k spacer on gate side). Fig. 14a, b shows that the best results are obtained for $L_{hk} = 2$ nm in ADK-DLTFET also. Thus, the optimum high-k spacer length for both types of transistors (ADK-JLTFET and ADK-DLTFET) is 2 nm, whether it is from source side or channel side.

The increase in dielectric constant of the high-k spacer on gate side increases the drain current due to stronger fringe

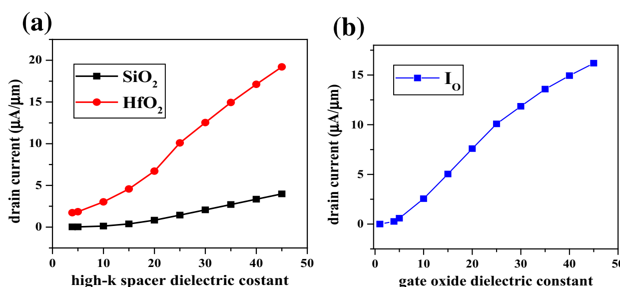

Fig. 15 **a** Effect of variation of dielectric constant 'k' of high-k spacer in JLTFET on I_o with gate oxide SiO_2, HfO_2, **b** effect of variation dielectric constant 'k' of gate oxide in JLTFET on I_{on}, ($k_{hk} = 25$)

fields of the gate through the high-k spacer with optimized value of 2 nm as shown in Fig. 6a. This behavior holds for both ADK-JLTFET and ADK-DLTFET as they both are conceptually same. As shown in Fig. 15a, b, the increase in dielectric constant of the high-k spacer in dual-k spacers or in gate oxide results in increased drain current due to the higher permittivity in high-k oxides or spacers. Thus, the use of high-k materials further enhances the performance of these transistors using dual-k spacers.

5.2 Effect of inherent traps at HfO_2/Si interface

Due to a large lattice mismatch between HfO_2 and Si, there are interface traps at the HfO_2/Si interface. Donor-type traps are positively charged/ionized when empty and neutral when they are filled with an electron. On the other hand, an acceptor-type trap is negatively charged/ionized when empty and neutral when filled with an electron. Usually, acceptor-type traps lie near conduction band edge and donor-type traps lie near valence band edge [22]. The interface traps have been taken into account by considering both types of traps [25], (a) acceptor traps having density of 5×10^{13}cm^{-2}, (b) donor traps having density of 5×10^{12}cm^{-2}. The capture cross section of both types of traps was taken from [26].

As the optimized length for high-k spacer is 2 nm which is on gate side in ADK-JLTFET (Fig. 6a) and ADK-DLTFET (Fig. 9a), the interface trap effects are not significant on ON-state current as shown in Fig. 16a, c. But these traps affect the OFF-state current in ADK-JLTFET due to increased trap-assisted tunneling shown in Fig. 16a. The larger concentration of traps at HfO_2/Si interface (acceptor and donor type) increases the trap-assisted tunneling under the high-k spacer on gate side in the OFF-state. However, the effects of interface traps are insignificant even for the worst-case scenario (for the acceptor traps, located 0.6 eV below the conduction band and for the donor traps, located 0.2 eV above the valence band [25,27]), when the high-k spacer is on source side as the tunneling happens near the gate away from high-k spacer. The interface trap effects on tunneling are negligible. Thus,

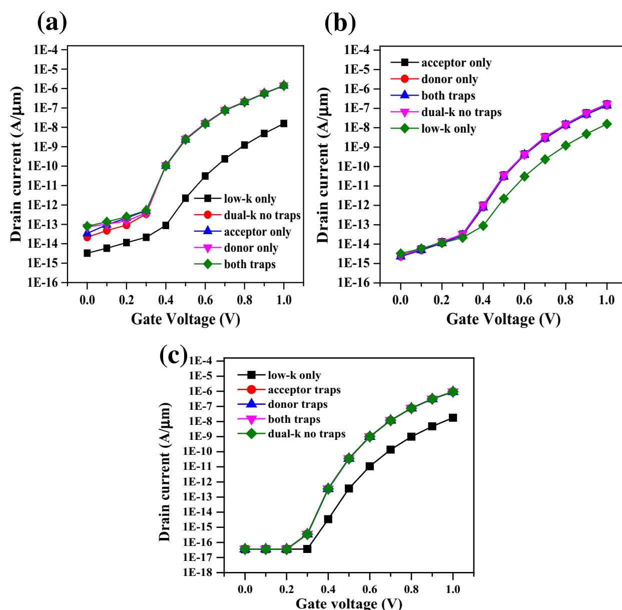

Fig. 16 **a** I–V characteristics of ADK-JLTFET for different traps (high-k on gate side). **b** I–V characteristics for ADKS-JLTFET with different traps (high-k on source side). **c** I–V characteristics for ADK-DLTFET having different traps (high-k on gate side)

we can say that the ADKS-JLTFET (high-k spacer on source side) is more immune to interface trap effects.

6 Conclusion

In this paper, we have comprehensively investigated the effects of asymmetric dual-k spacers on DLTFET and JLTFET. We have optimized the spacer length (L_S) for these transistors using low-k spacer only. We have investigated the impact of dual-k spacers and observed an improved ON-state current (two orders increase), reduced point SS, with a slight increase in capacitance (1.25×) due to the use of high-k spacers. We have also taken into account the interface properties of HfO_2/Si interface. The proposed device architecture provided increased ON-current without reducing the spacer length L_S, as reported earlier in [9,12], which severely increases the gate capacitance. Therefore, the proposed device structure can be used to enhance the analog and digital circuit performance.

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