



Reliable high-yield CNTFET-based 9T SRAM operating near threshold voltage region

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Abstract

We propose a reliable high-yield nine-carbon-nanotube field-effect transistor (9-CNTFET) static random-access memory (SRAM) cell using shared bit line and half-select-free techniques. The proposed SRAM cell operates near the threshold voltage of 325 mV. The proposed cell was also tested and verified under process variation, exhibiting stable write and read operations. Due to the reduced leakage current of the proposed cell, the power consumption is significantly decreased by 4.98-fold compared with the conventional six-transistor (6T) cell. Although the use of a CNT array increases the probability of functionality of the CNTFET, it occupies 1% more area. Due to its high I_{ON}/I_{OFF} ratio, shortest node, shared bit line, and high-efficiency read and write ports, the read and write access time of the proposed nine-transistor (9T) SRAM cell is improved by 43 and 98%, respectively, compared with the conventional 6T device. When using the low-feature-size CNTFET device in a new 9T SRAM cell, the area overhead is reduced to 32.9% compared with previously published 9T SRAM cells. The proposed cell operates with minimum supply voltage near the threshold voltage region, reducing the read and write power consumption per bit by 1.2- and 1.8-fold, respectively, compared with existing 9T SRAM cells.

Keywords Carbon nanoelectronics · CNTFET technology · High yield · Near threshold voltage · Probability of functionality

1 Introduction

As aggressive scaling of complementary metal–oxide–semiconductor (CMOS) technology approaches atomic level, the reliability of its operation becomes more challenging and requires replacement of conventional devices using new innovations such as FinFETs and CNTFETs [1–3]. The FinFET offers the significant advantage of excellent control over the threshold voltage, which reduces power dissipation [4]. However, reduction of the gate channel length of FinFETs is constrained by the gate insulator thickness [5]. In addition, scaling of the supply voltage requires a reduc-

tion in the threshold voltage to obtain stable performance. Meanwhile, CNTFET devices offer outstanding performance under ultralow-voltage operation near the threshold voltage region [6].

Variations in process, voltage, and temperature (PVT) are serious issues in memory circuits, greatly affecting their performance [7,8]. The advantage of CNTFET-based memory cells is their lower sensitive to temperature variation compared with conventional Si-based MOSFET memory cells [9]. The impact of such variations on CNTFET-based SRAM cells can be controlled using shared bit line (BL) and half-select-free techniques. The parameters of different SRAM cells have been evaluated under the effects of process variations for device operation at ultralow voltage near the threshold voltage region [10].

The threshold voltage V_t of a CNTFET varies inversely proportionally with the CNT diameter and can thus be controlled by diameter or chirality selection [10]. In this work, the same chirality vector is used for both p and n -type CNTFETs to design a CNTFET-based transistor, offering simplicity and a similar effect on the threshold voltage of both types of transistor.

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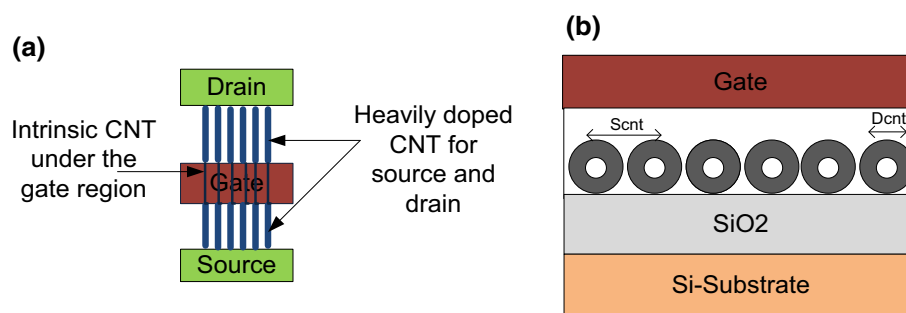
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Fig. 1 CNTFET model with diameter and pitch: **a** top and **b** cross-sectional views



Design of such memory cells for operation at ultralow voltage near the threshold voltage region is more challenging [11–15]. However, Si-MOSFET models are available for FinFETs with channel length below 32 nm, showing degraded performance due to various leakage currents, while low ON-current results in data instability [16]. CNTFET devices can be scaled down to below channel length of 10 nm, offering significantly improved power consumption and substantial performance enhancements [10]. A conventional 6T SRAM cell can be implemented using CNTFET-based transistors, offering reduced leakage current, improved read and write stability for data retention, and enhanced high-speed data transfer compared with the Si-MOSFET SRAM model. Furthermore, such 6T SRAM cells can operate at ultralow supply voltage, while aggressively scaled devices are needed to design memory cells using this new approach. This leads to the requirement for 9T SRAM cells that offer high yield and more reliable operation as well as improved read and write stability. Researchers have proposed various read and write ports to improve the parameters of such SRAM cells, including improved write and read delay, reduced leakage current, and enhanced write and read stability [17–19]. However, the use of an extra transistor increases the area overhead, which can compensate for the improvements in leakage current, read and write delay, data stability, and power consumption. We present herein a new approach to improve the performance of SRAM cells using shared bit line and half-select-free techniques under process, voltage, and temperature (PVT) variations.

The rest of this manuscript is organized as follows: A model of the CNTFET device is presented in Sect. 2. Comparisons between the conventional 6T, previous 9T, and proposed 9T SRAM cell are presented in Sect. 3. The performance and results for the conventional 6T, previous 9T, and proposed 9T SRAM cell are analyzed in Sect. 4, while final conclusions are presented in Sect. 5.

2 Model of CNTFET device

The CNTFET device can be implemented using single-walled carbon nanotubes (SWCNTs) or multiwalled carbon

nanotubes (MWCNTs), placed between the drain and source, as shown in Fig. 1a, b. Many researchers have investigated whether the CNTFET is a suitable and feasible alternative to conventional CMOS devices, because of its similar characteristics and simple manufacturing process. Figure 1a and b shows a model of the CNTFET device; a complete set of parameters for the 16-nm device is described in [20]. Figure 1a shows a top view of the ideal CNTFET model, while a cross-sectional view is presented in Fig. 1b. The notations D_{cnt} and S_{cnt} in Fig. 1b represent the CNT diameter and the array of the pitch, respectively.

2.1 Dual chirality selection

The nature of a CNT, i.e., conducting or semiconducting, can be defined using a chirality vector. The chirality selection can be represented using an integer pair (x, y) . If $x - y = 3i$, where i is an integer, or $x = y$, the CNT behaves as a conductor, while otherwise it is a semiconductor. The CNT diameter can also be obtained from the indexes x and y . Herein, a triplet index $(16, 19, 0)$ is used to describe the CNTFET structure, with $(16, 0)$ and $(19, 0)$ for the p -CNTFET and n -CNTFET, respectively. Researchers have designed and simulated CNTFET devices with various combinations of chirality vector, e.g., $(10, 19, 0)$, $(13, 19, 0)$, $(16, 19, 0)$, and $(22, 19, 0)$, for suitable adjustment of the threshold voltage [10,21]. The $V-I$ characteristic of the CNTFET device with different channel lengths is shown in Fig. 2.

2.2 Multithreshold technology

Variation of the CNT diameter has a significant impact on the performance parameters of the transistor, e.g., the I_{ON} current and threshold voltage [22]. Although process variation results show that large diameter results in significantly improved delay, this occupies greater width [23]. The channel gate width can be determined in terms of the CNT diameter as [24]

$$W_g = D_{\text{cnt}} + S(n - 1) + 2 * W_{\text{ol}}, \quad (1)$$

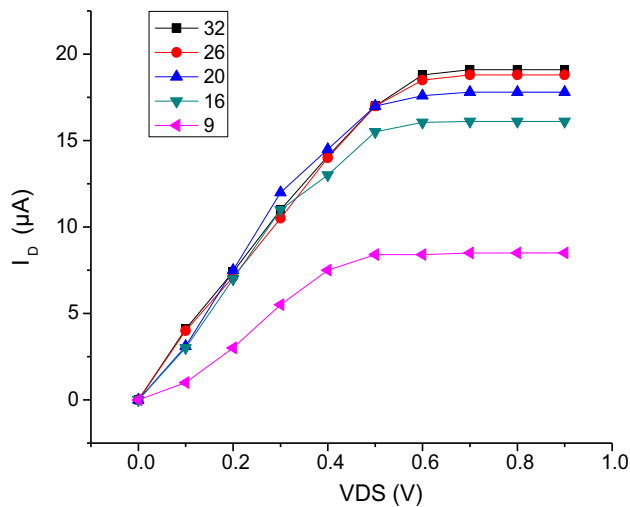


Fig. 2 V – I characteristics of the CNTFET

where D_{cnt} is the CNT diameter, S is the pitch of the uniform array, n is the number of tubes used in the CNTFET, and W_{ol} is the overlap width of the gate. The conductivity of the CNTFET can be adjusted by changing the number of tubes used. In the proposed architecture, the pitch of the array and the CNT diameter were taken to be 5.3 and 0.84 nm, respectively. For a structure with symmetrical read and asymmetrical write port, the number of CNTs in the array is supposed to be optimized at 4 and (3 and 6) in p and n-type CNTFETs respectively, to achieve high yield.

The CNT diameter can be correlated with the threshold voltage as [25]

$$V_{\text{th}} = \frac{0.577aV_{\pi}}{eD_{\text{cnt}}} \approx \frac{E_{\text{g}}}{2e}, \quad (2)$$

where e is the electronic charge, D_{cnt} represents the CNT diameter, $a = 0.243$ nm is the interatomic distance between carbons, and V_{π} is the π -bond energy between carbons. In Eq. (1), the threshold voltage is approximately half the energy bandgap. Also, the threshold voltage of a CNTFET transistor varies inversely proportionally with the CNT diameter. The advantage of multithreshold techniques is that CNTFET devices can operate with different threshold voltages. To design power-efficient SRAM cells with dual threshold voltages, low voltage threshold (LVT) and high voltage threshold (HVT) can be used to perform read and write operations, respectively. From Eq. (1), the energy band can be obtained as 0.49–0.64 eV for CNT diameter of 1.4 nm [26].

2.3 Reliability and yield

For SRAM cells operating at ultralow voltage near the threshold voltage region, reliability is a major challenge due to process variations in such nanoscale technology [26–28].

Writing data to a memory cell with ultralow supply voltage is the major constraint on conventional 6T SRAM cells. Therefore, conventional cells must be replaced by novel devices such as CNTFETs. SRAM cells based on CNTFETs offer enhanced performance and enhanced read and write stability compared with conventional 6T SRAM cells [10]. The performance and yield of CNTFET-based SRAM cells are affected by shorts or opens between the drain and source of a CNT. The probability of functionality, i.e., high yield, of SRAM cells can be increased by using an array of CNTs [29]. However, use of parallel CNTFETs with correlated CNTs increases the ON-current, while use of series CNTFETs increases the probability of semiconducting CNTs. The probability of functionality of a transistor can be defined as [30]

$$PF_{\text{tran}} = 1 - (1 - P_{\text{semi}}^n)^j, \quad (3)$$

where P_{semi} is the probability of a semiconducting CNT, n is the number of CNTs per CNTFET, and j is the number of series elements. From Eq. (3), note that the probability of functionality can be improved by increasing the number of tubes in the CNTFET device. The yield of the SRAM cell as a quality metric can be obtained as

$$QM_{\text{yield}} = \frac{\text{Array_Yield} \times \text{Read_SNM} \times \text{WVM}}{\text{Cell_}P_l \times \text{Cell_Delay}_{\text{max}} \times \text{Cell_Area}}, \quad (4)$$

where the yield of the cell can be evaluated as Array_yield, data stability is defined as Read_SNM, WVM is the write voltage margin to write new data, Cell_ P_l is the leakage current, Cell_Delay_max is the maximum delay to read and write data, and Cell_Area is the area of the SRAM cell. From Eq. (4), the yield can be evaluated, and should exceed 95 % to achieve highly reliable SRAM cells [44].

3 The 6T and proposed 9T SRAM cell

The CNTFET-based conventional 6T SRAM cell can be implemented with reduced leakage current, high performance, and improved stability for data retention in a node compared with the Si-MOSFET model. However, an aggressively scaled 6T SRAM cell cannot operate at ultralow supply voltage without use of write and read assist circuits.

3.1 Conventional 6T SRAM cell and limitations

The CNTFET-based 6T SRAM cell can be implemented with significantly improved power dissipation as well as enhanced read and write reliability. A conflict appears between read and write when they are applied simultaneously [31], and hence can be removed by using write and read assist circuits when

implementing the SRAM memory cell. A physically connected word line (WL) performs the pseudo read operation needed to isolate data [32]. Instead of using these read and write assist circuits, column read and write assist can also be used to remove this read and write conflict, as demonstrated in Fig. 3.

The different conflict combinations can be considered to minimize the supply voltage $V_{DD, \min}$ using the most probable failure point (MPFP) approach [31–33]. The minimum supply voltage $V_{DD, \min}$ is determined by successful data storage in the inverter node. In the proposed design, we consider that each transistor can have a different threshold voltage. Successful data transfer can be achieved by manipulation of the threshold voltage using a Gaussian distribution. The minimum supply voltage for read, write, and retention is assumed to be 0.325 V. In the proposed 9T SRAM device, the minimum supply voltage can be maintained by adjusting the threshold voltage by selection of the CNT diameter, the number of tubes, and the dual chirality, as well as modification of the circuit.

The CNTFET-based 9T SRAM cell architecture is less affected by temperature variations compared with CMOS SRAM devices, as shown by simulations performed in the temperature range from -10 to 90 °C [9]. For the proposed design, simulations performed at different temperatures revealed write failure below -10 °C, data flipping at 90 °C, insufficient BL swing at -10 °C, and retention of data failure at 90 °C.

The read and write assist techniques applied in the SRAM are word line A low select (WLA) and word line B high select (WLB), respectively, supported by a suppressed bit line (BL_2), negative VSS (NVSS), a negative bit line (BL_1), and transient control collapse (TVC) to remove the conflict between read and write [34–36]. In the cited work, for all conditions, the minimum load capacitance was assumed, to minimize delay. However, these techniques are not suitable for the 6T SRAM due to its unreliable operation at supply voltages near the threshold voltage region. Hence, the new approach was explored to reduce the power consumption with the minimum physical layout area. Considering all these challenges, a new 9T SRAM structure was proposed.

3.2 Drawbacks of previously published 9T SRAM cell

The CNTFET-based 9T SRAM cell proposed for more reliable read and write is shown in Fig. 4 [2]. The cross-coupled inverter is similar to in a conventional 6T SRAM cell. The transistor $x3$ and p -CNTFET $x6$ are used for write bit line access. The transistors $x7$ and $x9$ are used as a read port to isolate data from the write line. Therefore, data reading is improved compared with the conventional 6T SRAM cell. Use of a p -CNTFET transistor with an identical n -CNTFET results in current due to both electrons and holes. The layout is also optimized for high integration. The previous 9T SRAM cell design offered significantly improved leakage current, power dissipation, and write voltage margin. The

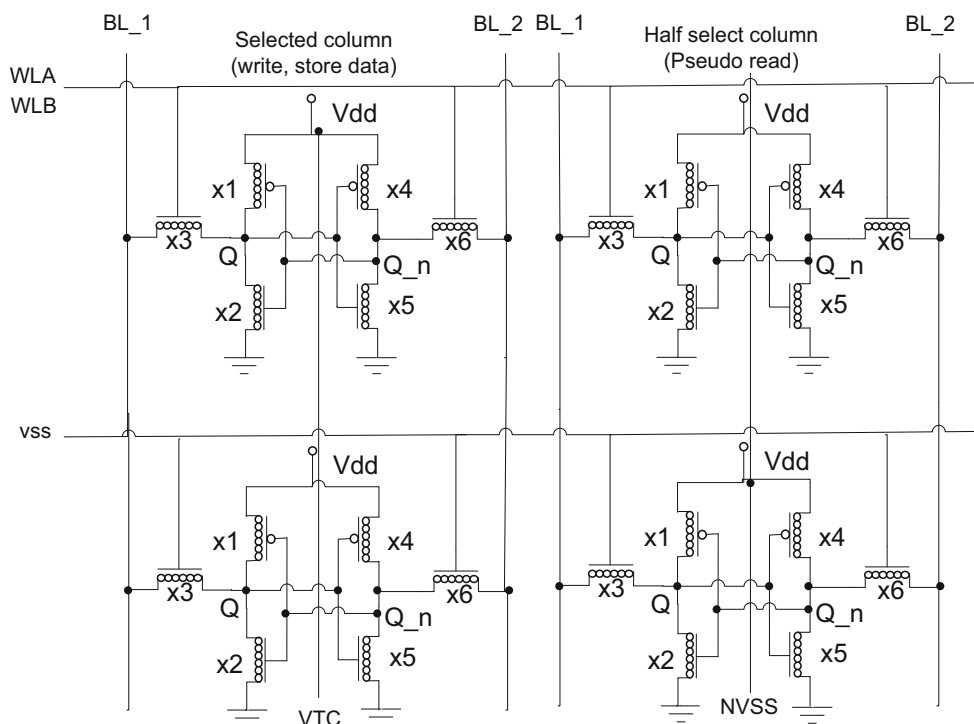


Fig. 3 Conventional 6T SRAM cell

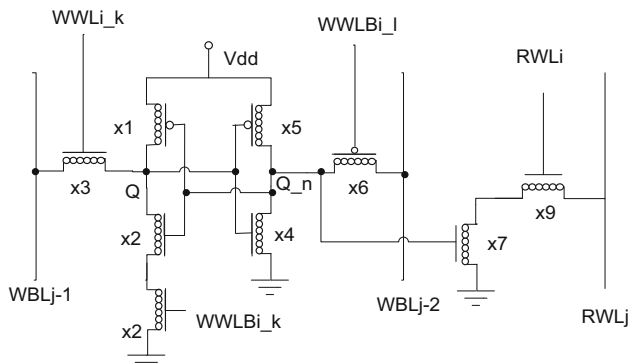


Fig. 4 Previously published 9T SRAM cell [2]

number of tubes was selected as one or two, for simplicity of circuit arrangement.

In the previous 9T SRAM design, one or two CNTs were used for the practical implementation, resulting in very low yield (assumed to be 0.0045%), which is less suitable for practical low-power applications. The half-select also results in problems, in addition to the pseudo read operation. The data conflict between read and write is also a serious issue with the previous 9T SRAM cell design. Consideration of all of these factors led to the introduction of a new, robust 9T SRAM cell using an increased number of tubes, shared bit line, and a half-select-free circuit, offering high yield. The circuit of the existing 9T SRAM cell is redrawn in Fig. 4.

3.3 Design and operation of proposed 9T SRAM cell

Various researchers have proposed 9T SRAM cells using different read and write assist combinations for reliable operation and reduced power consumption. An alternative approach to implement a CNTFET-based 9T SRAM with read and write assist ports is proposed herein, as illustrated in Fig. 5. One transistor can be removed between two adjacent cells by using a shared BL to implement the 9T SRAM

cell. This shared BL technique also removes the problem of half-select, which eliminates the pseudo read operation. In the proposed 9T SRAM cell design, single-ended read, three transistors ($X7$, $X8$, $X9$), and a pair of transistors ($X1 - X9$ and $X5 - X8$) are used to form the read and write port, respectively, thereby removing the read and write conflict and also rectifying the half-select problem. The data stored in the node can be obtained by performing the read operation with the BL precharged to V_{DD} then activating the bus lines using signals RWL and RRWLA and deactivating WL and RRWLB. Using the WL signal, the read operation can be isolated from data writing in the proposed cell. The write conflict is removed in the proposed cell by using separate bus lines to select the read path instead of using the WL interleaving approach [37]. First, the BL voltage is kept at V_{DD} to perform the read operation; while storing the data 1 at node Q, the BL voltage decreases during the write operation, while for data 0 at node Q, transistor $X2$ in the read path goes off. When writing data, RWL and WL are enabled to turn on the write assist circuit, while the read assist circuit (RRWLs) goes off.

The read operation can be performed with the shared BL by disabling WL and enabling RWL and RRWLA/B, using column addressing. To write the data 0/1, RWL and WL are enabled and RRWLA/B is stored at the node pair BL1 and BL_1, assuming that the WL completely isolates the storage node pairs, which efficiently removes the half-select problem. The signal WL ensures the write half-select, completely removing the half-select problem for a sufficient difference between row and column select voltages of 25 mV, with minimum retention voltage of 325 mV. The proposed architecture completely eliminates the leakage path, hence the dynamic power consumption is drastically reduced compared with the previously published 9T SRAM cell. Furthermore, the dynamic power consumption is reduced when using the precharge scheme with the selection line [38].

The physical layout of the proposed CNTFET-based 9T SRAM cell design is presented in Fig. 6. Four extra transistors

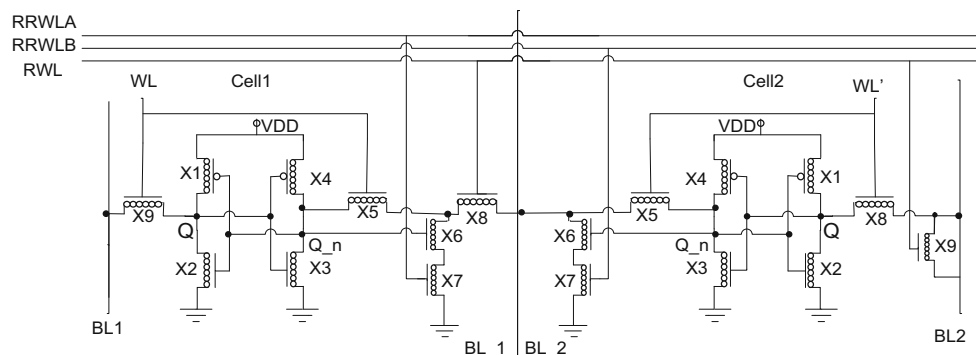


Fig. 5 Proposed CNTFET-based 9T SRAM cell with shared BL architecture

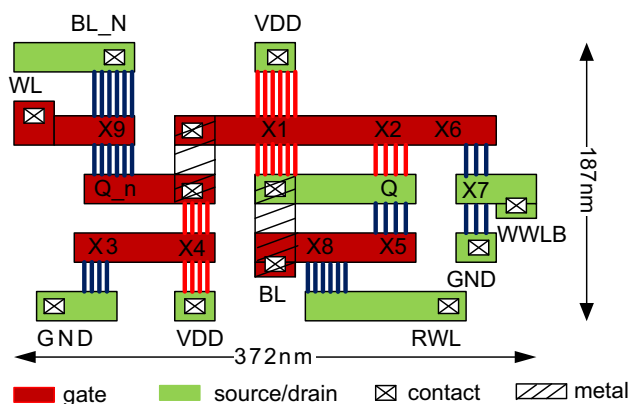


Fig. 6 Layout of proposed 9T SRAM cell design, with area of $187 \text{ nm} \times 372 \text{ nm} = 0.069 \mu\text{m}^2$

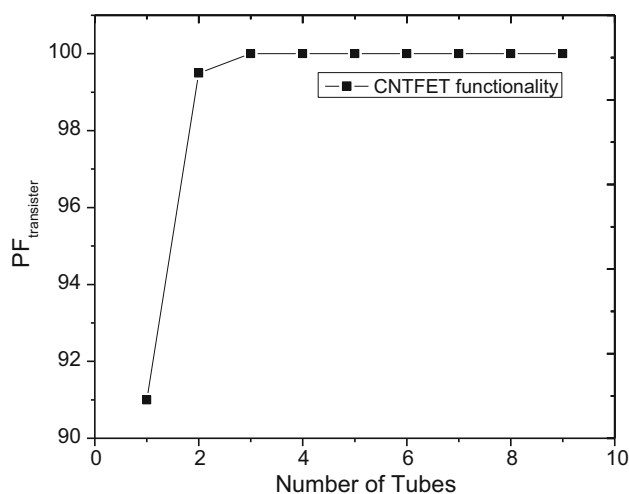


Fig. 7 Probability of functionality of CNTFET

(*X6*, *X7*, *X8*, and *X9*) are used to implement the proposed cell, which therefore occupies 18 % greater area compared with the conventional 6T SRAM cell. Due to the shared bit line technique used in the proposed CNTFET-based 9T SRAM, it occupies 4.8 % less area compared with the 9T Si-MOSFET SRAM cell at the same technology node. The use of an increased number of tubes enhances the probability of functionality and results in acceptable yield, albeit increasing the area by 1 % as shown in Fig. 7.

4 Performance and results analysis of 9T SRAM cell

The proposed CNTFET-based 9T SRAM cell has been optimized for an applied voltage near the threshold voltage of 325 mV. Simulations were performed in HSPICE using CNTFET compact model codes for 16-nm technology, to evaluate the different parameters [6].

4.1 Read and write ability test

The voltage transfer characteristic can be changed by properly adjusting the size ratio of the transistors. CNTs of constant size were applied to implement the proposed cell with enhanced read and write ability [39–41]. The proposed 9T SRAM exhibits improved read and write ability near the threshold voltage at 325 mV compared with the 6T SRAM cell. The write ability of the different SRAM cells was defined as the write noise margin and evaluated here to analyze the performance of the different SRAM cell designs. Wider read and write SNM indicates greater stability when reading and writing data. The dedicated read and write assist circuit provides increased ability to read and write data. The dual diameter selection in the CNTFETs results in the enhanced performance metrics, i.e., significantly reduced delay, mitigation of leakage current, and increased read and write ability. The dual diameter selection also has a positive impact on the $I_{\text{ON}}/I_{\text{OFF}}$ current ratio [42].

4.2 Minimum supply voltage V_{DD}

Aggressive supply voltage scaling degrades the performance of the 6T SRAM cell in the absence of parametric variation in the device. Furthermore, the performance can be improved by read and write assist circuits and dedicated read and write lines with row and column select. The supply voltage was scaled in the range from 0.2 to 1 V to determine the best operating voltage for the operating frequency range of 1.2 MHz to 1.8 GHz. The proposed 9T SRAM cell operating near the threshold voltage region of 325 mV at frequency of 1.25 GHz exhibited the best performance.

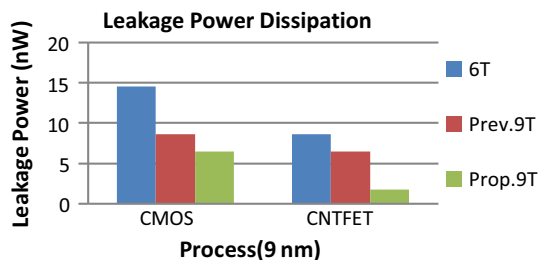
4.3 Leakage current analysis

Table 1 presents the leakage current evaluated for the conventional 6T, previously published 9T, and proposed 9T SRAM cell designs. The average leakage current to retain the data 1/0 was evaluated, due to the asymmetric structure of the 9T SRAM cell. Using the dedicated read and write assist circuit, the proposed 9T SRAM cell exhibited the minimum leakage current when compared with the conventional 6T and previously published 9T SRAM cells, by 49.8- and 9.7-fold, respectively [18].

The average leakage current per bit for the proposed 9T SRAM cell was evaluated as 1.83 pA consuming power of 0.549 pW for supply voltage of 0.3 V, or 2.4 pA consuming power of 0.168 pW for supply voltage of 0.7 V. The minimum leakage current achieved for supply voltage of 325 mV was 2.0 pA consuming power of 0.75 pW. The proposed 9T SRAM cell consumes the minimum leakage power when compared with the previous 9T SRAM cell at the same technology node. As shown in Fig. 8, the proposed 9T SRAM

Table 1 Evaluation of write power and leakage current of SRAM circuits in 16-nm CNTFET technology

Parameter	6T SRAM [2]	Previous 9T SRAM [2]	Proposed 9T SRAM
Computed write power (nW)	173.6	32.41	4.45
Computed read power (nW)	68	33.2	5.47
Evaluated leakage current (nA)	2.89	2.24	0.87

**Fig. 8** Leakage power consumption of different SRAM cells

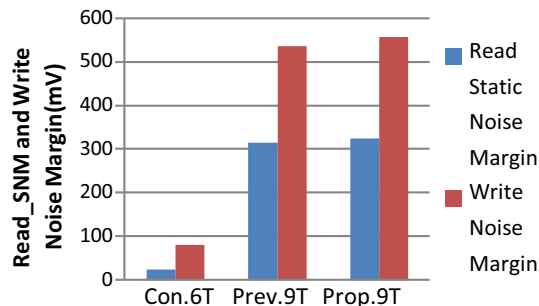
cell offers the minimum leakage power consumption and dissipation.

4.4 I_{ON}/I_{OFF} distribution

Placement of a CNT between the drain and source with local oxidation enhances the I_{ON} current, resulting in reduced leakage current and improved data stability. Use of high voltage threshold (HVT) technology and a similar number of CNTs enhances channel formation, thereby increasing the I_{ON}/I_{OFF} ratio. The modification in the dedicated read and write assist circuit of the proposed 9T SRAM also improves the I_{ON}/I_{OFF} ratio. Also, the use of dual diameter selection offers excellent control over the threshold voltage, increasing I_{ON} for low supply voltage. The wider SNM provides stable data operation, improved by 99.58% in the proposed 9T SRAM cell as compared with the 6T device shown in Fig. 9. Due to the use of the modified CNTFET device, the proposed 9T SRAM cell has very high I_{ON}/I_{OFF} current ratio of 2×10^4 , providing 1.83-fold higher switching speed compared with the previously published 9T SRAM cell. The delay for the proposed 9T SRAM cell to move the data 0 onto Q and 1 onto Q_n is improved by 13.58 and 8.5-fold as compared with the 6T device and previously proposed 9T SRAM cell [26].

4.5 Power consumption

The average read and write power consumption were evaluated for the proposed 9T SRAM cell, the previously published 9T SRAM cell, and the conventional 6T SRAM cell. Compared with the conventional 6T SRAM cell, the proposed 9T SRAM cell showed 12.4-fold less read power consumption at operating frequency of 1.25 GHz. The ded-

**Fig. 9** Read and write noise margin for different SRAM cells

icated read and write line isolate the data and completely cut off the leakage current path, hence reducing the dynamic power dissipation. Therefore, the proposed 9T SRAM has power consumption of 12.1 nW at 325 mV, while the previously published 9T SRAM cell and conventional 6T SRAM cell consume 65.7 and 272.8 nW, respectively. The write power consumption of the proposed 9T SRAM cell was found to be 11 nW, which is 1.63-fold lower than that of the previously proposed 9T SRAM cell. At the minimum operating voltage of 0.325 V, the proposed 9T SRAM cell consumes a worst-case average read and write power of 0.0138 nW per bit. However, the high voltage threshold reduces the delay when performing a write operation on a node, increasing the power consumption. To minimize the power consumption, low voltage threshold (LVT) is applied for read operations.

4.6 Stability test

The read and write stability of the 9T SRAM cell was evaluated by analysis of the read and write voltage margin. The use of the dedicated read and write line resulted in a wider SNM compared with the conventional 6T or previously published 9T SRAM cell, as presented in Fig. 9. Proper adjustment of the transistor ratio also resulted in a significantly improved noise margin. The transistor size ratio was taken as 1.4 for $X5/X6$ and 1.8 for $X1/X9$ to obtain better SNM. A wider SNM provides higher data stability. The proposed 9T SRAM cell achieved read SNM of 345 mV and write voltage margin of 576 mV, as shown in Table 2.

Table 2 Optimized parameters of different 9T SRAM cells

Parameter		65-nm CMOS process [8] 6T	65-nm CMOS process [31] Prev.9T	16-nm CNTFET process [2] Prev.9T	16-nm CNTFET proposed herein 9T
Write delay (ps)	1 (Q)	104	78	74.36	64
	0 (Q)	19	8.53	9.12	8.2
Read delay (ps)		128.4	102	93.7	92
Energy (fJ)		4.51	3.68	2.85	1.92
Area (μm^2)		0.44	1.83	0.0812	0.079

4.7 Read and write delay analysis

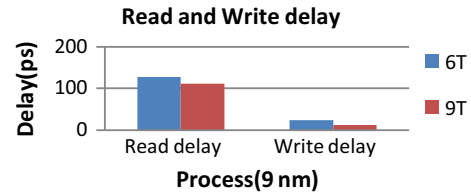
The read and write delay were evaluated for the different SRAM cells and are presented in Fig. 8. The write speed was improved by 1.89-fold compared with the conventional 6T SRAM cell. Due to the dedicated read line, the read delay was improved by 46.5 and 32 ps, respectively. When using the write port in the proposed cell to write the data 1 or 0, the delay was evaluated as 32 and 4.3 ps, respectively. The read and write delays for the different SRAM cells are compared in Fig. 10 and presented in Table 3.

4.8 Layout area

Despite offering significant advantages in terms of data stability, high-speed read and write, and improved overall design metrics, the proposed 9T SRAM cell increases the physical layout area for 16-nm technology. Although the use of a CNT array increases the width by 1%, it also improves the probability of functionality by 1423-fold and enables high yield under process variations. The physical layout area is $0.187 \mu\text{m} \times 0.372 \mu\text{m}$ ($0.069 \mu\text{m}^2$), which is 3.1-fold less compared with the Si-MOSFET based 9T SRAM cell. The conventional 6T SRAM cell occupies an area of $0.856 \mu\text{m}^2$ when using 65-nm CMOS technology. Optimization of the design for a 32×32 bit array of the proposed 9T SRAM cells results in a physical layout area of $71.23 \mu\text{m}^2$. Due to transistor sharing between the proposed SRAM cells, this is 3% less compared with the previous 9T SRAM cell.

Table 3 SNM and power consumption of different 9T SRAM cells

Parameter	65-nm CMOS process [8] 6T	65-nm CMOS process [31] Prev.9T	16-nm CNTFET process [2] Prev.9T	16-nm CNTFET proposed herein 9T
Read SNM (mV)	25	270	315	345
Write voltage margin (mV)	81.3	450	535	576
Leakage power dissipation (nW)	14.6	NA	8.1	1.78
Average read power (μW)	64.7	0.16	0.033	0.028
Write power (μW)	68.64	54.18	32.42	27.47

**Fig. 10** Write delay analysis of different SRAM cells

5 Conclusions

The challenge of implementing conventional 6T SRAM cells using aggressively scaled devices can be overcome by using a novel CNTFET design [43]. An array of CNTs is used to increase the probability of functionality and the yield of 9T SRAM cells [44]. The reliability of the proposed cell is enhanced by removing all possible open and short nodes from the CNTFET. Variation of the CNT diameter is applied to achieve multithreshold voltage and adjust the supply voltage to near the threshold voltage region. The proposed SRAM cell design offers significantly improved read and write delay due to the dedicated read and write port, respectively. The proposed SRAM cell was also tested and verified under process, voltage, and temperature (PVT) variations to confirm its robust and stable read and write operations. Shared bit line and half-select-free techniques were applied to reduce the number of transistors and remove the read and write conflict, respectively. The proposed cell occupies a very small area, 3.2-fold less than for conventional technology, due to

the shared bit line and use of ultralow-feature-size CNTFET devices.

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