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Controlling ambipolarity with improved RF performance by drain/gate work function engineering and using high κ dielectric material in electrically doped TFET: proposal and optimization

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Abstract This article proposes a novel device structure of electrically doped tunnel FET with drain/gate work function engineering by using hetero-dielectric material for the suppression of ambipolar behavior with improved DC and RF characteristics. For this, a P–I–N type structure was formed over an intrinsic silicon wafer by applying negative and positive voltages to create source and drain regions, respectively. Formation of source and drain regions by the concept of electrical doping is useful for reduction of random doping fluctuations and fabrication complexity. For suppression of ambipolar behaviour, the drain electrode is split into two different metal work functions ($\phi_{\mathrm{DE1}} < \phi_{\mathrm{DE2}}$), which alters the carrier concentration and increases the tunneling barrier at the drain/channel interface. Consequently, the proposed modification in terms of dual work functionality at the drain terminal offers better performance in terms of suppression of negative conductance (ambipolar current) and parasitic capacitances. However, the presence of dual work functionality at the drain electrode causes degradation in ON-state current and RF figures of merit. To resolve these problems, the control gate electrode is further split into two different work functions and uses hetero gate dielectric material, where the gate work function near the source/channel interface is greater than the gate work function near the drain/channel interface. It assists tunneling of carriers at the source/channel junction and improves ON-state current with RF performance. Apart from this, the use of hetero gate dielectric material provides further enhancement in DC and high frequency behaviour of the device.

Keywords Ambipolar current · Electrically doped · RF performance and work function engineering

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1 Introduction

In the new era of technology, the tunnel field effect transistor (TFET) has various advantages over the MOSFET in low power applications. TFET posses steep slope in conduction state (subthreshold swing <60 mV/dec.), immune to short channel effects (SCEs) such as threshold roll-off and low OFF-state current [1,2]. TFET holds these technical advantages because the flow of charge carriers is based on a quantum tunneling mechanism, which makes it a radical device and a potential replacement for conventional MOSFET [3]. But, due to miniaturization of the device dimensions, it is recently reported that process variation [random doping fluctuations (RDFs)] have become significant at the nano scale, which results in OFF-state current running unacceptably high and degrading the device performance due to reduction of abruptness at the source/channel junction [4–6]. In the case of TFET, an abrupt junction is indispensable for efficient tunneling at the source/channel interface, but it is difficult to maintain, since diffusion of dopant atoms at source/channel and drain/channel interface results in degradation of device performance [7,8].

Thus, the introduction of charge plasma [9,10], junctionless [11–14] and electrically doped [15–18] concepts are helpful for providing an abrupt junction profile, reduction

in RDFs and fabrication complexity with cost effectiveness. In the case of charge plasma TFET (CP-TFET), the formation of source and drain regions is performed by the deposition of appropriate work function metal [19]. CP-TFET achieves these benefits, but the presence of a barrier between a gate and a source electrode at source/channel interface is responsible for severe degradation in ON-state current in comparison to physically doped TFET [20]. In this regard, the formation of junctionless TFET (JL-TFET) by using an N+ doped parent substrate improves the ON-state current, subthreshold slope and threshold voltage due to presence of an N+ doped pocket layer near the source/channel junction [11], but this approach retains the issues related to physically doped TFET [8,21,22]. Further, the use of group III–V materials in hetero junctionless TFET enhances the electrical characteristics (I_{ON}, SS and V_{th}) of the device, containing the issues related to lattice mismatch [25,26]. Apart from these, performance of JL-TFET is poor with respect to CP-TFET in terms of RDFs, fabrication complexity and capital investment. Hence, investigation of TFET by the electrically doped mechanism [15,18,23], in contrast to CP-TFET, is more beneficial for formation of better abrupt source/channel and drain/channel junctions. Electrically doped TFET architecture is also useful for overcoming the fabrication challenges of physically doped TFET and JL-TFET with low fabrication cost. It also possess ambipolar conduction due to prevention of Gaussian doping profile in the drain regions, low ON-state current, high parasitic capacitance, and poor high frequency figures of merit as CP-TFET and JL-TFET. In this paper, we use the dual work function concept at the drain electrode in electrically doped TFET for the first time to suppress ambipolar behaviour and parasitic capacitances. The presence of work function engineering at the gate electrode with hetero dielectric material enhances the ON-state current and RF performance of the device. The proposed device has the advantage of a dopingless substrate, which involves a simple fabrication process similar to conventional ED-DL-TFET. Although the proposed device, DMDG-ED-DL-TFET, has some different and complex fabrication steps because of the dual metal drain and gate electrodes with hetero dielectric material, advanced nanolithography techniques make it possible. Atomic layer deposition (ALD) and ion beam deposition (IBD) facilitate a single atom layer with complete control over deposition in one cycle. ALD provides pinhole-free deposition with a wide variety of oxides [27] (Al_2O_3, HfO_2, SiO_2, TiO_2, $SrTiO_3$, Ta_2O_5) over silicon, InAs, etc. Apart from these due to the incompatibility of poly-silicon electrodes with high κ dielectric and downscaling, metal gates once again came into the picture [28]. By ALD, two different work function metals on the drain and gate electrodes can be integrated on the same wafer, which leads to fabrication simplicity [29]. From fa abrication point of view, we have considered molybdenum (Mo) as gate electrode because it possesses low resistivity $5 \times 10^{-6}\ \Omega$ cm, high melting temperature (2600 °C) and a work function adjustable by nitrogen doping. By increasing the nitrogen implantation, a low work function can be achieved through Mo, and it facilitates dual work functionality of any length on the same metal [30]. In addition to this dual work function, metal can be deposited by the technique of interdiffusion of two metals [31].

This paper is organized as follows: the device description and simulation tactics are presented in Sect. 2. Section 3 depicts the DC characteristic of the proposed device, the Dual metal drain gate electrically doped-dopingless TFET (DMDG-ED-DL-TFET), along with the conventional devices, the electrically doped-dopingless TFET (ED-DL-TFET) and the dual metal drain electrically doped-dopingless TFET (DMD-ED-DL-TFET). Section 4 shows a comparative analysis of different RF parameters of these devices. The optimization of control gate work function (ϕ_{CG2}) and spacer length between gate and source (L_{GS}) are discussed in Sect. 5. Finally, the important findings are covered in the conclusion, Sect. 5.

2 Device structure and simulation setup

Figure 1a–c shows the cross sectional view of devices ED-DL-TFET, DMD-ED-DL-TFET and DMDG-ED-DL-TFET. An intrinsic silicon wafer is used as a substrate for all the devices. Source and drain regions were created by applying −1.2 V to create the P+ region and +1.2 V to create the N+ region, respectively, to develop a P–I–N type structure over the intrinsic silicon film [17]. A thin layer of oxide is grown to prevent the formation of silicide between the semiconductor and the metal electrodes over the source and drain regions [18,19].

Nickel silicide (NiSi) has a near-mid-band gap metal work function, which is used for source and drain contacts with 0.45 eV barrier height [16,17]. From these specifications, Fig. 1a is designated as ED-DL-TFET; further dual metal work function is applied at the drain electrode of the conventional ED-DL-TFET to form a DMD-ED-DL-TFET as shown in Fig. 1b. Dual drain work function and gate work function engineering are brought together with hetero-dielectric ,i.e. HfO_2, in DMDG-ED-DL-TFET as depicted in Fig. 1c. Device dimensions and other structural parameters used in the simulation are given in Table 1.

All the electrical characteristic simulations were carried out by 2D ATLAS device simulator [24]. The models used to process the simulations were as follows:

- Auger recombination model
- Band to band tunneling model
- Shockley Read Hall recombination model
- Fermi–Dirac statistical model

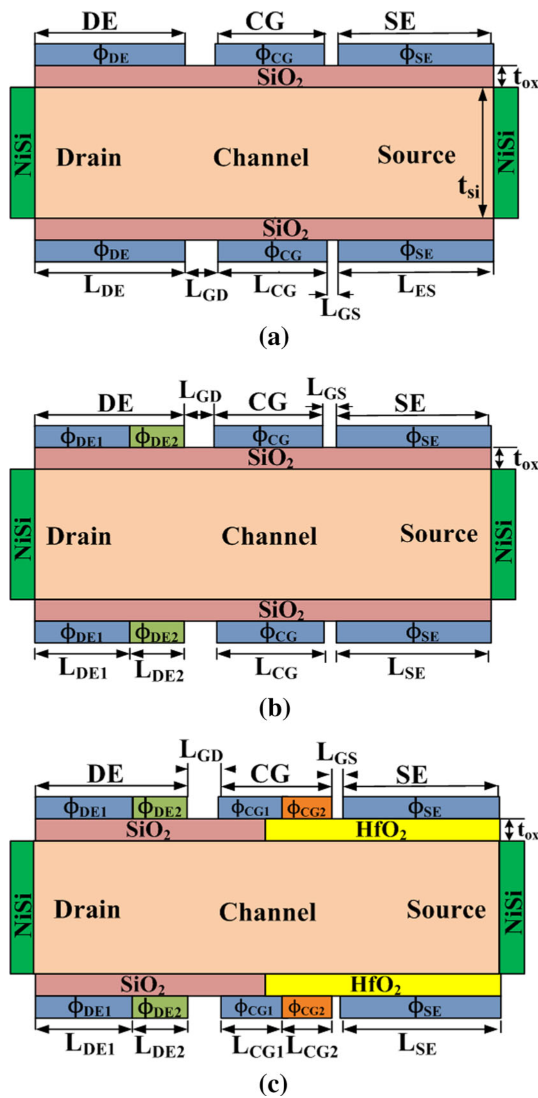

Fig. 1 Device structure of **a** electrically doped-dopingless TFET (ED-DL-TFET), **b** dual metal drain electrically doped-dopingless TFET (DMD-ED-DL-TFET) and **c** dual metal drain gate electrically doped-dopingless TFET (DMDG-ED-DL-TFET)

The universal Schottky tunneling model was also incorporated into the simulation models because nickel silicide (NiSi) was used for drain and source contacts.

3 Results and discussion

This section describes the performance and comparison of all the devices (Fig. 1a–c) in terms of energy band levels, DC characteristics and analog/RF performance.

3.1 DC characteristics

The electrically doped tunnel FET is structurally the same as the classical gated P–I–N structure, except in the formation of drain and source regions, which are created by applying positive and negative voltages over the drain and source regions, respectively. In this regard, +1.2 V and −1.2 V were applied to the drain electrode (DE) and the source electrode (SE), respectively, and were kept constant; only the gate to source voltage (V_{GS}) varied during device operations. The comparison of ED-DL-TFET, DMD-ED-DL-TFET with the proposed device, DMDG-ED-DL-TFET, in terms of electric field, energy band diagram and electron hole concentration is shown in Fig. 2a–c.

DMD-ED-DL-TFET and DMDG-ED-DL-TFET both imply dual work function metals at the drain electrode (Fig. 1b–c), whereas DMDG-ED-DL-TFET consists of dual work functions at the gate electrode along with hetero dielectric from gate to source. The impact of introducing dual work functions can be seen in Fig. 2a, which shows the electric field under thermal equilibrium conditions. It characterises a low electric field under the drain section DE2, because of its higher work functon (ϕ_{DE2}), which means it would offer a large barrier for tunneling of charge carriers at the drain/channel junction. Further, Figs. 2b, c show the energy band diagram and carrier concentration of devices in equilibrium. Figure 2b shows significant uplift in the energy bands under DE2 for DMD-ED-DL-TFET and DMDG-ED-DL-TFET, compared with conventional ED-DL-TFET, which shows reduction in electron concentration as given by Fig. 2c. This change in carrier concentration (electrons) results in a significant rise in the energy bands in the ambipolar-state, as can be seen in Fig. 2d; thus the tunneling rate reduces due to a wider tunneling width as depicted in Fig. 3. Here it is observed that DMD-ED-DL-TFET and DMDG-ED-DL-TFET exhibit lower hole tunneling rates due to the presence of dual work functions at the drain electrode in ambipolar state.

Once again, by inspection of Fig. 2a, a high electric field is observed (which supports the higher electron tunneling rate) for DMDG-ED-DL-TFET under the control gate2 (CG2). Figure 2b i.e. the energy band diagram in thermal equilibrium shows band bending or a decrement in the energy levels under CG2. CG2 in DMDG-ED-DL-TFET is strategically placed near the source/channel interface, so that more electrons accumulate in channel region as shown in Fig. 2c. So from Fig. 2b, c, it can be asserted that the presence of CG2 reduces the tunneling width due to an increase in the carrier concentration, which in turn increases the ON-state current (Fig. 4a).

Drain work function engineering reduces the ambipolar current drastically up to the level of the OFF-state current in the DMD-ED-DL-TFET, for a range of negative gate-to-source voltages (0 V $\geq V_{GS} \geq -1.5$ V), as shown in Fig. 4a. But, at the same time, from the same figure, it is observed that the DMD-ED-DL-TFET suffers from a low ON-state current while suppressing ambipolarity, which is resolved in

Table 1 Device dimensions and structural parameters for TFETs

Parameters name/unit	Symbol	ED-DL	DMD-ED-DL	DMDG-ED-DL
Substrate doping (cm^{-3})	n_i	1×10^{15}	1×10^{15}	1×10^{15}
Drain electrode length (nm)	L_{DE}	65	–	–
Source electrode length (nm)	L_{SE}	65	65	65
Work function of drain electrode (DE) (eV)	ϕ_{DE}	4.5	–	–
Work function of source electrode (SE) (eV)	ϕ_{SE}	4.5	4.5	4.5
Silicon body thickness (nm)	t_{si}	10	10	10
Oxide thickness (nm)	t_{ox}	0.8	0.8	0.8
Length of drain electrode1 (nm)	L_{DE1}	–	45	45
Length of drain electrode2 (nm)	L_{DE2}	–	20	20
Work function of DE1(eV)	ϕ_{DE1}	–	4.5	4.5
Work function of DE2 (eV)	ϕ_{DE2}	–	5.4	5.4
Control gate length (nm)	L_{CG}	52	52	–
Length of control gate1 (nm)	L_{CG1}	–	–	40
Length of control gate2 (nm)	L_{CG2}	–	–	12
Work function of control gate (eV)	ϕ_{CG}	4.5	4.5	–
Work function of control gate1 (eV)	ϕ_{CG1}	–	–	4.5
Work function of control gate2 (eV)	ϕ_{CG2}	–	–	3.9
Gate to source spacer length (nm)	L_{GS}	1	1	1
Gate to drain spacer length (nm)	L_{GD}	5	5	5
Drain source contact	–	NiSi	NiSi	NiSi
Length of high κ dielectric (nm)	L_{HKD}	–	–	94

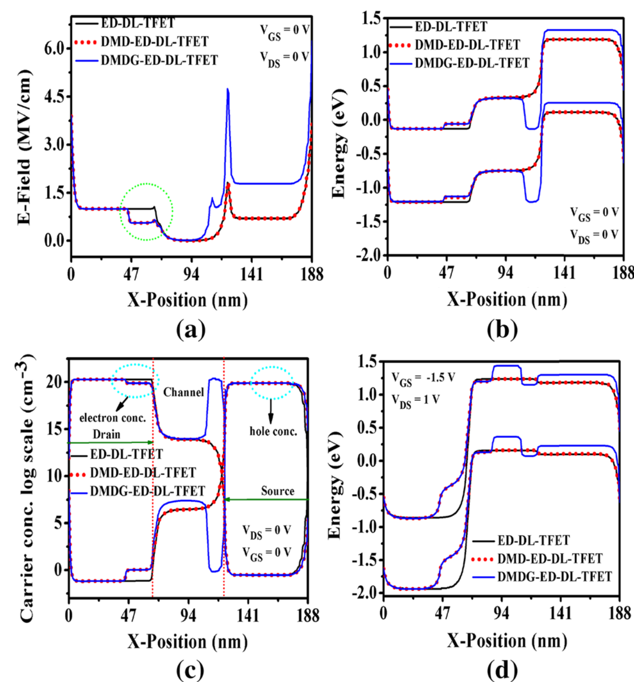

Fig. 2 **a** Electric field variation as a function of length for different device structures in equilibrium, **b** energy band profile versus length for different device structures in equilibrium, **c** carrier concentration versus length for different device structures in equilibrium and **d** energy band profile versus length for different device structures in the ambipolar state

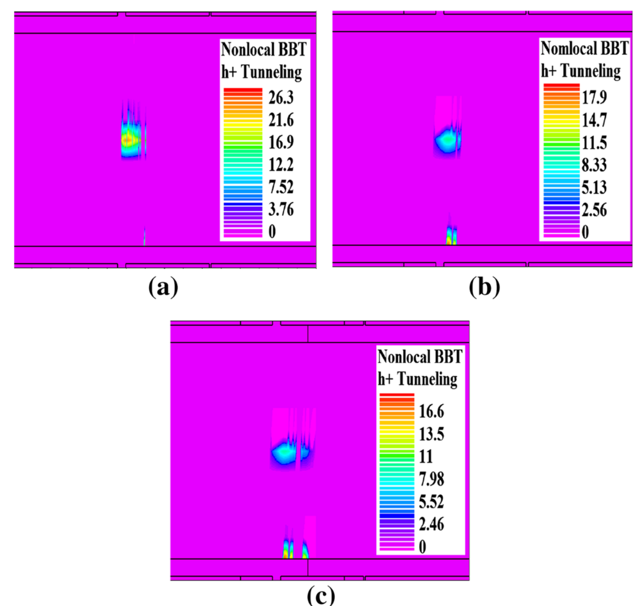

Fig. 3 Tunneling rate of holes for different devices in the ambipolar state **a** ED-DL-TFET, **b** DMD-ED-DL-TFET and **c** DMDG-ED-DL-TFET

the DMDG-ED-DL-TFET by gate work function engineering and by using high κ dielectric material. From Fig. 4b, we can see drain current as a function of V_{DS} for different values of V_{GS}. Initially, drain current increases for small

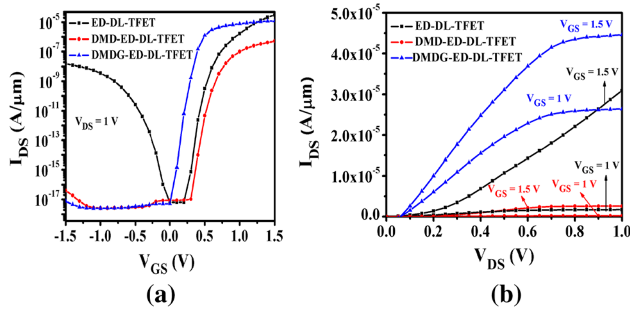

Fig. 4 **a** Transfer characteristics for different devices and **b** $I_D - V_D$ characteristics for different devices

values of V_{DS}, but after a certain drain voltage, drain current becomes independent and gets saturated. Further, from the same figure, it is noticed that DMDG-ED-DL-TFET has higher drain current and an earlier saturation point as compared to ED-DL-TFET and DMD-ED-DL-TFET, because of gate work function engineering. Moreover it has been found that DMD-ED-DL-TFET has low drain current as compare to ED-DL-TFET for $V_{GS} = (1 \text{ and } 1.5\,\text{V})$, due to work function engineering at the drain electrode (DE2). From this discussion, it is clear that two phenomena (gate work function and hetero dielectric engineering) in the DMDG-ED-DL-TFET with drain metal engineering are highly effective for enhancing ON-state current as well as suppressing ambipolar current, without any reliability issues. A comparative study of DC parameters is shown in Table 2.

3.2 Analog/RF analysis

In the present scenario, analog/RF performance is a crucial issue due to the need for low power but high frequency devices, which is a critical trade-off for device performance. Fundamental characteristics for interpreting analog performance of the device include parameters such as transconductance (g_m), output transconductance (g_{ds}), gate-to-drain capacitance (C_{gd}), cut-off frequency (f_T), gain bandwidth product(GBP), transit time (τ), intrinsic gain (IG), maximum oscillating frequency (f_{max}), early voltage (V_A) and transconductance generation factor (TGF). Transconductance is defined as the ability of a device to transform gate-to-source voltage into drain current. Transconductance g_m behaves as an increasing function for initial values of V_{GS}, but further increments in V_{GS} cause degradation in g_m because of mobility saturation of carriers (electrons). When V_{GS} increases beyond 0.37 V, in the case of DMDG-ED-DL-TFET, g_m starts increasing and attains peak value near about 0.8 V of V_{GS}, as shown in the Fig. 5a.

High κ dielectric used for half-length of the device from gate-to-source side, which also helps to improve g_m for DMDG-ED-DL-TFET due to efficient coupling of V_{GS}. Apart from these, DMD-ED-DL-TFET has lower g_m than ED-DL-TFET due to work function engineering at the drain electrode. Figure 5b shows output transconductance (g_{ds}), which is the inverse of output resistance and is defined as $g_{ds} = \partial I_{DS}/\partial V_{DS}$ (A/V), where I_{DS} is drain current and V_{DS} is drain voltage. From the same figure, we can observe that initially g_{ds} increases as a function of V_{DS} and, after a certain voltage, it falls with V_{DS}. DMDG-ED-DL-TFET achieves higher values of g_{ds} as compared to both ED-DL-TFET and DMD-ED-DL-TFET, due to flow of sufficient carriers from source to drain the region. In addition to these, DMD-ED-DL-TFET has poorer g_{ds} than ED-DL-TFET because of lower drain current. Gate-to-drain capacitance (C_{gd}) is Miller capacitance and its accurate analysis is very important for designing high frequency circuits, since C_{gd} behaves as parasitic capacitance for lower values of V_{GS}, but for higher values of V_{GS}, it behaves as inversion capacitance ($C_{gd,inv}$) [32,33]. Both types of gate-to-drain capacitance should be as low as possible to improve switching speed of the TFET. Higher work function (ϕ_{DE2}) drain electrode DE2, causes abruptness in drain doping profile at the drain/channel interface and reduces gate-to-drain coupling, due to the fact that C_{gd} trims down drastically in the case of DMDG-ED-DL-TFET, as compared to ED-DL-TFET , asshown in the Fig. 5c. However, it can be seen from the same figure that C_{gd} of the DMDG-ED-DL-TFET is slightly greater than that of DMD-ED-DL-TFET, due to the high κ dielectric near the gate/source junction, but it is negligible. Cut-off frequency(f_t) or unity gain frequency is defined as the frequency at which short circuit current gain of the device in the common source configuration becomes unity [15]. It is formulated as

$$f_t = g_m/2\pi(C_{gs} + C_{gd}).$$

Figure 5d shows the variation in f_t as a function of V_{GS}. Note that f_t increases with V_{GS} because of increments in g_m. With further increases in V_{GS}, f_t starts falling because of some increment in C_{gd} and degradation in carrier mobility. It can be seen from the same figure that DMD-ED-DL-TFET has a lower f_t than ED-DL-TFET because DMD-ED-DL-TFET has an improved C_{gd} but poor g_m, which is comparatively more dominant than C_{gd}. Further, it is found that DMDG-ED-DL-TFET has greater g_m due to gate work function engineering, so it is clear that DMDG-ED-DL-TFET has better performance than both ED-DL-TFET and DMD-ED-DL-TFET at low V_{GS}. This indicates that the device is suitable for a wide range of frequencies in low power applications. Another important parameter of RF analysis is gain bandwidth product (GBP), which illustrates the trade-off between gain and bandwidth for a given device and follows the same trend as f_T. For a certain DC gain of 10, GBP can be formulated as follows: GBP $= g_m/20\pi$ (C_{gd}). The proposed device has high GBP due to its structural con-

Table 2 Comparison of DC parameters for all the three devices

Parameter/unit	ED-DL-TFET	DMD-ED-DL-TFET	DMDG-ED-DL-TFET
V_{th} (V)	0.67	0.5	0.41
ON current (A/μm)	3.09×10^{-5}	5.15×10^{-7}	1.24×10^{-5}
OFF current (A/μm)	6.33×10^{-18}	8.7×10^{-18}	5.15×10^{-18}
Ambipolar current (A/μm)	1.54×10^{-8}	3.95×10^{-17}	7.69×10^{-18}
Subthreshold slope (mV/dec)	18.5	25.5	9.81

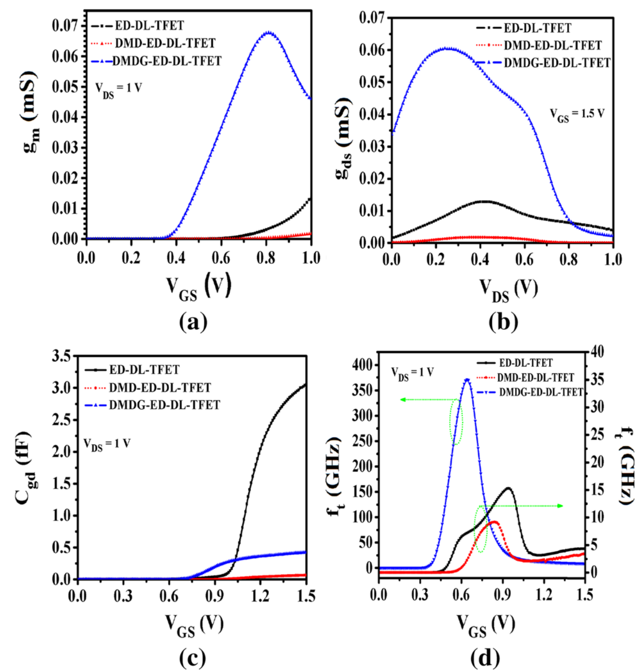

Fig. 5 Variation in **a** transconductance with gate-to-source voltage, **b** output transconductance with gate-to-source voltage, **c** gate-to-drain capacitance with gate-to-source voltage and **d** cut-off frequency with gate-to-source voltage

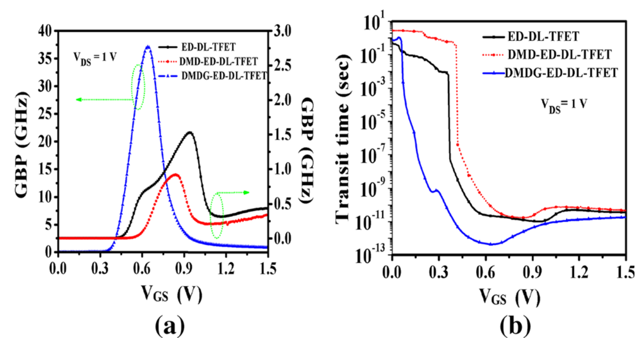

Fig. 6 Variation in **a** gain bandwidth product with gate-to-source voltage and **b** transit time with gate-to-source voltage

figuration, including a dual metal gate and high κ dielectric material near the source channel junction. This reflects that the device is able to maintain gain as well as optimum bandwidth, as shown in the Fig. 6a. However, from the same figure we can see that DMDG-ED-DL-TFET has higher values of GBP as compared to ED-DL-TFET and DMD-ED-DL-TFET. In parallel with GBP and f_t, transit time (τ) is also one of the significant parameters for defining the RF performance of the device; it measures the time taken by charge carriers to sweep out from the channel region. Transit time decides the switching speed of device, and is defined as $\tau = 1/(2\pi f_t)$, an equation that shows the dependency of τ on f_t. Figure 6b shows the behaviour of τ as a function of V_{GS} for all the three structures. τ for DMDG-ED-DL-TFET decreases rapidly with increments in V_{GS} because f_t is a function of V_{GS}; the low τ of DMDG-ED-DL-TFET represents that the sweep time of the carriers in the channel region (below the gate electrode) is much reduced when compared to ED-DL-TFET and DMD-ED-DL-TFET.

Intrinsic gain is the product of transconductance and output resistance (R_o), where R_o is the dominating factor. Figure 7a shows variation of intrinsic gain (IG) with respect to V_{GS}; it depicts high IG under the subthreshold region, which then falls with V_{GS}. Below threshold voltage, R_o is very high due to low drain current, but after exceeding V_{th} TFETs fall under the influence of BTBT, which results in a sudden rise in g_m and a drop in R_o. This action results din egradation in IG with V_{GS} [25]. DMDG-ED-DL-TFET has the highest IG at lower values of V_{GS} as compared to other two structures. f_{max} is the frequency at which the power gain of the device is unity; by the small signal model it can be formulated as:

$$f_{max} = \sqrt[2]{\frac{f_T}{8\pi C_{gd} R_{gd}}} \tag{1}$$

From the above equation, it can be seen that f_{max} includes g_m, C_{gd} and C_{gs}, which means that f_{max} is influenced by geometrical parameters. f_{max} rises with V_{GS}, then after achieving peak it falls; DMDG-ED-DL-TFET achieves 3250 THz of f_{max} higher than the other two devices as shown in Fig. 7b. High transconductance and low parasitic capacitances are two main reasons for better performance of the proposed device, which indicates that DMDG-ED-DL-TFET is suitable for high frequency applications. Figure 8a shows increments in early voltage (V_A) with respect to V_{DS} in

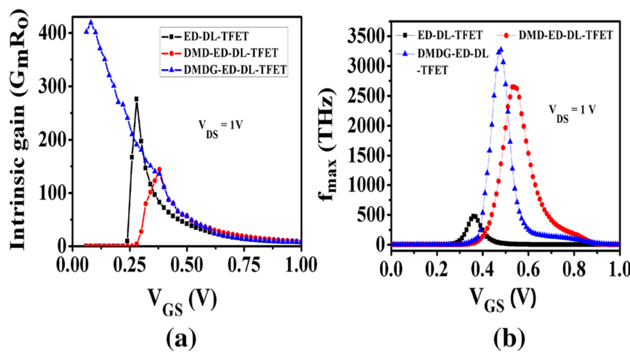

Fig. 7 Variation in **a** intrinsic gain and **b** maximum oscillating frequency with gate-to-source voltage

a comparative manner for three structures ED-DL-TFET, DMD-ED-DL-TFET and DMDG-ED-DL-TFET. DMDG-ED-DL-TFET shows higher V_A than the other two devices, because DMDG-ED-DL-TFET has a steep subthreshold slope due to the dual metal gate and high-K dielectric material at the source/channel junction [34]. High V_A results in an improvement in the low frequency open loop gain of the device.

Transconductance generation factor (TGF) refers to device efficiency in converting DC parameter (drain current) into AC parameter (g_m). It gives an idea of the degree to which a device optimizes drain current for efficient amplification with low power dissipation [35]. Under the subthreshold region, drain current is negligible and TGF presents the ratio of g_m to I_{DS}, which is why TGF has been plotted from 0.4 V (near threshold voltage) as shown in Fig. 8b. DMDG-ED-DL-TFET shows the highest TGF as compared to ED-DL-TFET and DMD-ED-DL-TFET near threshold voltage, but further increments in V_{GS} cause a fall in TGF for all structures, because after V_{th}, the drain current increases rapidly with V_{GS} and the drain current, rather than g_m, behaves as the dominating factor in the case of TGF.

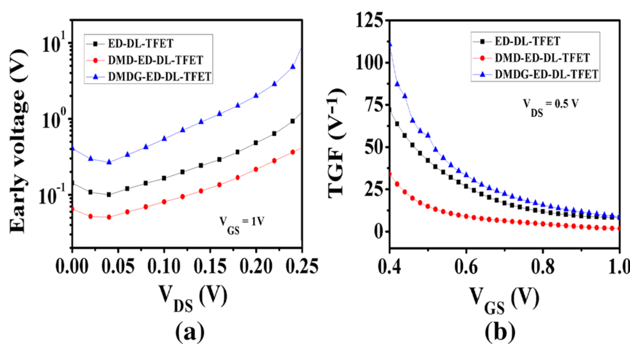

Fig. 8 Variation in **a** early voltage and **b** transconductance generation factor with gate-to-source voltage

4 Optimization

4.1 Work function optimization of DE2

Suppression of ambipolarity without any trade-off with ON-state current requires selection of an appropriate work function. This section is dedicated to the work function optimization of DE2. Figure 9a shows the energy band diagram of the DMDG-ED-DL-TFET for different drain work functions in the ambipolar state, where upliftment of bands near the drain/channel interface can be seen with increments in ϕ_{DE2}. Figure 9b shows the electric field on an enlarged scale in the ambipolar state; it presents degradation of electric field in DMDG-ED-DL-TFET under electrode DE2 as ϕ_{DE2} increases. So from Fig. 9, it can be concluded that the tunneling barrier for charge carriers increases with increments in ϕ_{DE2}.

From the Fig. 10, it is seen that significant suppression of ambipolar current occurs as ϕ_{DE2} increases from 5.0 to 5.4 eV. Although for $\phi_{DE2} > 5.4$ eV the ambipolar current is not much affected, it reduces the ON-state current by significant orders. So a sufficient amount of suppression is found in ambipolar current for $\phi_{DE2} = 5.4$ eV in DMDG-ED-DL-TFET without any compromise in the ON-state current.

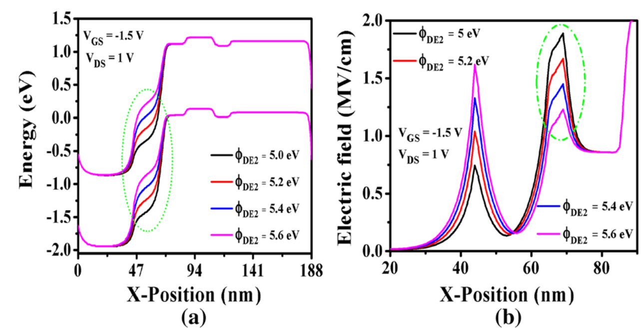

Fig. 9 **a** Energy band profile along the length of the proposed device for different work functions of DE2 under ambipolar state and **b** electric field variation along the length of the proposed device for different work functions of DE2 under ambipolar state

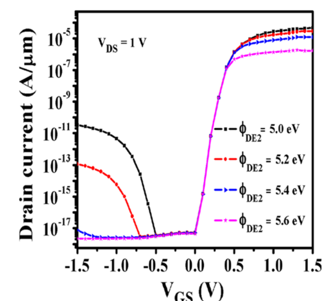

Fig. 10 Transfer characteristic of the proposed device for different work function of DE2

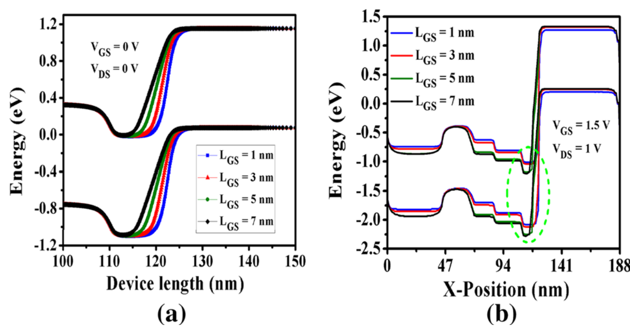

Fig. 11 **a** Energy band profile along the magnified length of the proposed device for different L_{GS} under equilibrium-state and **b** energy band profile along the complete length of the proposed device for different L_{GS} under ON-state

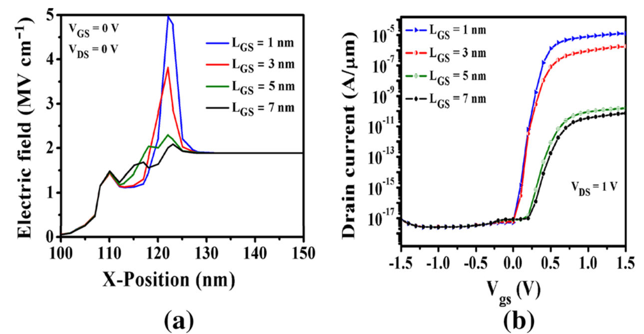

Fig. 12 **a** Variation in electric field along the magnified length of the proposed device, for different L_{GS} under equilibrium state and **b** transfer characteristic of the proposed device for different L_{GS}

4.2 Optimization of L_{GS} along with scaling of CG2

Spacer length (L_{GS}) is the gate-to-source electrode gap, which affects DC and AC characteristics of the device. Therefore, optimization of L_{GS} is necessary for desired performance of the device. Variation in L_{GS} indirectly changes the length of control gate 2 (CG2) in the case of DMDG-ED-DL-TFET. Figure 11a, b shows the energy band diagram for different spacer lengths in equilibrium and ON-state, respectively. Both the figures show increments in tunneling width as spacer length increases from 1 to 7 nm at the source/channel interface. Variation in L_{GS} also reflects changes in the electric field, where we can see higher a electric field for $L_{GS} = 1$ nm and the least electric field for $L_{GS} = 7$ nm under the spacer length as shown in Fig. 12a. The narrow tunneling width (Fig. 11a) and high electric field for $L_{GS} = 1$ nm (Fig. 12a) support a higher tunneling rate at the source/channel interface, so that ON-state current becomes optimum. Figure 12b shows the drain current versus the gate-to-source voltage characteristic for different L_{GS} values. This indicates that a change in L_{GS} does not affect the ambipolar current, but it causes a reduction in the ON-state current. For $L_{GS} = 1$ and 3 nm, ON-state current shows negligible changes, but as L_{GS} increases ($L_{GS} > 3$ nm), drastic suppression can be seen in ON-state current.

Similarly, we have plotted tarnsconductance as function of V_{GS} for different L_{GS} values as shown in Fig. 13. It is found that maximum g_m is achieved for $L_{GS} = 1$ nm, which then decreases with further increments of L_{GS}. Overall results of this optimization section are presented in Table 3, which shows the variation in several DC and AC characteristics due to changes in spacer length along with scaling of CG2.

4.3 Performance analysis of DMDG-ED-DL-TFET at $L_{GS} = 5$ nm without scaling of CG2

To ease the fabrication process, gate-to-source spacer length could be increased to 5 nm without changing the length of

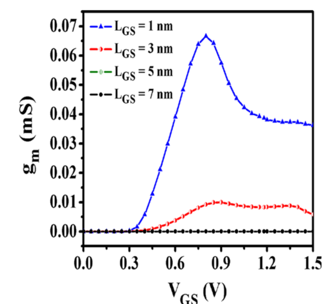

Fig. 13 Variation in transconductance with gate-to-source voltage for different values of L_{GS}

CG2. So L_{GS} increases by scaling down the drain electrode of 4 nm. This section shows the effect on device performance of choosing $L_{GS} = 5$ nm. Figure 14a shows the variation in drain current with V_{GS}; when $L_{GS} = 5$ nm, it decreases from 3×10^{-5} to 2×10^{-6}) A/μm. Transconductance (g_m) increases with V_{GS} and achieves a maximum value of 1.75 μS near about 1.4 V, as shown in Fig. 14b. Incrementing L_{GS} from 1 to 5 nm results in drastic suppression in gate-to-drain capacitance due to less coupling between the gate and drain electrodes as shown in Fig. 15a. Apart from this, cut-off frequency has an increasing trend with V_{GS}; after achieving optimum value, it drops down as shown in Fig. 15b. Cut-off frequency reaches about 200 GHz near $V_{GS} = 0.4$ V at $L_{GS} = 5$ nm.

4.4 Optimization of V_{GS} and V_{DS}

For optimization purposes, both supply and gate voltages are scaled down to 0.5 V. The effect of scaling on DC and RF performance of DMDG-ED-DL-TFET is analysed in this section. Figure 16a shows $I_D - V_{GS}$ characteristic of the three structures at $V_{GS} = V_{DS} = 0.5$ V. Maximum values of drain current for ED-DL-TFET and DMD-ED-DL-TFET degraded, but the proposed DMDG-ED-DL-TFET device performed well with small changes in terms of maximum value of drain current, subthreshold swing and threshold voltage. Further variation of transconductance (g_m) with respect

Table 3 Variation in different characteristic with respect to spacer length variation

$(L_{GS})/(L_{CG2})$ (nm)	1/12	3/10	5/8	7/6
I_{on} (A/μm)	1.24×10^{-5}	1.74×10^{-6}	1.5×10^{-10}	7.2×10^{-11}
C_{gd} (Farad)	4.33×10^{-16}	2.75×10^{-16}	8.18×10^{-16}	3.78×10^{-16}
C_{gs} (Farad)	2.12×10^{-16}	3.05×10^{-17}	1.16×10^{-17}	3.78×10^{-18}
g_m (Siemens)	3.62×10^{-5}	5.8×10^{-6}	4.02×10^{-9}	2.29×10^{-9}

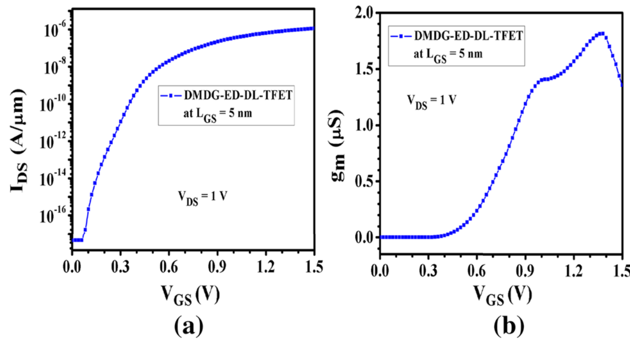

Fig. 14 **a** $I_D - V_G$ characteristics and **b** variation of transconductance with V_{GS} at $L_{GS} = 5$ nm

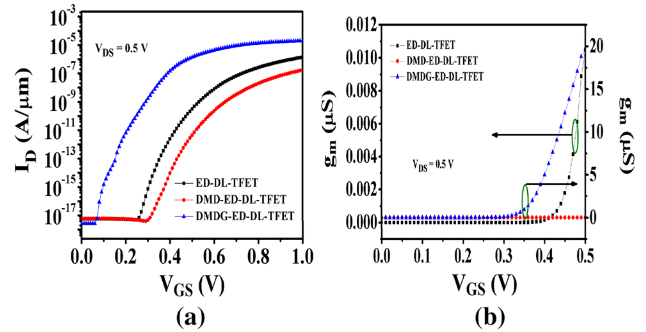

Fig. 16 **a** $I_D - V_G$ characteristics for all three structures **b** variation in transconductance for all three structures at $V_{GS} = 0.5$ V, $V_{DS} = 0.5$

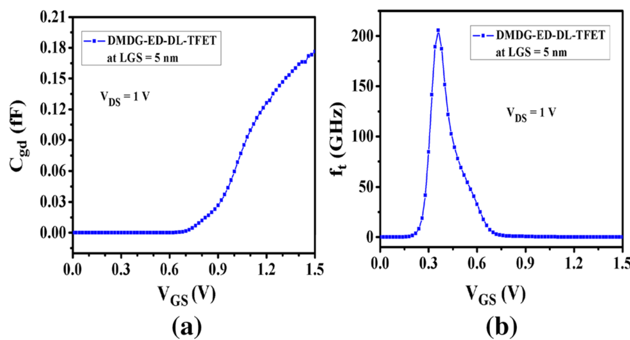

Fig. 15 Variation of **a** gate-to-drain capacitance and **b** cut-off frequency with V_{GS} at $L_{GS} = 5$ nm

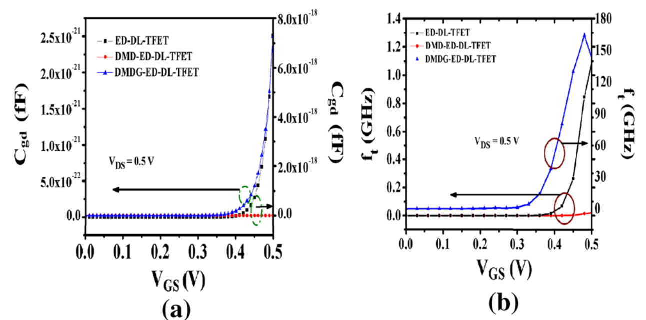

Fig. 17 **a** Variation in gate-to-drain capacitance with V_{GS} and **b** variation in cut-off frequency with V_{GS}

to V_{GS} is shown in Fig. 16b, which indicates increments in g_m with V_{GS} and DMDG-ED-DL-TFET have better performance in terms of maximum value of g_m than the other two structures. Down scaling of V_{DS} and V_{GS} results in reduction in C_{gd}, due to less coupling between the gate and drain electrodes, as shown in Fig. 17a. Unity current gain frequency increases with V_{GS}. DMDG-ED-DL-TFET has highest cut-off frequency (165 GHz) as compared to DMD-ED-DL-TFET and ED-DL-TFET, due to drastic suppression of c_{gd} at scaled $V_{GS} = V_{DS} = 0.5$ V as shown in Fig. 17b.

4.5 Performance analysis of DMDG-ED-DL-TFET with alignment and misalignment of the dual-metal gate and the hetero-gate dielectric interface

The length of high-K dielectric material is 94 nm and LCG2 = 12 nm (110–122 nm), so there is a misalignment of 16 nm between the interface of the dual material gate and the hetero-gate dielectric interface in DMDG-ED-DL-TFET, which is purposely created. If they are aligned then device

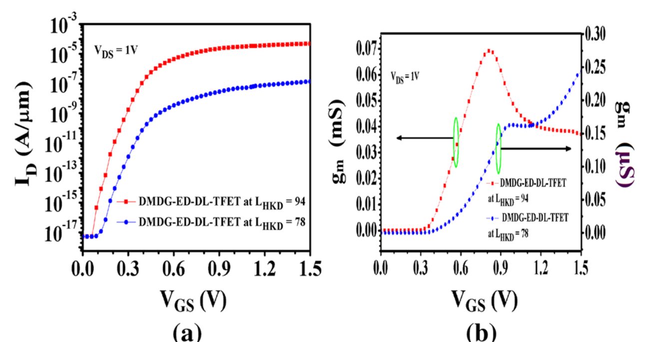

Fig. 18 **a** Variation in drain current with V_{GS} and **b** variation in transconductance with V_{GS} for different lengths of high-K dielectric material

performance degrades. Alignment of CG2 and the hetero gate dielectric causes a reduction in ON-state current and tarnsconductance as given by Fig. 18a and b, respectively. Alignment of the dual-metal gate and the hetero gate dielectric interface reduces the length of the high-K dielectric to 78 nm from 94 nm. This causes variation in the threshold voltage, subthreshold swing and the maximum value of g_m, as can be seen from the same figures. From a fabrication point of view, we have considered molybdenum (Mo) as the gate electrode because it facilitates dual work functionality of any length on the same piece of metal. So fabrication complexity can be managed by means of a misalignment of the hetero gate material and the dual metal control gate.

5 Conclusion

A thorough study of electrically doped TFET using high κ dielectric material with work function engineering shows the various advantages of DMDG-ED-DL-TFET in terms of DC and RF performance. Presence of dual work function metal in DMD-ED-DL-TFET at the drain reduces ambipolar current drastically but, at the same time, it has an adverse effect on DC characteristic and RF performance, such as transconductance, ON-state current, cut-off frequency and gain bandwidth product. On the other hand, the presence of a dual work function at the control gate (CG) and drain electrode along with high κ dielectric over half the length of the device at the gate/source side in DMDG-ED-DL-TFET shows improvement in DC and RF characteristics as compared to conventional ED-DL-TFET and DMD-DL-TFET. To simplify fabrication complexity of DMDG-ED-DL-TFET, performance analysis of the proposed device with variation in ϕ_{DE2} and L_{GS} is shown in the optimization section. This effect of scaling of V_{GS} and V_{DS} and the alignment of the dual metal gate with the hetero gate dielectric interface has been included in the same section for the proposed device.

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