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Asymmetric junctionless nanowire TFET with built-in n^+ source pocket emphasizing on energy band modification

Morteza Rahimian[1] · **Morteza Fathipour**[1]

Abstract We present a detailed study on a technique to realize a narrow and highly doped built-in n^+ source pocket in an asymmetric junctionless nanowire tunnel field-effect transistor (AJN-TFET). In the proposed structure, a built-in n^+ source pocket is created between the p^+ source and the channel without the need for any separate implantation or epitaxial growth. This leads to band diagram modification by providing a local minimum in the conduction band which results in tunneling width reduction at the source–channel interface in on-state. This leads to an abrupt transition between on- and off-state, improved subthreshold swing (SS) (38 mV/dec), and significant on-current enhancement (~ 2000 times) at low operating voltage compared with the conventional TFET. We further study the effect of the length of the built-in n^+ source pocket on the AJN-TFET characteristics. The proposed structure overcomes the difficulty in creating a narrow n^+ pocket and thus renders the AJN-TFET device more amenable for the future scaling trend needed in low-power applications.

Keywords Junctionless nanowire TFET (JN-TFET) · Built-in n^+ source pocket · Band-to-band tunneling (BTBT) · Subthreshold swing · On-state current · 2D TCAD simulation

1 Introduction

With the incessant downscaling in complementary metal–oxide–semiconductor (CMOS) integrated circuits, achieving high performance at low operating power is an important

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concern [1–3]. For low-power applications, lowering the static power ($I_{off} \times V_{DD}$) as well as the dynamic power ($C_g \times V_{DD}^2 \times f$) is crucial ($I_{off}$: off-state leakage current; V_{DD}: supply voltage; C_g: gate capacitance; f: operating frequency) [4–7]. In recent years, there has been an increasing desire to explore novel devices that can provide low leakage current at low V_{DD} while still maintaining high on-current (I_{on}) to achieve switching speeds comparable to Si CMOS technology [8,9]. These devices also need lower threshold voltage (V_T) while maintaining low I_{off}, which is strongly dependent on the subthreshold swing (SS) of the device [10,11]. This dictates the need to break the 60 mV/dec barrier in metal–oxide–semiconductor field-effect transistors (MOSFETs) [8–11].

In MOSFETs, the current-switching process involves thermionic (temperature-dependent) injection of electrons over an energy barrier as well as temperature-dependent Fermi tails (source injection) [8,12]. These are major obstacles that fundamentally limit the steepness of the transition slope from off- to on-state and thereby increase the SS value [10,11].

Thus, with the goal of replacing MOSFETs by transistors based on a new carrier injection mechanism, tunnel field-effect transistors (TFETs) are being aggressively studied [8–11]. The TFET has been considered as one of the most promising electron devices for next-generation applications, since it is immune to subthreshold swing degradation [10,11]. However, the SS < 60 mV/dec limitation has remained challenging for short channel length over a significant number of decades [13–17]. The reason why TFETs can reach below 60 mV/dec is the energy filtering of the Fermi tail [8,12]. Indeed, when highly energetic carriers in the Fermi distribution are less involved in current flow, the highly energetic tail of the Fermi distribution is eliminated, which leads to SS improvement [8,12].

It is noteworthy that certain drawbacks of TFETs impede further high-speed applications and adversely affect the functionality of circuits based on these transistors: (1) It has been demonstrated that conventional TFETs suffer from unacceptably low I_{on} and cannot provide the I_{on} levels usually achieved in MOSFETs [8,9]. In TFETs, the tunneling current depends on the height and width of the tunneling barrier. To date, numerous device structures have been proposed to further boost the on-state current of TFETs, which can be divided into two classes: engineering of (I) tunnel barrier height and (II) tunnel barrier width. The tunnel barrier height can be lowered using various techniques, e.g., replacing silicon with lower-bandgap semiconductors such as germanium (Ge) and SiGe in the channel [16,17], source [18], and a thin layer between the source and channel [19,20], or by employing various III–V compounds such as InAs and InGaAs [21,22], and also by use of a strained source [23,24]. However, employing a channel with Ge or SiGe increases I_{off} due to the narrow bandgap of these materials [16–18].

Also, alleviation of the tunneling barrier width (or equivalently, sharp band bending near the source as well as high lateral electric field) leads to a high band-to-band tunneling (BTBT) rate, which has exponential dependence on the lateral electric field [25–27]. Several approaches have been reported to reduce the tunnel barrier width, including use of a source pocket with heavy doping [4–6,25–27], dual material gate [28–31], hetero gate dielectric [32,33], and high-k gate dielectrics such as HfO_2 or TiO_2 [35–37].

Notably, introduction of a highly doped n^+ pocket between the source and channel modifies the energy band profile by providing a minimum in the conduction band [4–6,25–33]. To benefit fully from the aforementioned electrical characteristics of these structures, the size of this pocket should ideally be very narrow and the doping level high [4–6]. However, realizing such a narrow and highly doped n^+ pocket using ion implantation or epitaxial growth is a technological challenge [4–6].

(2) TFETs also suffer from ambipolar behavior; i.e., they provide conduction at both high negative and high positive gate voltage, which restricts their utility in digital circuit applications [14–18,38,39]. A well-known remedy to suppress this ambipolar conductivity is extension of the tunneling width on the drain side. (3) The presence of abrupt and highly doped junctions is essential for efficient tunneling in TFETs [40–43]. Practically, due to diffusion of dopant atoms from source/drain regions into the channel, this task is difficult to accomplish [40–43].

The dopingless TFET [44] and junctionless nanowire TFET (JN-TFET) [45–47] are two recently proposed structures which employ appropriate workfunctions to realize source and drain regions, producing behavior similar to that of the conventional TFET (C-TFET) [44–47]. They combine the advantage of TFETs of low subthreshold swing [8–11]

with the fabrication processing advantages of junctionless devices, such as formation of source and drain regions without any metallurgical junctions [48,49]. Although they are expected to be free from problems associated with random dopant fluctuations because of the low thermal budget, just as for their doped counterparts, they still exhibit low on-state current [44–47]. Hence, attention is focusing on new solutions for the above constraints.

To address these issues, we propose herein a novel JN-TFET with a narrow and highly doped built-in n^+ tunnel pocket. Converting part of the n^+ source region to a p^+ region by adding a metallic contact, here called the P-gate (PG), with workfunction of 5.93 eV (Pt, platinum) provides a built-in n^+ pocket between the p^+ source and channel. This n^+ source pocket modifies the band diagram of the proposed AJN-TFET structure by creating a minimum in the conduction band at the source–channel interface. This minimum reduces the tunneling path in on-state of the AJN-TFET compared with the conventional TFET (C-TFET). Thus, abrupt transition between on- and off-state, steep subthreshold slope, and significant on-current improvement are achieved in the AJN-TFET structure at low operating voltage.

2 Device structure and models used in the simulation

To realize the built-in n^+ source pocket, we began with a conventional JNT (C-JNT) starting structure with homogeneous n doping, i.e., $N_D = 1 \times 10^{15} \, cm^{-3}$ for channel and drain regions, and $N_D = 1 \times 10^{19} \, cm^{-3}$ for source region, as shown in Fig. 1a. Figure 1b demonstrates that holes can be induced in the n^+-doped region, converting it to a p^+ source region, by employing a metallic contact (PG) with appropriate workfunction (Pt, platinum, $WF_{PG} = 5.93 \, eV$). Such conversion of part of the n^+-doped region to a p^+ source region leaves a pocket of n^+-doped region between the source and channel in the AJN-TFET structure, as shown in Fig. 1b. This obviates the need for either epitaxial n^+ growth or n^+ ion implantation. Figure 1c shows the C-TFET structure with source doping of $N_A = 1 \times 10^{19} \, cm^{-3}$ and channel and drain doping of $N_D = 1 \times 10^{15} \, cm^{-3}$.

The following parameter values were employed in this numerical study for the AJN-TFET structure: silicon film thickness (t_{Si}) = 10 nm, gate dielectric (SiO_2) thickness (t_{ox} = 1 nm), main gate (MG) length (L_{MG} = 30 nm), built-in n^+ source pocket length = 5 nm and main gate workfunction of 4.6 eV.

The electron and hole concentrations of the AJN-TFET structure along the vertical direction (along the BB' cut line located 15 nm from the left side of the structure) are shown in Fig. 2. As can be seen from this figure, the hole concentration in the source region is noticeably large at the Si–SiO_2
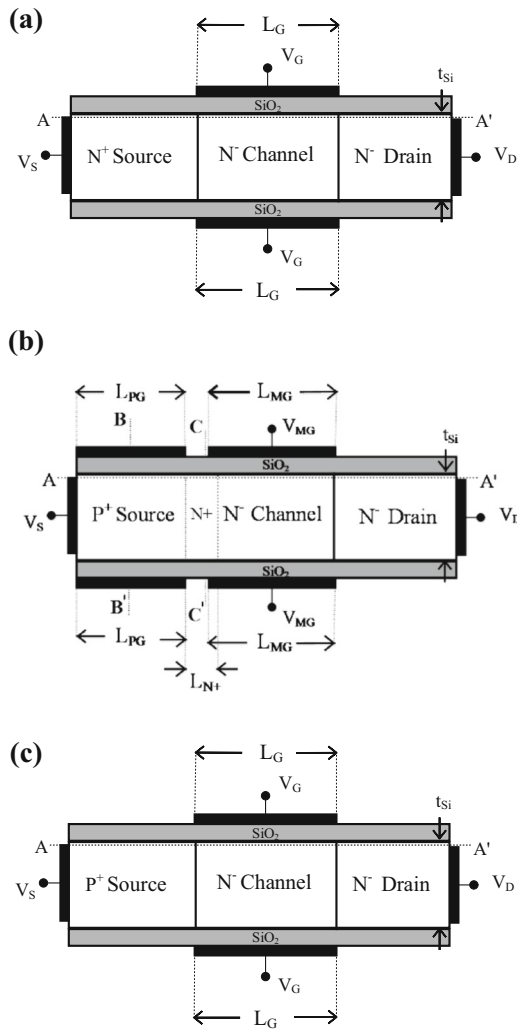
Fig. 1 Cross-sectional view of the **a** C-JNT, **b** AJN-TFET, and **c** C-TFET structures. Main gate and P-gate have workfunction of 4.6 and 5.93 eV, respectively. Silicon film thickness ($t_{Si} = 10$ nm), gate dielectric thickness ($t_{ox} = 1$ nm), main gate (MG) length ($L_{MG} = 30$ nm), length of built-in n^+ source pocket = 5 nm

Fig. 2 Electron and hole concentration of AJN-TFET structure at $V_{GS} = 1$ V and $V_{DS} = 1$ V along vertical direction (along BB' cut line) for silicon film thickness (t_{Si}) = 10 nm, and length of built-in n^+ source pocket = 5 nm. The hole concentration in the source region is noticeably large at the Si–SiO$_2$ interface, where tunneling takes place

interface, where tunneling takes place. This demonstrates the impact of the holes induced by employing the additional P-gate electrode. Moreover, in [34], the hole concentration at the center of the silicon body is plotted for different silicon body thicknesses, demonstrating that the complete source region can be converted to a p^+ region when the silicon body thickness is reduced below 10 nm. Since we do not consider any quantum effects in our study, we limit the choice of the silicon film thickness to 10 nm [31,44,50,51]. For silicon film thicknesses below 10 nm, one would need to consider quantum effects due to the considerable quantization, which causes an increase in the on-state barrier and thereby on-current reduction [50,51].

All of the above parameter values were also used for the C-TFET structure, except the built-in n^+ source pocket. Just as
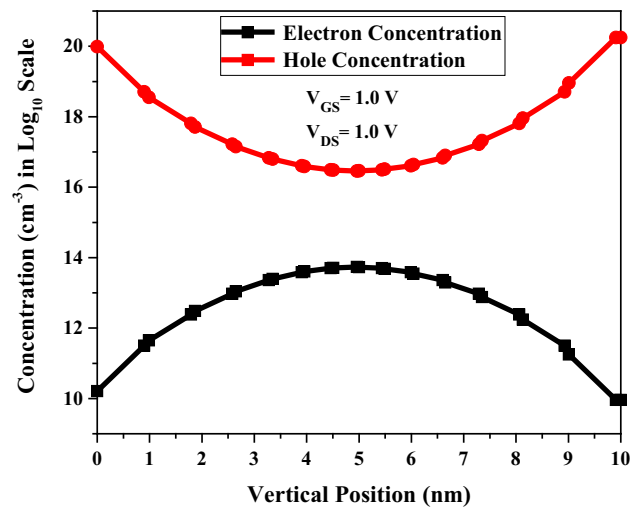
for the C-TFET, to turn on the device, gate voltage is applied only to the main gate while in off- and on-state, while the P-gate terminal is kept at zero voltage.

Device characteristics were obtained by two-dimensional (2D) numerical simulations realized using Atlas from Silvaco [52]. We used a nonlocal band-to-band tunneling (BTBT) model to take into account the spatial variation of the energy bands [28–33,44–47]. In contrast to local tunneling models, the nonlocal BTBT model describes a physical picture of carrier transport through the barrier, and considers the energy band profile along the entire tunneling path. It is well known that the TFET current depends on the BTBT probability. The most widely used model for calculating the tunneling current is Kane's model [16–19]. This model determines the effective BTBT generation rate of carrier tunneling from the valence band of the source region to the conduction band of the channel, which can be evaluated as follows [16–19]:

$$G_{BTBT} = A \frac{E^D}{E_g^{1/2}} \exp\left(-B \frac{E_g^{3/2}}{E}\right), \qquad (1)$$

where E is the magnitude of the electric field, E_g is the energy bandgap, and D is a user-adjustable parameter, being 2.5 for indirect and 2 for direct tunneling processes. The parameters A and B are tunneling process-dependent coefficients which are equal to 3.5×10^{21} eV$^{1/2}$/cm-s-V^2 and 22.5×10^6 V/cm-eV$^{3/2}$, respectively [53,54]. Parameter values reported here were calibrated against experimental Zener diode characteristics reported by Fair and Wivell [53,54].

To take into account recombination effects, we employed the Shockley–Read–Hall (SRH) model. Also, due to the pres-
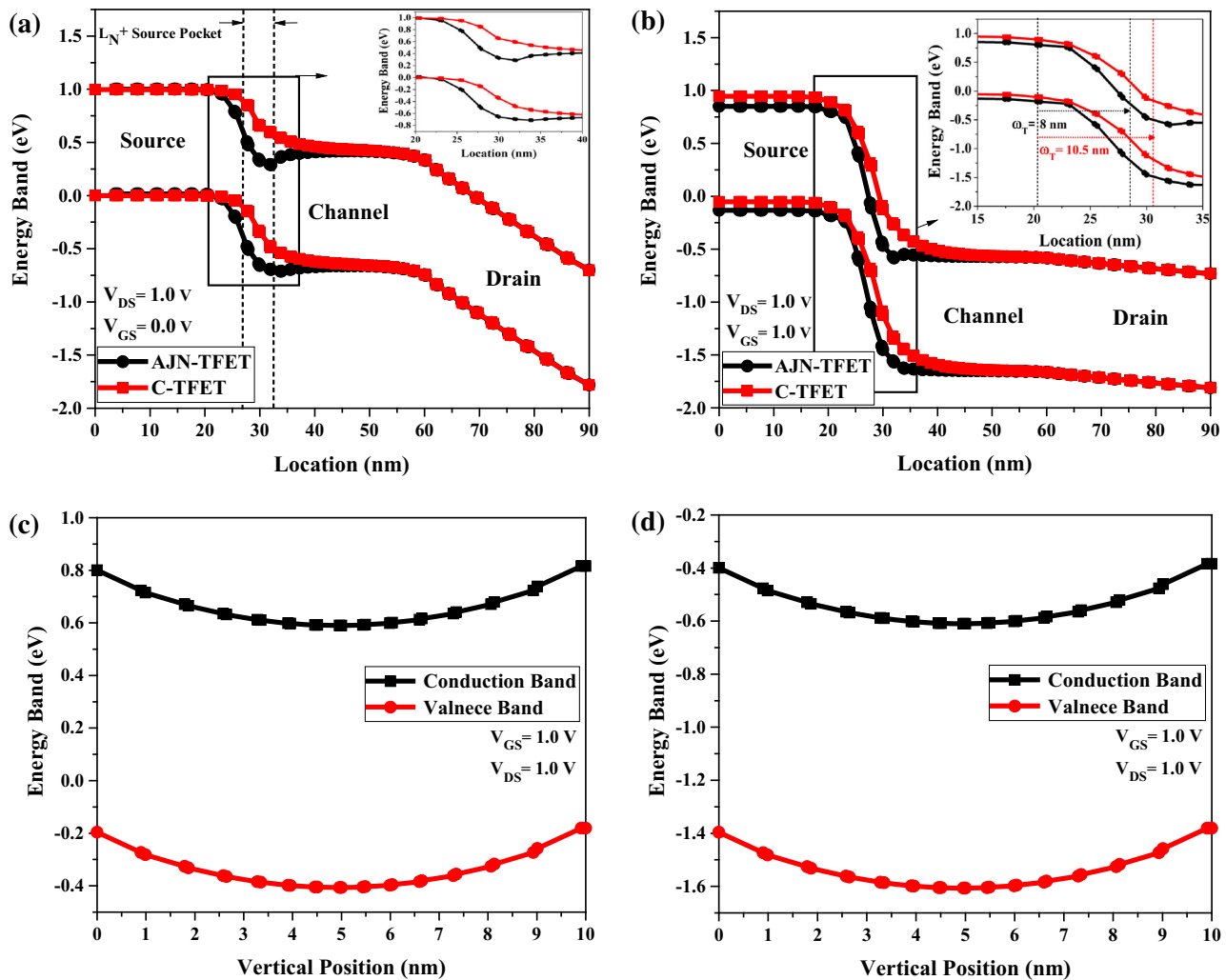
Fig. 3 Band diagram shown in lateral direction for the AJN-TFET and C-TFET structures: **a** in off-state ($V_{GS} = 0.0$ V and $V_{DS} = 1$ V), where the narrow and highly doped n^+ source pocket modifies the band diagram with a minimum in the conduction band, and **b** in on-state ($V_{GS} = 1$ V and $V_{DS} = 1$ V). The tunneling path is reduced from $w_{C-TFET} = 10.5$ nm in the C-TFET structure to $w_{AJN-TFET} = 8$ nm in the AJN-TFET. Band diagrams of the AJN-TFET structure at $V_{GS} = 1$ V and $V_{DS} = 1$ V in vertical direction along the **c** BB' and **d** CC' cut line

ence of interface traps at the silicon–oxide interface and high carrier concentration, we employed a direct recombination (Auger) model [55]. A bandgap narrowing (BGN) model was used due to the high doping density in different regions of the device. The mobility models used in the simulation take into account both field-dependent and concentration-dependent mobility.

3 Physical operation of the AJN-TFET

In this section, we study the underlying physics of the AJN-TFET structure. First, we compare this device with the C-TFET structure and discuss the on-state current as well as subthreshold swing. We then optimize the length of the built-

in n^+ source pocket as well as the workfunction of the P-gate to obtain desirable characteristics.

3.1 Comparison with C-TFET structure

In TFETs, the current is proportional to the electron/hole transmission probability $T(E)$, given by [16–19]

$$
\begin{aligned}
T(E) &\approx \exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{\frac{3}{2}}}{3\,|e|\,h\left(\Delta\phi + E_g\right)}\right) \\
&= \exp\left(-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3\,|e|\,h(\Delta\phi + E_g)}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}t_{Si}}\right),
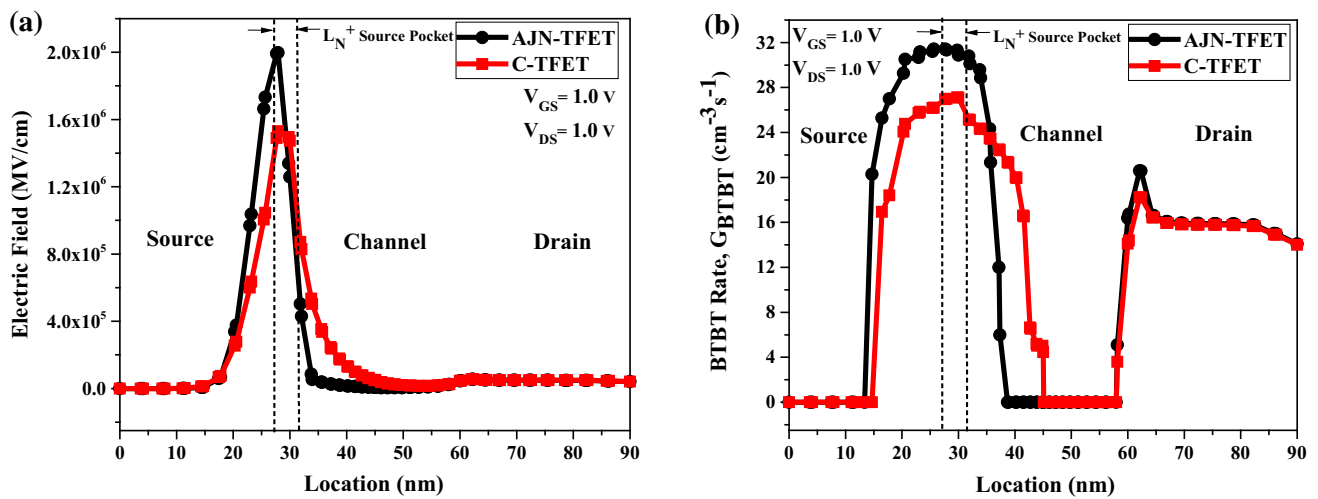\end{aligned} \quad (2)
$$

Fig. 4 **a** Electric field and **b** nonlocal BTBT rate for the AJN-TFET and C-TFET structures versus lateral position in on-state ($V_{GS} = 1$ V and $V_{DS} = 1$ V) along the AA' cut line. The AJN-TFET structure has a stronger peak at the source–channel junction near the n^+ source pocket. The high electric field within the built-in n^+ region of the AJN-TFET structure leads to an enhanced BTBT rate

where m^* is the carrier effective mass, e is the electron charge, E_g is the bandgap, $\Delta\phi$ is the energy range over which tunneling can occur (controlled by V_{GS}), Λ is the spatial extent of the transition at the source–channel interface, ε_{ox} and ε_{Si} are the dielectric constants of oxide and silicon, respectively, and t_{ox} and t_{Si} are the gate oxide and silicon layer thickness, respectively. According to Eq. (2), one approach for tunneling current enhancement is reduction of the bandgap in the channel region [16–24], while another is increasing the electric field along the channel (proportional to $(\Delta\phi + E_g)/\Lambda$) [25–37].

The operation of the built-in n^+ source pocket in the AJN-TFET device can be understood from the band diagrams shown in Fig. 3a for off-state ($V_{GS} = 0$ V, $V_{DS} = 1$ V) and Fig. 3b for on-state ($V_{GS} = 1$ V, $V_{DS} = 1$ V) along the AA' cut line located 0.1 nm below the Si–SiO$_2$ interface. The more efficient injection of carriers through the narrow built-in n^+-doped region improves the electrical characteristics compared with the C-TFET structure. This is mainly due to the following three reasons: (1) The presence of a local dip in the energy band profile at the conduction band of the source–channel junction in off-state, as shown in Fig. 3a, decreases the tunneling barrier width in on-state. The band diagram modification is further clarified by the inset in Fig. 3a. (2) The increase in V_{GS} aligns the local minimum of E_C with the valence-band edge E_V of the source and gradually places the E_C of the channel below the E_V of the source region. Thus, electrons can tunnel into the E_C minimum and the tunneling path is sharply reduced. The reduction of the tunneling width is clearly shown in the inset of Fig. 3b. It can be observed that the spatial extent of the transition Λ at the source–channel interface is smaller for the AJN-TFET structure [refer to Eq.

(2)]. (3) The increase in the lateral electric field enhances the tunneling efficiency and helps in obtaining high on-state current.

Figure 3c and d show vertical band diagrams of the AJN-TFET structure along the cut lines BB' and CC', respectively. The CC' cut line is located 30 nm from the left side of the structure, at the point of maximum BTBT. As can be seen from this figure, there is no band overlap in the vertical direction. This suggest that BTBT is dominant in the lateral direction.

It is well known that BTBT exhibits exponential dependence on the lateral electric field. A low BTBT rate has been held responsible for the low on-state current of the C-TFET [27,31]. To discuss the performance improvement for the AJN-TFET structure, the on-state electric field along the AA' cut line is shown in Fig. 4a for both structures. As can be seen from this figure, both structures provide a peak near the source–channel tunneling junction. However, due to the steep gradient of the band diagrams in on-state for the AJN-TFET, a stronger peak at the source–channel junction is achieved.

Note that the high electric field together with the reduced tunneling width leads to a high BTBT rate. The improvement of the on-state current for the AJN-TFET structure can be explained based on the BTBT rate shown in Fig. 4b at $V_{GS} = 1.0$ V and $V_{DS} = 1.0$ V. As can be seen from this figure, a larger BTBT rate is obtained for the AJN-TFET structure near the built-in n^+ region, which leads to an enhanced on-state current and improved subthreshold swing.

The improved performance of the AJN-TFET structure compared with the C-TFET can also be understood from the on-state electric field contours shown in Figs. 5 and 6. We
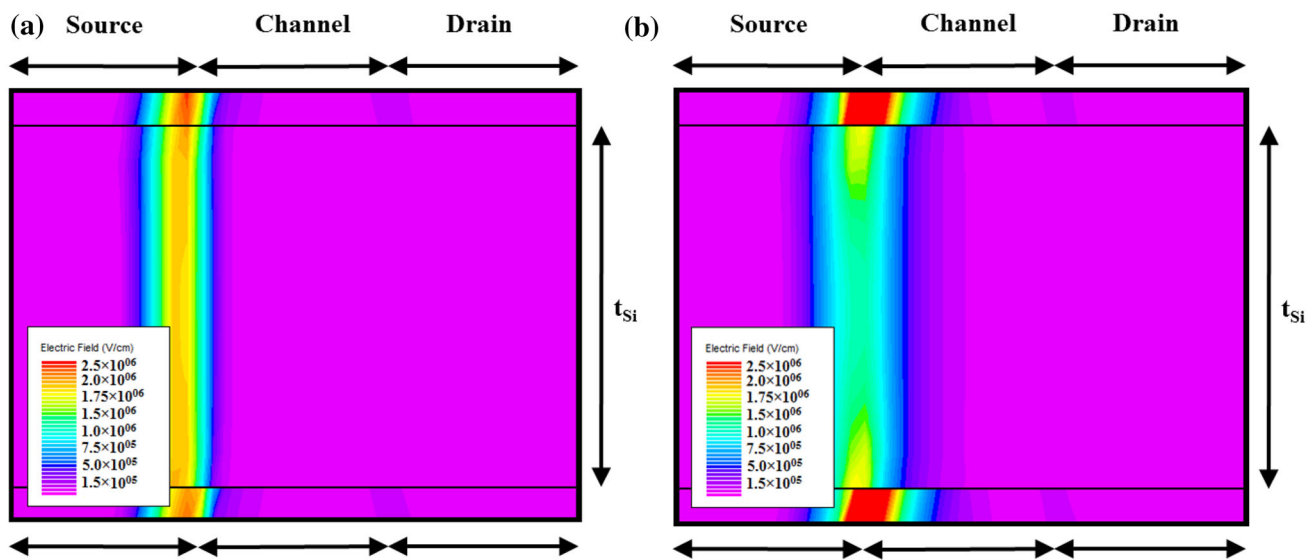
Fig. 5 On-state ($V_{GS} = 1$ V and $V_{DS} = 1$ V) electric field contours in the **a** AJN-TFET and **b** C-TFET structures. In the AJN-TFET structure, a larger electric field occurs near the built-in n^+ source pocket
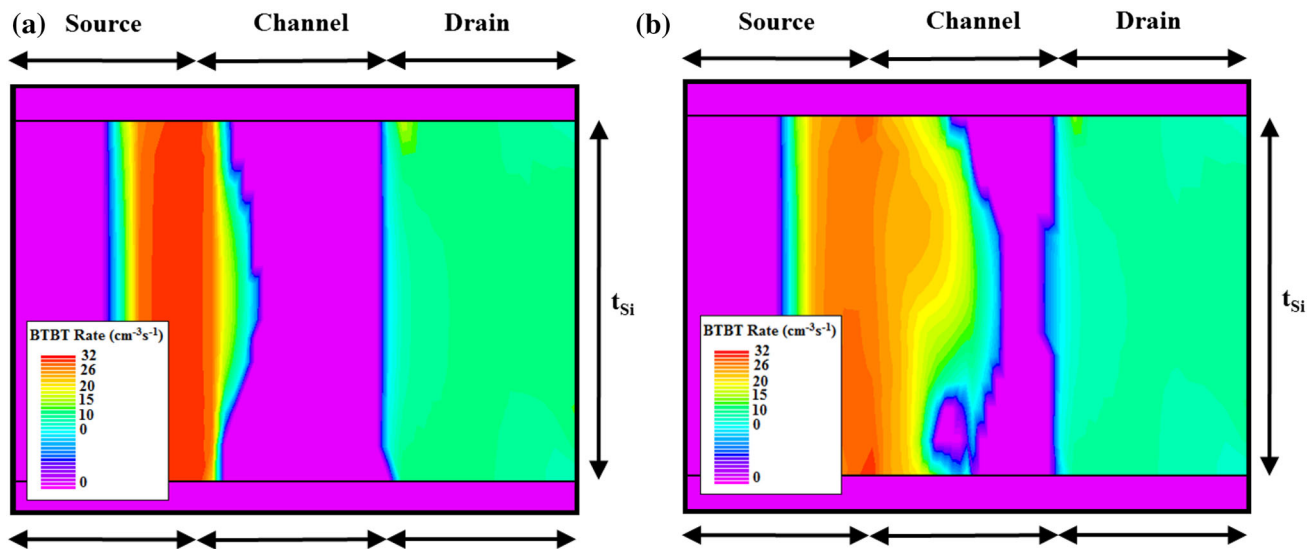

Fig. 6 On-state ($V_{GS} = 1$ V and $V_{DS} = 1$ V) nonlocal band-to-band tunneling rate in the **a** AJN-TFET and **b** C-TFET structures. High electric field, together with a reduced tunneling width near the built-in n^+ source pocket, leads to a higher band-to-band tunneling rate and enhanced drain current

observe that the electric field and BTBT rate of the AJN-TFET structure at the source–channel junction are higher compared with the C-TFET owing to the presence of the n^+ source pocket (as shown in Fig. 3b).

Figure 7 compares the transfer characteristic ($I_{DS} - V_{GS}$) of the AJN-TFET with that of the C-TFET structure. As can be seen from this figure, the AJN-TFET structure not only exhibits about 2000 times enhancement in the on-state current, but also its SS value is significantly smaller (38 mV/dec for $L_{n^+} = 5$ nm) than that achieved in the C-TFET structure (56 mV/dec). Since, in general, TFETs suffer from low I_{on}, it is desirable to adjust the built-in n^+ source pocket parameters

to obtain a maximum I_{on}. Fig. 7b shows the SS value versus the drain current. As usual, the C-TFET structure exhibits SS < 60 mV/dec over a limited range of I_D, whereas the AJN-TFET has SS < 60 mV/dec over wide decades of drain current.

The entire simulation presented above was conducted for main gate workfunction of 4.6 eV. Any change in this value shifts the $I_{DS} - V_{GS}$ characteristic by the same magnitude as the change [47]; For example, if the workfunction of the main gate is adjusted to 4.4 eV (4.8 eV), i.e., a change of 0.2 eV, the conduction- and valance-band levels in the channel region are moved down (up) by 0.2 eV, corresponding to a main gate at
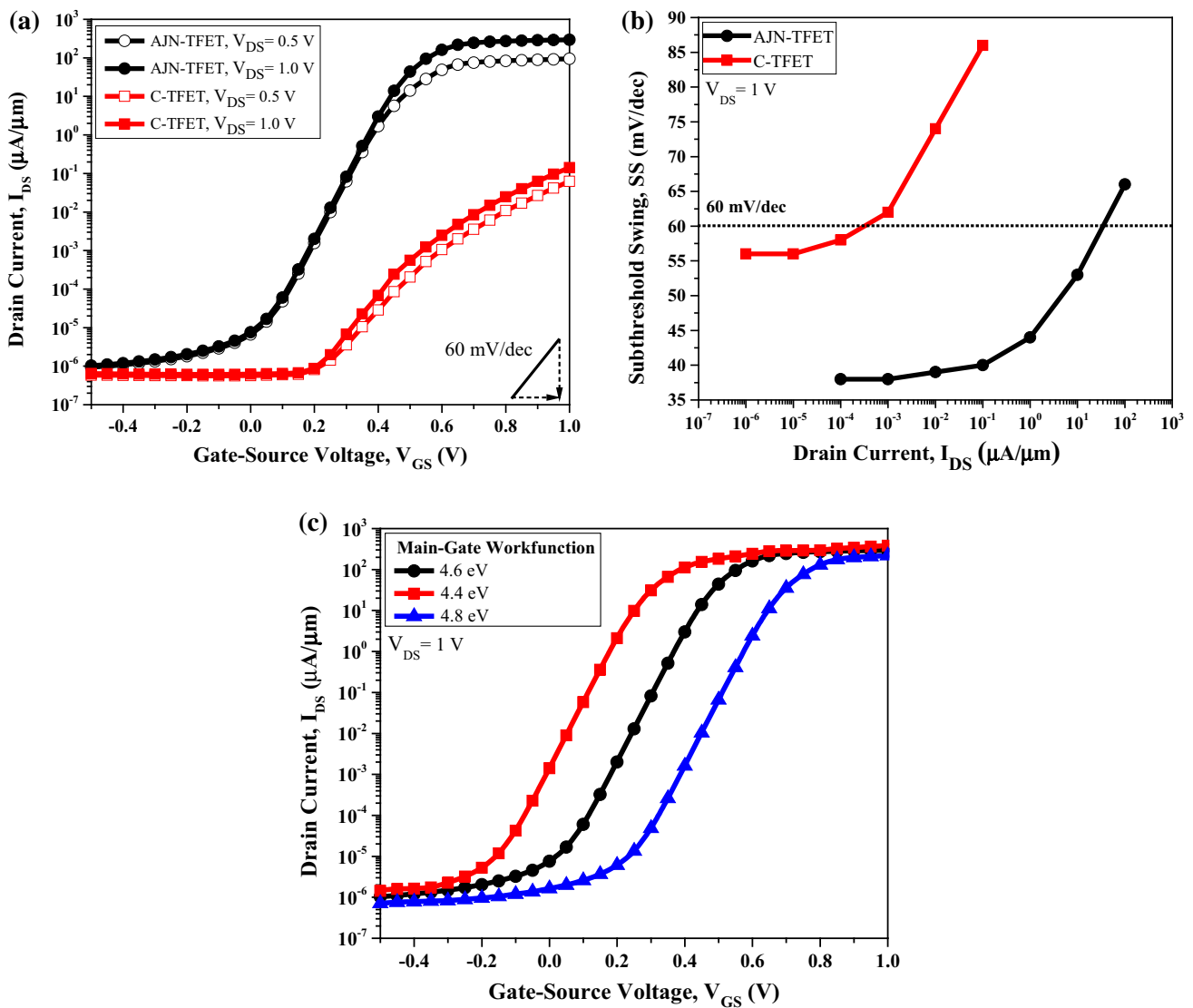
Fig. 7 a $I_{DS} - V_{GS}$ characteristics at $V_{DS} = 0.5$ and 1.0 V and **b** SS–I_{DS} for the AJN-TFET and C-TFET structures, with $t_{Si} = 10$ nm, $L_{ch} = 30$ nm , and $t_{ox} = 1$ nm. The I_{on} and SS values of the AJN-TFET are 2.95×10^2 A/μm and 38 mV/dec, whereas for the C-TFET structure they are 1.42×10^{-1} A/μm and 56 mV/dec at $V_{DS} = 1.0$ V. The line with SS= 60 mV/dec is drawn for reference. (c) $I_{DS} - V_{GS}$ characteristics of the AJN-TFET structure with main gate workfunction of 4.4, 4.6, and 4.8 eV at $V_{DS} = 1.0$ V. P-gate workfunction is kept constant at 5.93 eV

4.6 eV with 0.2 V (−0.2 V) of additional bias. Hence, there is a shift in the $I_{DS} - V_{GS}$ characteristic by 0.2 V to the left (right), as shown in Fig. 7c.

3.2 Optimization of the built-in n^+ source pocket and P-gate workfunction

The length (L_{n^+}) of the n^+ source pocket plays an important role in the improvement of the electrical characteristics for the AJN-TFET structure. The optimization process is related to the depth and width of the conduction band well, where a local minimum of E_c is located.

For the AJN-TFET structure, the I_{off} and SS values are shown in Fig. 8a as functions of the length of the built-in n^+ source pocket. The AJN-TFET structure exhibits both low off-state current and low SS for a range of values of $L_{n^+} \sim 3 - 6$ nm, indicating that there exist optimum values for L_{n^+} which minimize both SS and I_{off}. Thus, the gate-controlled BTBT near the source region is dominant in determining the subthreshold conduction mechanism for optimum values of L_{n^+}. Figure 8b shows the change in the transfer characteristic ($I_{DS} - V_{GS}$) of the AJN-TFET struc-
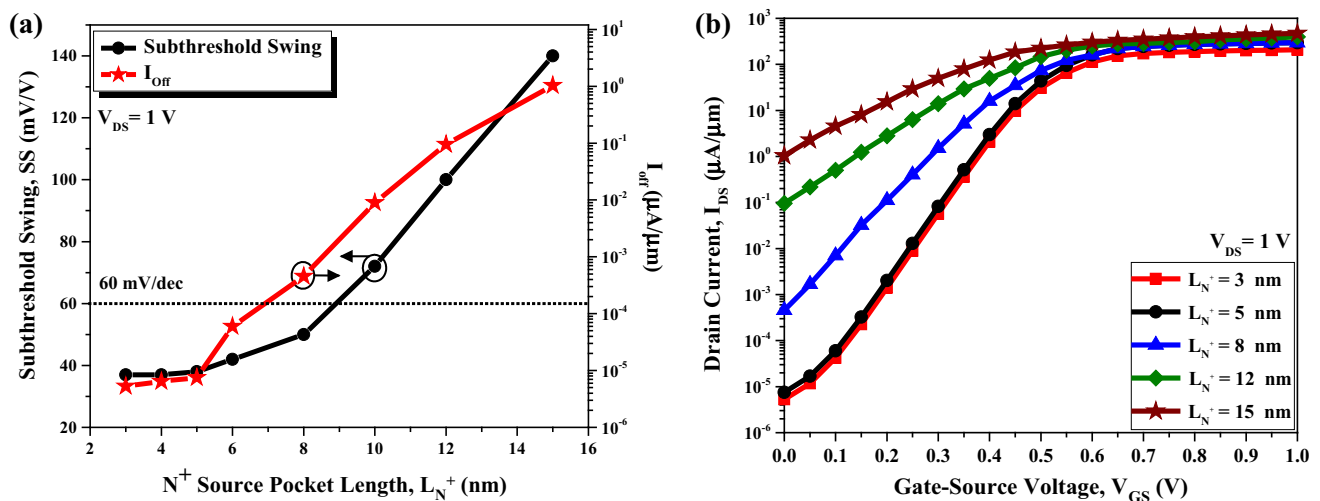
Fig. 8 **a** I_{off} and SS, and **b** transfer characteristic ($I_{DS} - V_{GS}$) of AJN-TFET structure for different values of L_{n+}. I_{off} is calculated at $V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V
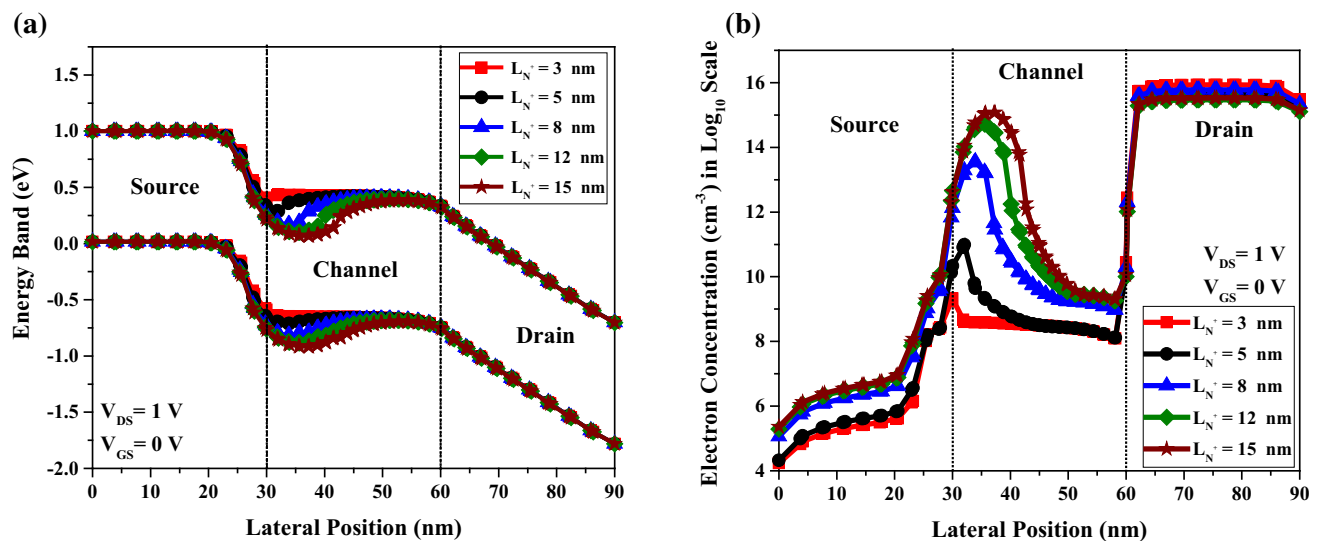

Fig. 9 **a** Off-state energy band diagram and **b** electron concentration in the AJN-TFET structure versus lateral position for different values of L_{n+}. As L_{n+} increases, the local E_C minimum widens and dips more, also acting as a virtual source of electrons in the channel

ture as the length of the built-in n^+ source pocket is increased from 3 to 15 nm. Since the impact of L_{n+} is only to modulate the energy band profiles in the subthreshold region, the on-state current is independent of L_{n+} whereas the I_{off} and SS values are degraded for larger L_{n+}. It is worth noting that, in the larger pocket, the confinement effect and scattering through confined states becomes more noticeable. Thus, the optimum length is acceptable within the current scope of Kane's model when not considering these effects.

As L_{n+} is increased, the local E_C minimum widens and dips more, as shown in Fig. 9a. This phenomenon provides electrons at E_V of the source region to tunnel into the minimum of E_C, which acts as a virtual source for electrons as shown in Fig. 9b. Further increase in L_{n+} saturates the tun-

neling width modification, so that transistor action occurs by lowering the barrier under the main gate. The carrier injection mechanism is now similar to that of a conventional MOSFET, i.e., injection over a barrier. Therefore, this results in degradation of the SS and increase of I_{off} for the device, as shown in Fig. 8.

Notably, the influence of changes in the main gate workfunction is similar to that for conventional TFETs and MOSFETs [28,30,44]. However, the impact of changes in the P-gate workfunction appears to be different. The purpose of having a P-gate in this device is to: (I) fully deplete the source region and (II) move the conduction- and valance-band edges towards higher energy levels [47]. This leads to sufficient band overlap between the source and channel
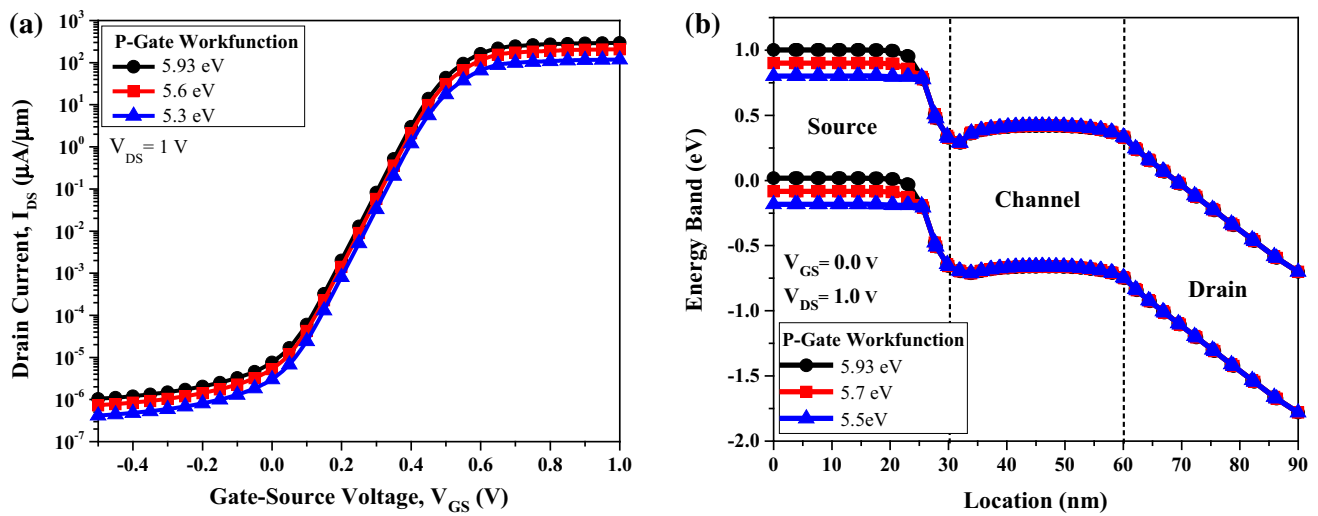
Fig. 10 **a** $I_{DS} - V_{GS}$ characteristics of AJN-TFET structure at $V_{DS} = 1.0$ V. Reduced off- and on-state currents are achieved with lower P-gate workfunction. **b** Lateral band diagram of AJN-TFET structure in off-state ($V_{GS} = 0$ V and $V_{DS} = 1$ V) for three different P-gate workfunctions of 5.5, 5.7, and 5.93 eV

regions for tunneling to occur. So, for achieving higher I_{on}, it is always advisable to have a high workfunction for the P-gate [47]. Lowering the workfunction of the P-gate reduces both the I_{on} and I_{off} of the device, as demonstrated in Fig. 10, which shows the lateral band diagram in off-state and the corresponding $I_{DS} - V_{GS}$ characteristic for three different workfunctions of the P-gate. The reduced off- and on-states are due to the reduction in the band overlap between the source and channel regions.

4 Comparison with TFETs in literature

Table 1 summarizes the characteristics of some recently reported TFETs with a dip in the conduction band and compares them with the JN-TFET device proposed herein. All the reported TFET devices demonstrate very low off-state current, making them strong candidates for low-power and energy-efficient applications. Moreover, the AJN-TFET structure proposed herein also offers excellent characteristics such as high I_{on} and I_{on}/I_{off}, and low SS values at low operating voltage, comparable to those of previously reported devices.

We now discuss the advantages of the proposed AJN-TFET structure compared with the previously reported structures. Recently, several structures which employ an n^+ pocket at the source–channel interface formed using ion implantation or epitaxial growth have been suggested [4–6,25,26,39]. However, these structures suffer from certain drawbacks: (1) Their starting structure is $p^+p^-n^+$ or $p^+n^-n^+$, becoming $p^+n^+p^-n^+$ or $p^+n^+n^-n^+$, respectively. Unfortunately, dopant diffusion from source/drain regions into the channel is a detrimental problem. (2) Real-

izing a narrow and highly doped n^+ pocket at the source–channel interface using ion implantation or epitaxial growth is a fabrication challenge. Hence, attention is focused on novel solutions for creating a minimum in the conduction band. Various techniques have been proposed, including use of a dual-material gate [15,28–31], hetero gate dielectric [31–33], and inner source pocket [34] on $p^+p^-n^+$, $p^+n^-n^+$, and $n^+p^-n^+$ starting structures. However, these structures still suffer from the problem associated with dopant diffusion. To address these issues, the AJN-TFET structure provides a new design which combines the advantages of the JN-FET structure with an n^+ source pocket to improve the electrical performance. The JN-FET device is immune to dopant diffusion, since it has a homogeneously doped structure. Also, compensating part of the n^+-doped region to yield a p^+ source leaves a pocket of n^+-doped region between the source and channel. This technique allows for realization of a narrow and highly doped n^+ source pocket without any need for additional ion implantation or any epitaxial growth. The proposed AJN-TFET structure presents an innovative and low-cost approach for achieving applicable TFET device characteristics.

5 Conclusions

We propose an innovative technique to realize a built-in n^+ source pocket on a junctionless nanowire FET (JN-FET) starting structure. This approach eliminates the need for either separate ion implantation or epitaxial growth to create the n^+ region. The modified band diagram of the proposed asymmetric junctionless nanowire TFET (AJN-TFET) shows a local dip in the conduction band of the

Table 1 Comparison of various TFET devices with a minimum in the conduction band reported in literature and herein

Reference	Experimental/ simulation	Channel length (nm)	Type	V_{DS} (V)	V_{GS} (V)	SS[a] (mV/dec)	I_{on}^{b} (A/μm)	I_{off}^{c} (A/μm)	Dielectric material	t_{ox} (nm)	Channel material
[4]	Experimental	100	p	−1.1	−1.0	46	1.4×10^{-6}	1.1×10^{-13}	Al_2O_3	3.5	Si
[5]	Simulation	100	n	1.0	1.0	25	3.2×10^{-5}	2.0×10^{-15}	SiO_2	3	Si
[5]	Experimental	1000	n	1.1	3.0	225	3.0×10^{-8}	1.0×10^{-10}	SiO_2	4	Si (bulk)
[5]	Experimental	1000	n	1.1	3.0	220	1.0×10^{-8}	6.1×10^{-13}	SiO_2	4	Si (SOI)
[6]	Experimental	90	n	1.0	4.0	200	9.0×10^{-7}	3.0×10^{-12}	SiO_2	6.6	Si
[39]	Simulation	50	n	1.0	1.0	–	5.2×10^{-5}	7.0×10^{-17}	SiO_2	1	Si
[31]	Simulation	50	n	1.0	0.8	20	3.2×10^{-4}	8.7×10^{-18}	HfO_2 and SiO_2	2	Si
[25]	Simulation	100	n	1.0	1.0	38	8.2×10^{-4}	4.0×10^{-11}	SiO_2	2.5	Si
[25]	Experimental	1000	n	1.0	0.6	65	2.0×10^{-5}	2.0×10^{-6}	SiO_2	3	Si
[26]	Simulation	60	n	1.0	1.0	44	3.5×10^{-5}	1.0×10^{-15}	SiO_2	2	Si
[29]	Simulation	50	n	1.0	1.5	12	2.0×10^{-5}	1.0×10^{-17}	HfO_2	3	Si
[32]	Simulation	50	n	1.0	1.0	12	9.5×10^{-5}	2.1×10^{-16}	HfO_2 and SiO_2	2	Si
[33]	Simulation	35	n	0.7	1.5	60	5.0×10^{-5}	1.0×10^{-12}	HfO_2 and SiO_2	2	Si
[30]	Simulation	30	n	1.0	1.0	17	2.0×10^{-5}	3.0×10^{-13}	HfO_2	2	Si
This work	Simulation	30	n	1.0	1.0	38	2.9×10^{-4}	7.5×10^{-12}	SiO_2	1	Si

[a] Steepest SS, the best observed subthreshold swing in the $I_{DS} - V_{GS}$ characteristic

[b] I_{on} measured at the given V_{DS} and V_{GS}

[c] I_{off} is the lowest current observed at given V_{DS}

channel, which results in an abrupt transition between on- and off-state. We have shown that, within the scope of Kane's model, the AJN-TFET structure can achieve up to about three orders of magnitude enhanced on-state current and an improved subthreshold swing (∼38 mV/dec) at low supply voltage as compared with the C-TFET structure. Notably, some important conclusions stem from this study regarding the AJN-TFET, as follows: (1) The length of the built-in n^{+} source pocket has an optimum value of 5 nm to achieve applicable electrical characteristics. (2) The additional electrode, called the P-gate, in the AJN-TFET structure must have as high a workfunction as possible, since it has a strong effect on the on- and off-state current. (3) The main gate workfunction can be used to tune the on- and off-state current, as any change in this value simply shifts the $I_{DS} - V_{DS}$ characteristic. Thus, the proposed device is an attractive alternative for use in future low-power circuit applications.

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