

High-performance multiplexer architecture for quantum-dot cellular automata

Hamid Rashidi¹ · Abdalhossein Rezaei² · Sheema Soltany¹

Published online: 25 May 2016
© Springer Science+Business Media New York 2016

Abstract The quantum-dot cellular automata (QCA) technology is a promising alternative technology to CMOS technology to extend the exponential Moore's law progress of microelectronics at nanoscale level, which is expected to be beneficial for digital circuits. This paper presents and evaluates three multiplexer architectures: a new and efficient 2:1 multiplexer architecture, a 4:1 multiplexer architecture, and 8:1 multiplexer architecture in the QCA technology. The 4:1 and 8:1 QCA multiplexer architectures are proposed based on the 2:1 QCA multiplexer. The proposed architectures are implemented with the coplanar crossover approach. These architectures are simulated using the QCADesigner tool version 2.0.1. The 2:1, 4:1, and 8:1 QCA multiplexer architectures utilize 15, 107, and 293 cells, respectively. The simulation results demonstrate that the proposed QCA multiplexer architectures have the best performance in terms of clock delay, circuit complexity, and area in comparison with other QCA multiplexer architectures.

Keywords Nanotechnology · Multiplexer · Wire crossing · Clock zone · Quantum cellular automata · QCADesigner

1 Introduction

Due to the dramatic increase rate in the number of transistors within the chip, reducing the size of transistors is essential,

but in the CMOS technology, size reduction of transistors, at nano-scale, is not possible simply and the extension of Moore's law in CMOS technology beyond 10-nm is not feasible as it introduces an anomalous quantum behavior in nanoscale [1–4]. The quantum-dot cellular automata (QCA) technology is able to achieve higher speed and density and lower power consumption designs compared to conventional CMOS technology [2,4–6]. The binary information in this technology is encoded by reconfiguration of the charges instead of current [6]. So in recent years, circuit implementation in QCA technology has received a great deal of attention due to a number of promising applications such as efficient QCA full adder design [6–9], efficient QCA multiplier design [10,11], and efficient QCA multiplexer design [4,12–16].

On the other hand, the multiplexers have wide applications in digital circuit implementations such as RAM cells, ALU, and row decoders [4,12,17]. A lot of efforts have been made at the logic and layout levels to improve the performance of the multiplexers in the QCA technology [4,12–16,18–21,24–29]. This paper presents and evaluates new and efficient QCA multiplexer architectures. The main distinctive characteristics of our contribution are as follows:

- It presents a new and efficient 2:1 QCA multiplexer architecture as a basic logic module.
- It presents a new and efficient 4:1 and 8:1 QCA multiplexer architectures based on the proposed basic logic module.
- It simulates the proposed QCA multiplexer architectures on the QCADesigner version 2.0.1.

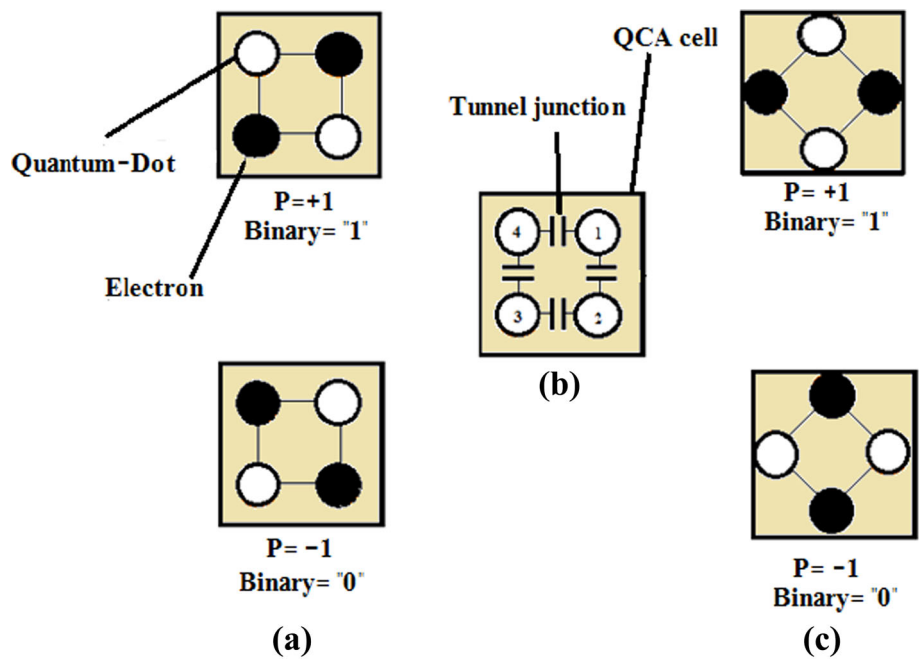
The overall QCA cell dimensions are defined to be 18 nm × 18 nm. In this paper, we have used the metallic and semiconductor QCA, and the simulation results presented here have been at 1 K temperature. The proposed multiplexer is

✉ Abdalhossein Rezaei
rezaie@acecr.ac.ir

¹ ACECR Institute of Higher Education, Isfahan Branch, Isfahan 84175-443, Iran

² Academic Center for Education, Culture and Research (ACECR), Isfahan University of Technology (IUT) Branch, Isfahan 8415681167, Iran

Fig. 1 Two kinds of QCA cells (90° and 45°) with their polarizations (P = -1 and P = +1) [4]



compared to previous designs [4, 12–16, 18–21, 24–29] versus some characteristics such as area, cell count, and delay. Our implementation results demonstrate that the proposed QCA multiplexer architectures have the best performance in comparison with the other QCA multiplexer architectures.

The rest of this paper is organized as follows: Section 2 briefly describes preliminaries of the QCA technology and multiplexer implementation in this technology. Section 3 presents the proposed 2:1, 4:1, and 8:1 QCA multiplexer architectures. Section 4 provides simulation results. Section 5 evaluates the proposed architectures. Finally the conclusion is given in Sect. 6.

2 Preliminaries

This section briefly describes preliminaries of the QCA technology and multiplexer architectures in this technology.

2.1 QCA cells

QCA cells are the basic units in the QCA technology, which consist of four quantum-dots located in the corners of a square [2]. There are two kinds of QCA cells, 90° and 45°, with their polarizations, P = -1 and P = +1. Figure 1 shows these kinds of QCA cells [4, 5].

As it is shown in Fig. 1, an interconnection between the intercell electrons forms two stable arrangements, $p = 1$ and $p = -1$, which are used to denote logic stats “1” and “0,” respectively [4, 5]. If cells are placed near each other, the polarization of one cell will influence the polarization of

another. When the electrons are placed in the position 1 and 3, cell polarization (P) is +1. Similarly, when the electrons are placed in the position 2 and 4, cell polarization (P) is -1. P is the polarization of cell that is calculated from equation 1:

$$P = \frac{(P_2 + P_4) - (P_1 + P_3)}{P_1 + P_2 + P_3 + P_4}, \tag{1}$$

where P_i shows the electronic charge at i th dot.

2.2 QCA wire

In the QCA technology, there are two types of wires, which are utilized for transferring input cell polarizations: (a) multilayer crossing wire, and (b) coplanar crossing wire.

As it is shown in Fig. 2, the coplanar crossing wires are implemented in a single layer and the vertical wire has all the cells rotated by 45°, whereas crossing multilayer wires are implemented at least in three layers [22].

2.3 QCA gates

Figure 3 shows the basic gates in the QCA technology. The fundamental QCA gates in this technology are classified in three groups as follows [6]:

- (a) Original majority gates (OMGs)
- (b) Rotate majority gates (RMGs)
- (c) Inverter gates (IGs)

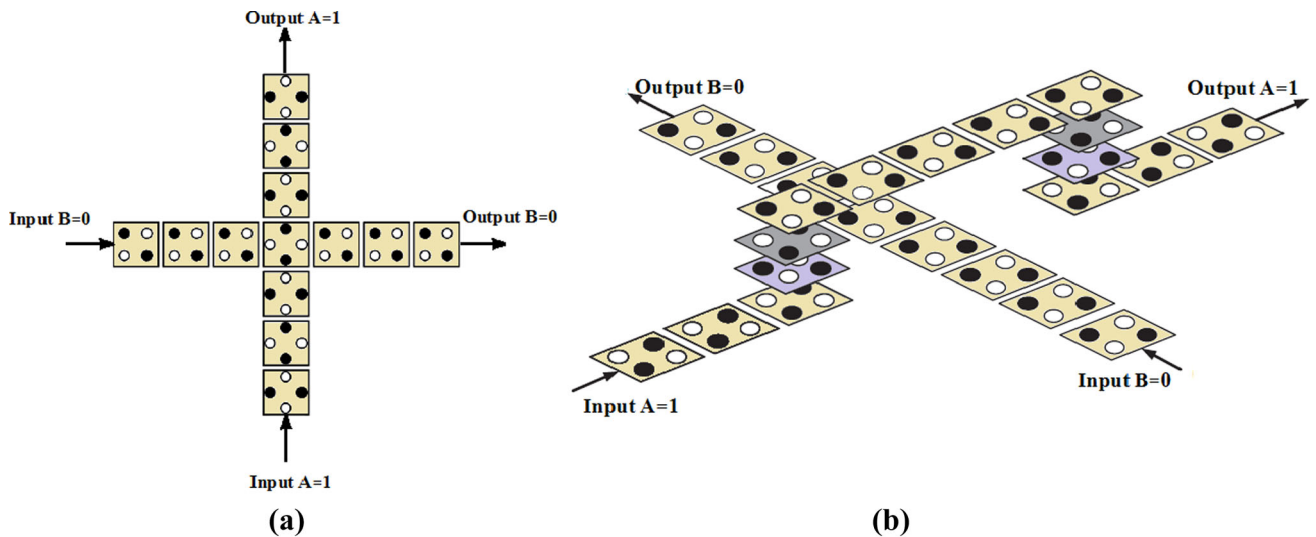


Fig. 2 The QCA wires, a coplanar crossing wire, b multilayer crossing wire [22]

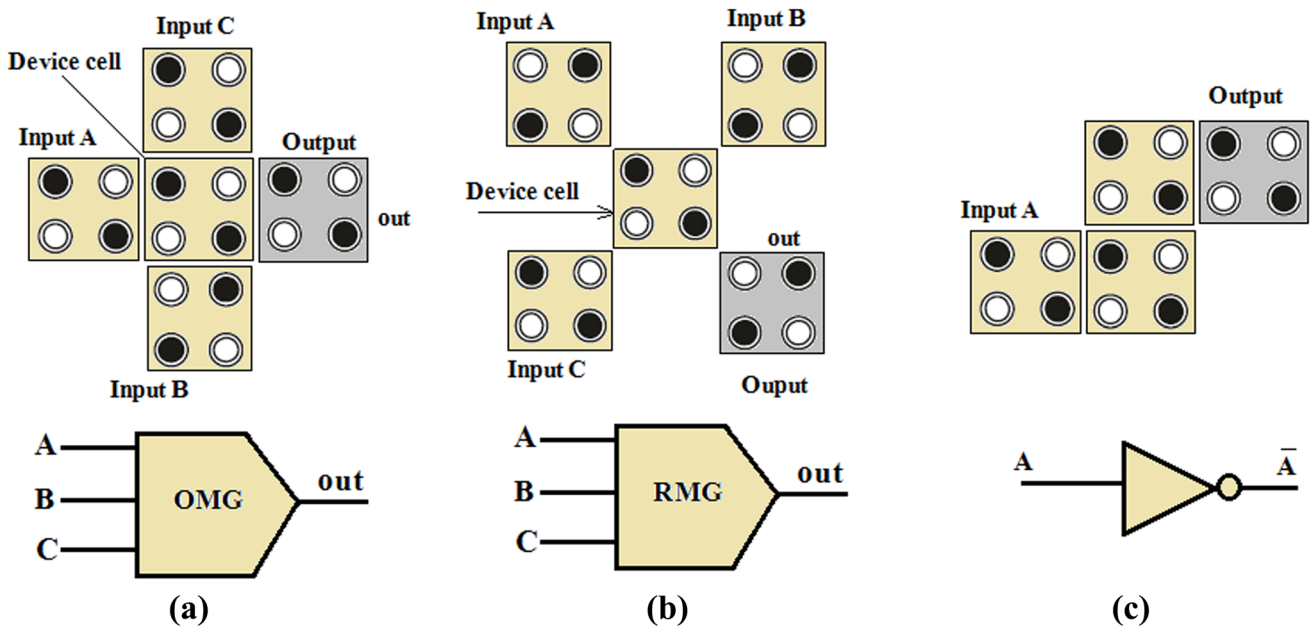


Fig. 3 The fundamental gates in QCA technology, a original majority gate (OMG), b rotate majority gate (RMG) and c inverter gate [6]

These QCA gates are used for the implementation of digital circuits. The logic function of the majority gate is as follows:

$$\text{Out} = AB + AC + BC \tag{2}$$

Based on this equation, the output of the majority gate is “1” where at least two inputs are “1”. It should be noted that the majority gate can be utilized as a 2-input AND or a 2-input OR gate by fixing one of the three input cells to $P = -1$ or $P = +1$, respectively [12]. Figure 4 shows the logical gates implemented by majority gate.

2.4 Clocking in the QCA

Synchronization plays a major role in the QCA circuits. The QCA clock can be utilized to synchronize QCA circuits and provide the required power for functionality. In other words, the clocking zone partitioning is utilized to control the flow direction of the signals and achieve computational pipelining in the QCA circuits. Indeed, each clock zone operates similar a D-latch. The number of zones in the critical path of the QCA circuit determines the overall delay [23,25]. The QCA clock zones are illustrated in Fig. 5. Clocking scheme in the QCA technology consists of four phases namely, switch, hold, release, and relax. Each one of these phases is shifted

Fig. 4 The logical gates implemented by majority gate, **a** 2-input AND gate and **b** 2-input OR gate [6]

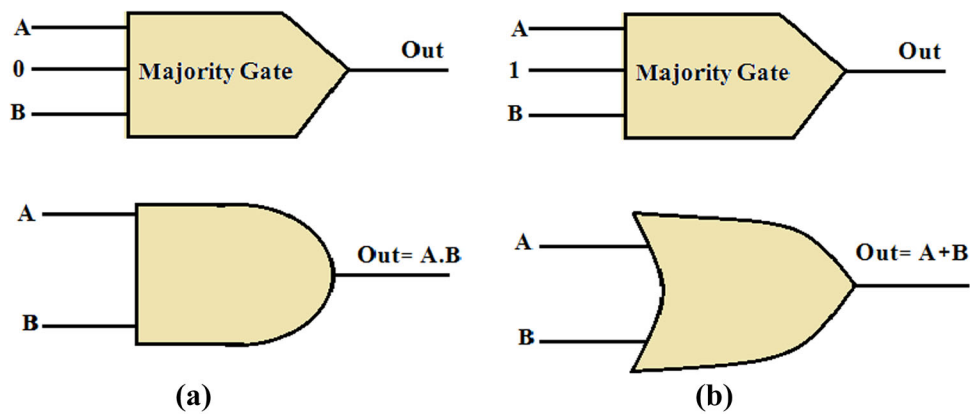
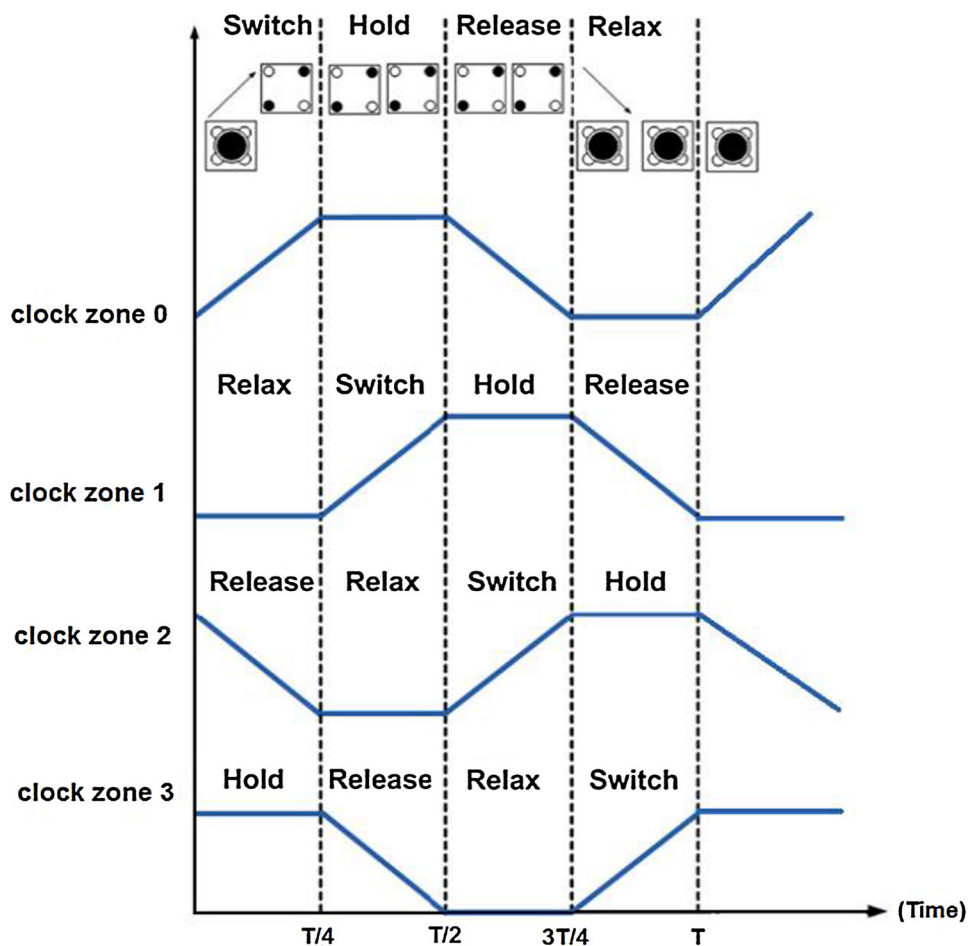


Fig. 5 The four clock signals are used to control the flow direction of the signals within the QCA circuit [25]



by 90° . At the starting of the first phase, switch, the computations are occurred and the QCA cells begin as unpolarized. In switch phase, the inter-dot potential barriers of cells are low. In this phase, the tunneling barriers are raised. At the hold phase, the electrons retain their polarity and barriers of the cells are high enough to prevent electrons from tunneling. During the release phase, the inter-dot potential barriers start to reduce and the cells lose their polarity. Finally, during the fourth clock phase, relax phase, when the clock is

low, the cell barriers remain low and the cells remain in an unpolarized state [5,25].

2.5 Related works

The 2:1 QCA multiplexer architectures presented in [4,12–16,18–21,24–26,28] are based on Fig. 6a. These architectures consist of two 2-input AND gates, a 2-input OR gate, and an inverter gate. The 2:1 QCA multiplexer architecture

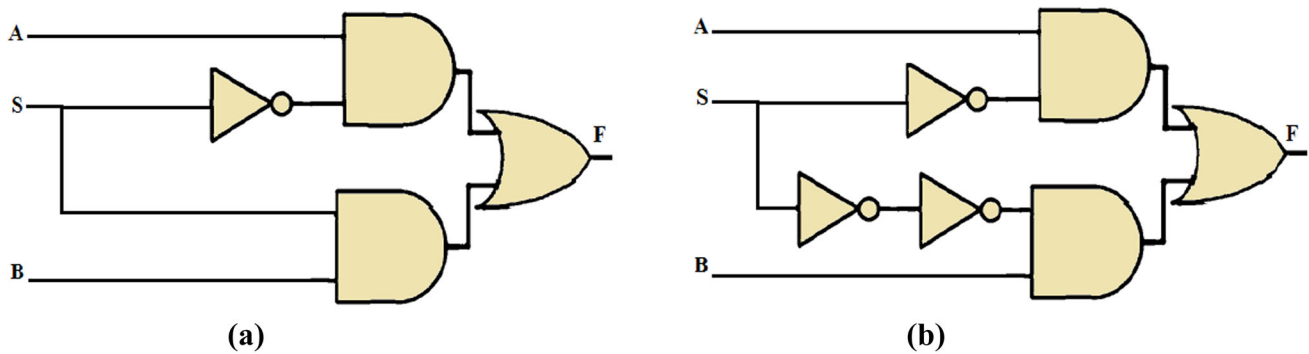


Fig. 6 Schematic logic diagram of the 2:1 QCA multiplexer, **a** in [4, 12–16, 18–21, 24–26, 28] and **b** in [27].

presented in [27] is based on Fig 6b. This architecture consists of two 2-input AND gates, a 2-input OR gate, and two inverter gates.

The QCA multiplexer was addressed for the first time in a primitive work by Gin et al. in [24]. There are several attempts to improve the QCA multiplexer architecture in terms of number of cell, area, and delay [4, 12–16, 18–21, 25–28].

Teodósio and Sousa [18] have proposed two types of the 2:1 QCA multiplexer. The first type of the 2:1 QCA multiplexer is generated using a Layout Generator (LG) tool, which is shown in Fig. 7a. The second type of the 2:1 QCA multiplexer is a handmade structure as shown in Fig. 7b. They concluded that the handmade structure has better performance compared to the LG structure, because the handmade structure involves four QCA clock zones, but the LG structure has been used eight QCA clock zones.

Wu et al. [25] have designed a 2:1 QCA multiplexer architecture which only utilizes four clock zones. Figure 7c shows the multiplexer architecture presented in [25].

Mardiris et al. [26] have presented a 2:1 QCA multiplexer architecture that is shown in Fig. 7d. The layout is designed using block logics such as AND gates, OR gates, and delay blocks in one layer. This architecture is not effectiveness in realizing higher-order $2^n : 1$ multiplexers. This design consists of 67 cells and $0.14 \mu\text{m}^2$ area.

Hashemi et al. [21] have proposed a QCA multiplexer architecture. Their 2:1 QCA multiplexer layout has been constructed in three layers. The first layer, which is the main layer, comprised the backbone of the circuit. Their multiplexer is illustrated in Fig. 7e.

In reference [27], a new 2:1 QCA multiplexer design has been proposed, which consists of 35 cells, and $0.04 \mu\text{m}^2$ area. The presented architecture in [27] is illustrated in Fig. 7f.

Work presented in [20] has proposed a design of a 2:1 QCA multiplexer, which can be used to design $2^n : 1$ QCA multiplexers. This 2:1 QCA multiplexer is shown in

Fig. 7g. Their architecture consists of 56 cells, and $0.07 \mu\text{m}^2$ area.

Roohi et al. [28] have designed and simulated a 2:1 QCA multiplexer architecture, which consists of 27 cells and $0.03 \mu\text{m}^2$ area. Figure 7h depicts the multiplexer presented in [28].

Sen et al [13] have presented a 2:1 QCA multiplexer architecture, which consists of 19 cells, and $0.02 \mu\text{m}^2$ area. This 2:1 QCA multiplexer is shown in Fig 7i.

Sabbaghi Nadooshan and Kianpour [19] have presented and simulated a 2:1 QCA multiplexer architecture, where this design consists of 26 cells and $0.02 \mu\text{m}^2$ area. They have used a model of signal distribution network for implementation of QCA multiplexers. Figure 7j depicts the multiplexer presented in [19].

Sen et al. [12] have also presented a QCA Reversible Arithmetic Logic Unit (RALU) using a reversible multiplexer unit. The 2:1 QCA multiplexer presented in [12] consists of 19 cells. Figure 7k shows the multiplexer presented in [12]. Moreover, they [4] have presented a 2:1 QCA multiplexer architecture which consists of 23 cells and an area of $0.02 \mu\text{m}^2$. Their multiplexer is constructed in one layer. The multiplexer presented in [4] is shown in Fig. 7l. They [15] have also designed and simulated two models of 2:1 QCA multiplexer architecture, which are constructed in 3-layers and 4-layers. Figure 7m, n depicts the 3-layer and 4-layer models of the 2:1 QCA multiplexer architecture, respectively.

3 The proposed QCA multiplexer architectures

In this section, a new and efficient architecture is presented for 2:1 QCA multiplexer, and then new and efficient architectures are presented for 4:1 QCA multiplexer and 8:1 QCA multiplexer as described later. We use the basic QCA logic gates such as the majority gate and the inverter gate in the implementation of the proposed architectures.

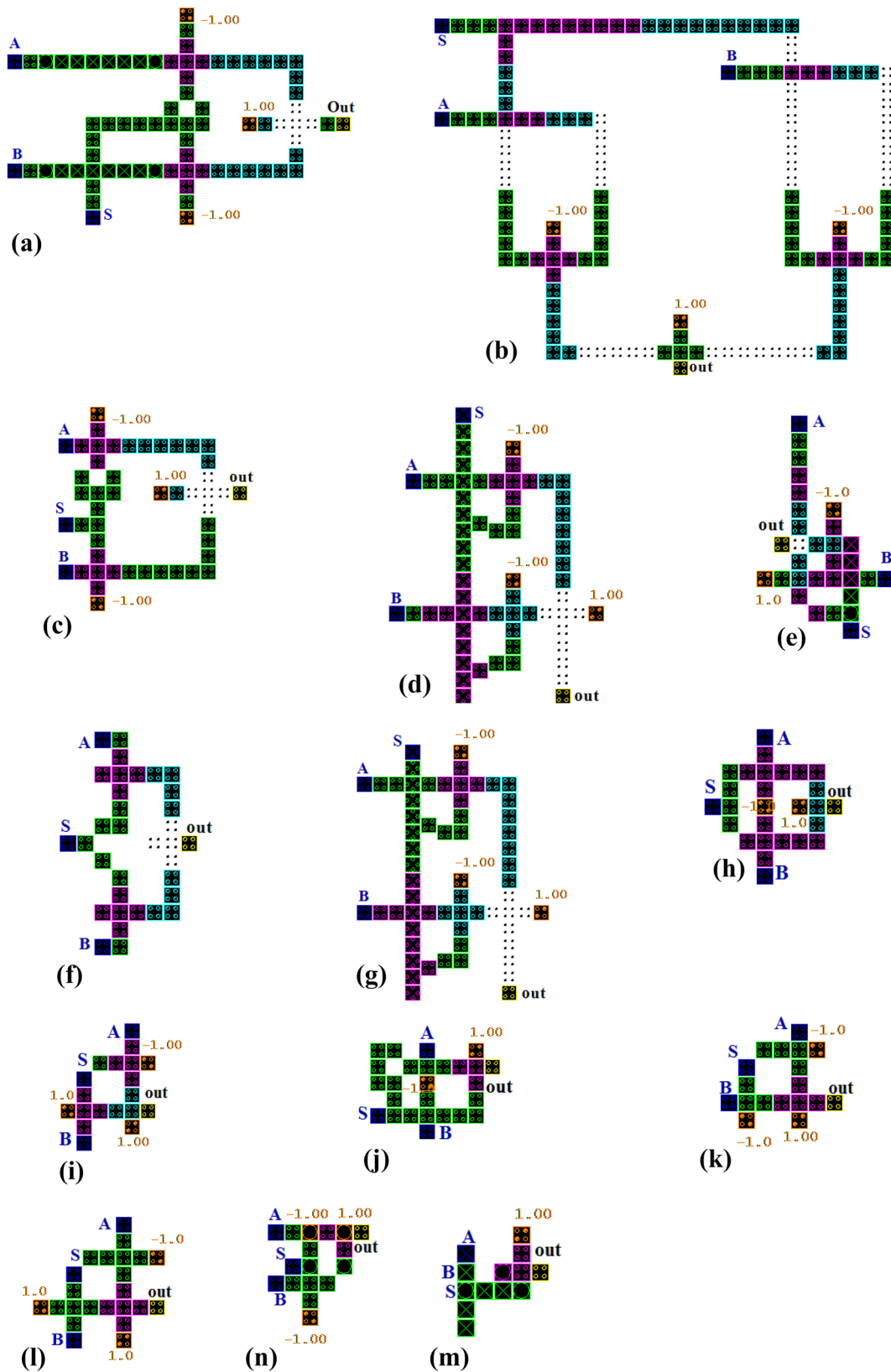
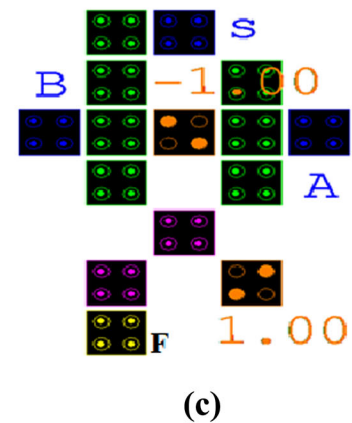
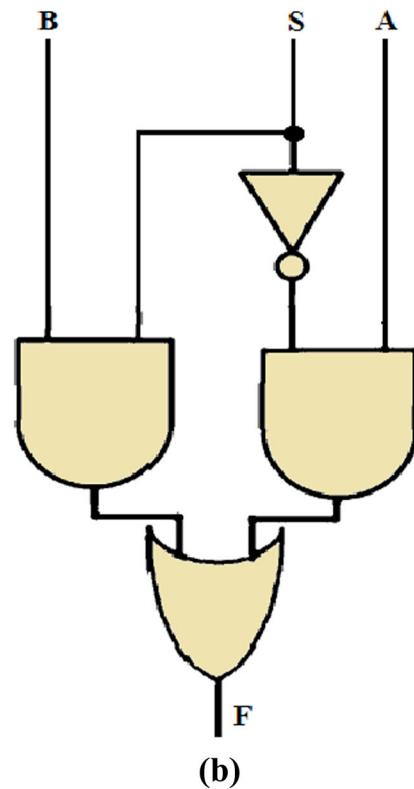
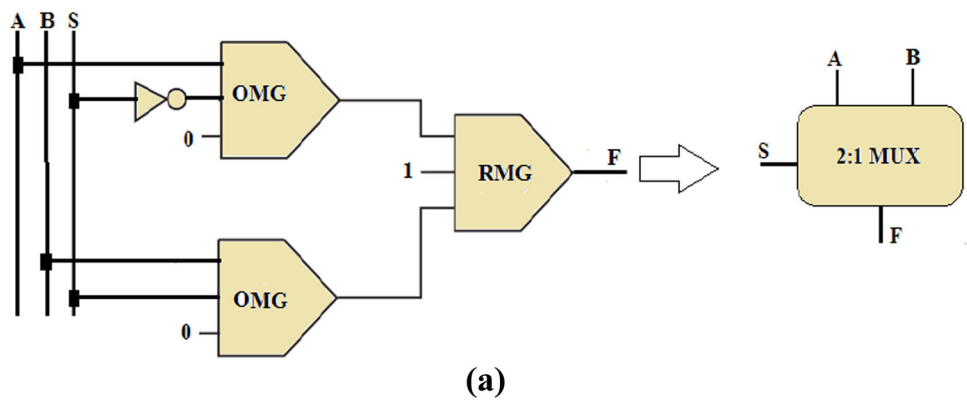


Fig. 7 The 2:1 QCA multiplexer architectures, **a** in [18] generated by QCALG, **b** in [18] handmade, **c** in [25], **d** in [26], **e** in [21], **f** in [27], **g** in [20], **h** in [28], **i** in [13], **j** in [19], **k** in [12], **l** in [4], **m** in [[14]–3L] and **n** in [[14]–4L]

Fig. 8 The proposed 2:1 QCA multiplexer architecture, **a** the block diagram of the proposed 2:1 QCA multiplexer architecture, **b** the logic block of the proposed 2:1 QCA multiplexer architecture and **c** the layout of the proposed 2:1 QCA multiplexer architecture



3.1 The 2:1 QCA multiplexer architecture

Figure 8a shows the block diagram of the proposed 2:1 QCA multiplexer architecture. Figure 8b shows the logic block of the proposed 2:1 QCA multiplexer architecture, and Fig. 8c shows the layout of the proposed 2:1 QCA multiplexer architecture in QCADesigner. As is shown in Fig. 8b, the proposed 2:1 QCA multiplexer is implemented using two AND gates and an inverter gate in the inputs and one OR gate in the output.

The proposed 2:1 QCA multiplexer architecture has two inputs, an address line, and an output. The inputs are labeled as A and B and the output is shown by F. Here the address

line named as S. It can be seen that, when S is 0, input A is selected, and when S is 1, input B appears at the output. The logic function of the proposed architecture can be expressed as follows:

$$F = A.\bar{S} + B.S \tag{3}$$

The majority gate representation of this function is $F = \text{Maj}(\text{Maj}(\bar{S}, A, 0), \text{Maj}(S, B, 0), 1)$. This architecture contains two original majority gates: a rotate majority gate and an inverter gate. The proposed 2:1 QCA multiplexer takes only one clock zone to generate the AND function, and it takes one clock zone to execute the OR function.

3.2 The proposed 4:1 QCA multiplexer architecture

Figure 9a shows the block diagram and logic block of the proposed 4:1 QCA multiplexer architecture, and Fig. 9b shows the layout of the proposed 4:1 QCA multiplexer architecture.

The proposed 4:1 QCA multiplexer architecture consists of three proposed 2:1 QCA multiplexer architectures. This architecture has four inputs, two address lines, and one output. The inputs are labeled as A, B, C, and D and the output is shown by F. In addition, the address lines named as S0, S1. It can be seen that, if both S0 and S1 are 0, input A appears at the output. When S0 is 1 and S1 is 0, the output F will become B, when S0 is 0 and S1 is 1, input D is selected and when both S0 and S1 are 1, input C appears at the output. The logic function of the proposed architecture can be expressed as follows:

$$F = (\bar{S}0.\bar{S}1)A + (S0.\bar{S}1)B + (\bar{S}0.S1)D + (S0.S1)C \quad (4)$$

3.3 The proposed 8:1 QCA multiplexer architecture

Figure 10a shows the logic block of the proposed 8:1 QCA multiplexer architecture. Figure 10b shows the block diagram and the truth table of the proposed 8:1 QCA multiplexer, and Fig. 10c shows the layout of the proposed 8:1 QCA multiplexer.

As it is shown in Fig. 10b, the proposed architecture has been implemented using two proposed 4:1 QCA multiplexers and one proposed 2:1 QCA multiplexer. The proposed 8:1 QCA multiplexer architecture has eight inputs, three address lines, and one output. The inputs are labeled as A, B, C, D, E, F, G, and H and the output is shown by word “out”. Here, S0, S1, and S2 signals are utilized as address lines. The output of the proposed architecture can be shown as follows:

$$\begin{aligned} \text{out} = & (\bar{S}2.\bar{S}1.\bar{S}0)A + (\bar{S}2.\bar{S}1.S0)B + (\bar{S}2.S1.\bar{S}0)C \\ & + (\bar{S}2.S1.S0)D + (S2.\bar{S}1.\bar{S}0)E + (S2.\bar{S}1.S0)F \\ & + (S2.S1.\bar{S}0)G + (S2.S1.S0)H \end{aligned} \quad (5)$$

For example, when address lines are 0, input A appears at the output, when S0 is 1 and the both S1 and S2 are 0, the output will become B, and when S0 and S1 are 0 and S2 is 1, input E is selected to appear at the output. The rest states are shown in the truth table in Fig. 10b.

4 The simulation results

4.1 The proposed 2:1 QCA multiplexer architecture

Simulation results have been acquired using the QCADesigner tool version 2.0.1 [23] that is a simulation tool for QCA

circuits. The simulation results of the proposed 2:1 QCA multiplexer are shown in Fig. 11. It should be noted that there are two types of simulation engines in QCADesigner: a bi-stable approximation and a coherence vector [23]. We have simulated the proposed 2:1 QCA multiplexer architecture in QCADesigner simulator version 2.0.1 in the bi-stable approximation simulation engine, because it is faster than coherence vector. The utilized parameters for the simulation are as follows: the number of samples: 220,000, radius of effect: 41 nm, clock low: $3.8e-22$, clock high: $9.8e-22$, lower threshold: -0.5 , upper threshold: 0.5 , and cell size: 18 nm, temperature = 1 K. The rest of the parameters are selected as default.

The simulation results of the proposed 2:1 QCA multiplexer architecture, which are shown in Fig. 11, confirm that the output is correctly achieved after two clock zones delay. In addition, the proposed 2:1 QCA multiplexer consists of 15 cells and an area of $0.01 \mu\text{m}^2$.

4.2 The proposed 4:1 QCA multiplexer architecture

We have simulated the proposed 4:1 QCA multiplexer architecture in the QCADesigner version 2.0.1 in the bi-stable approximation simulation engine. The utilized parameters for simulation are as follows: the number of samples: 26,903, radius of effect: 65 nm, clock low: $3.8e-22$, clock high: $9.8e-22$, lower threshold: -0.5 , upper threshold: 0.5 , and cell size: 18 nm, temperature = 1 K. The rest of the parameters are selected as default. The QCADesigner simulation results of the proposed 4:1 QCA multiplexer are shown in Fig. 12.

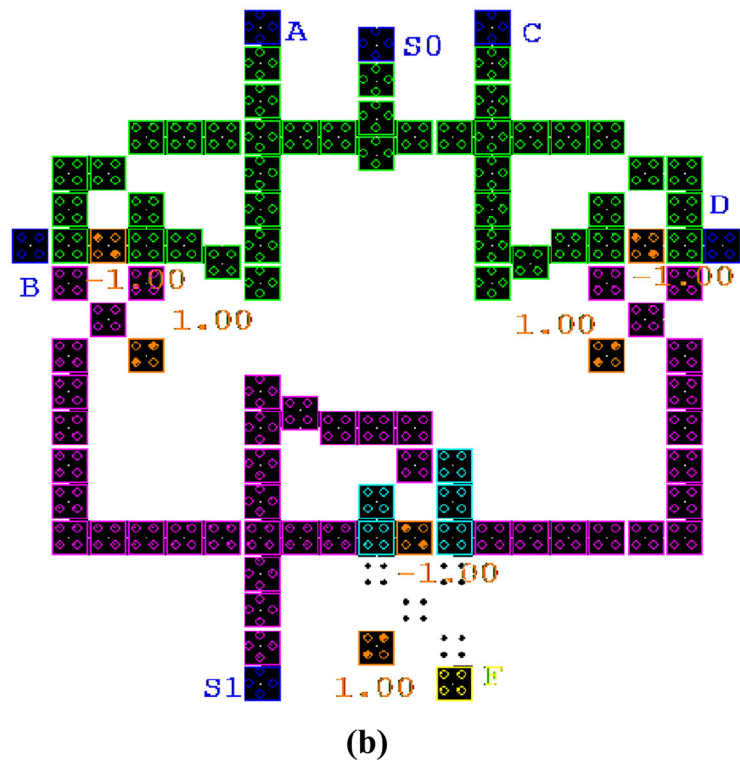
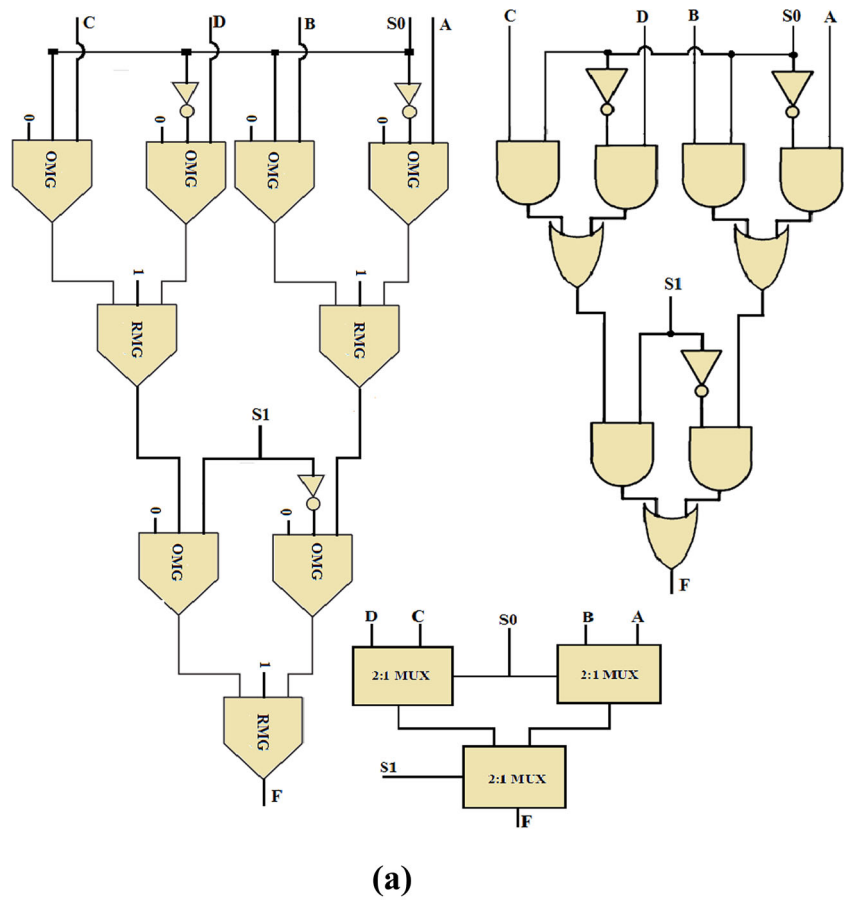
The simulation results of the proposed 4:1 QCA multiplexer architecture confirm that the output is correctly achieved after four clock zones delay. Moreover, the proposed 4:1 QCA multiplexer consists of 107 cells and an area of $0.15 \mu\text{m}^2$.

4.3 The proposed 8:1 QCA multiplexer architecture

Simulation results of the proposed 8:1 QCA multiplexer architecture have been acquired using the QCADesigner tool version 2.0.1 [23] in the bi-stable approximation simulation engine. Figure 13 shows these simulation results. The utilized parameters for simulation are as follows: the number of samples: 209,025, radius of effect: 65 nm, clock Low: $3.8e-22$, clock high: $9.8e-22$, lower threshold: -0.5 , upper threshold: 0.5 , and cell size: 18 nm, temperature = 1 K. The rest of the parameters are selected as default.

The simulation results of the proposed 8:1 QCA multiplexer architecture confirm that the output is correctly achieved after six clock zones delay. Moreover, the proposed 8:1 QCA multiplexer consists of 293 cells and an area of $0.49 \mu\text{m}^2$

Fig. 9 The proposed 4:1 QCA multiplexer architecture, **a** the block diagram and logic block of the proposed 4:1 QCA multiplexer architecture, **b** the layout of the proposed 4:1 QCA multiplexer architecture



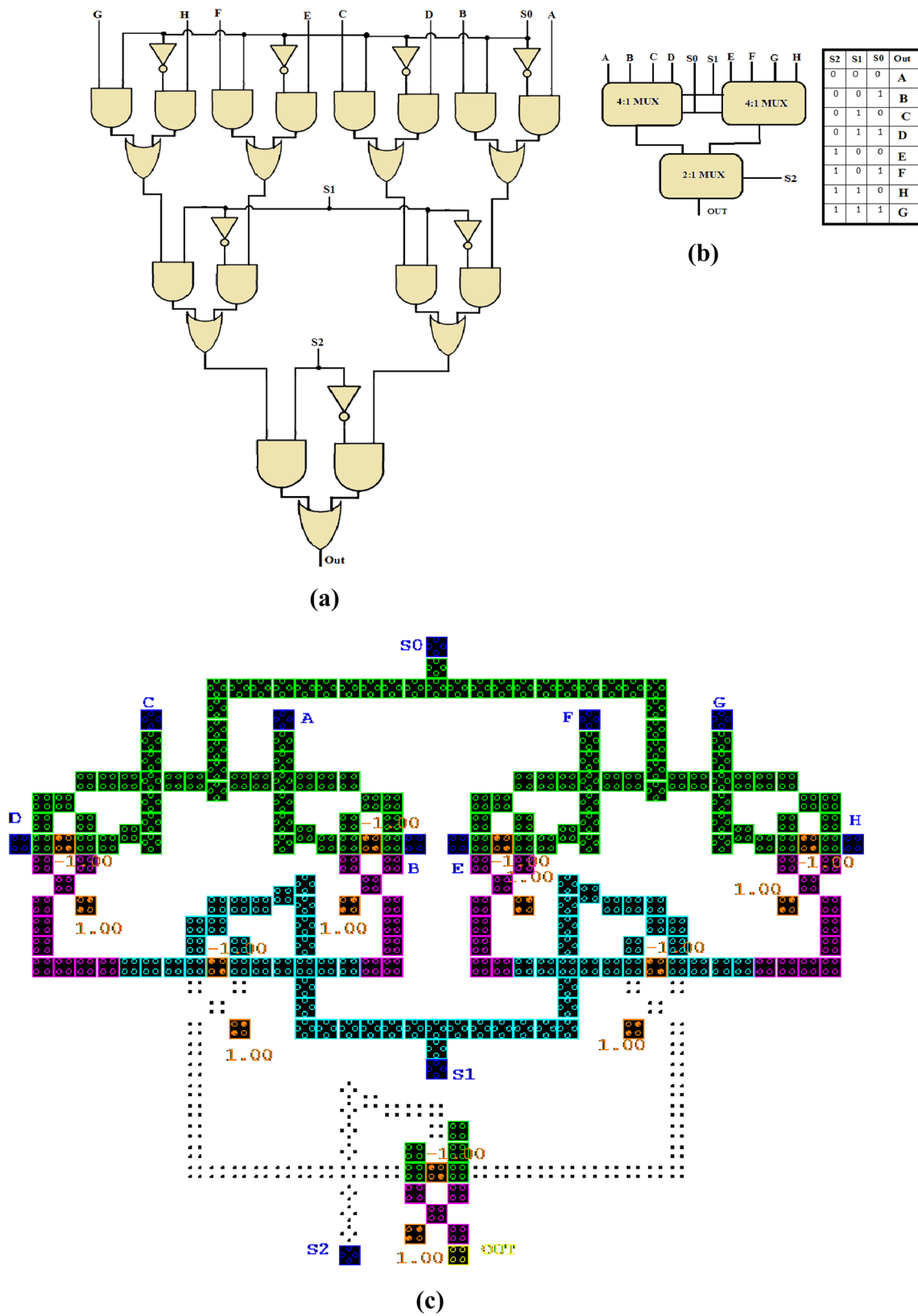


Fig. 10 The proposed 8:1 QCA multiplexer architecture, **a** the logic block of the proposed 8:1 QCA multiplexer architecture, **b** the block diagram and truth table of the proposed 8:1 QCA multiplexer architecture and **c** the layout of the proposed 8:1 QCA multiplexer architecture

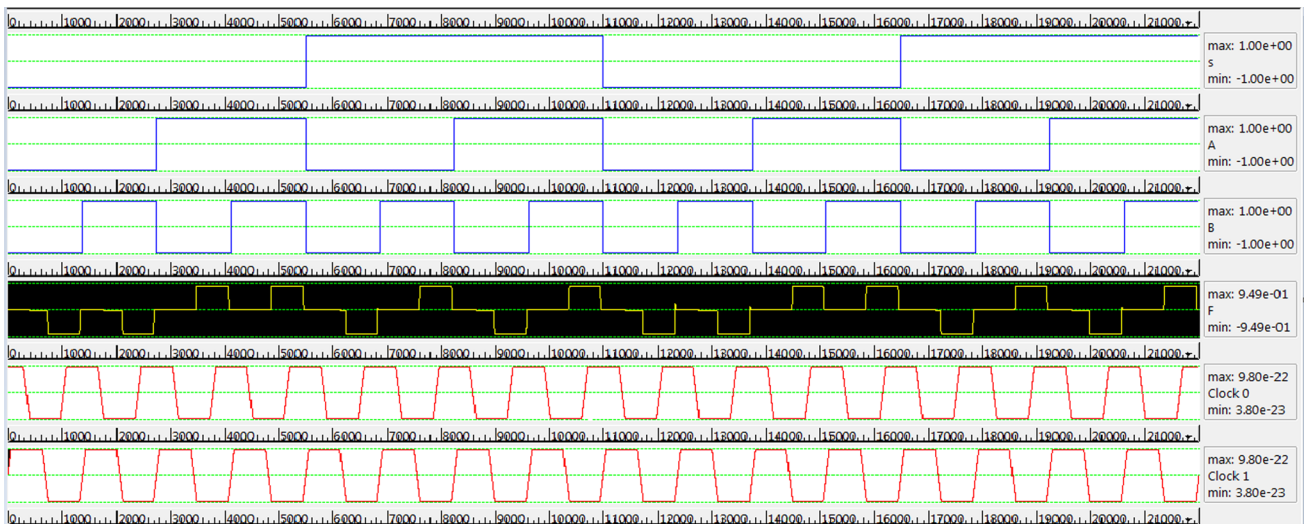


Fig. 11 The simulation results of the proposed 2:1 QCA multiplexer architecture

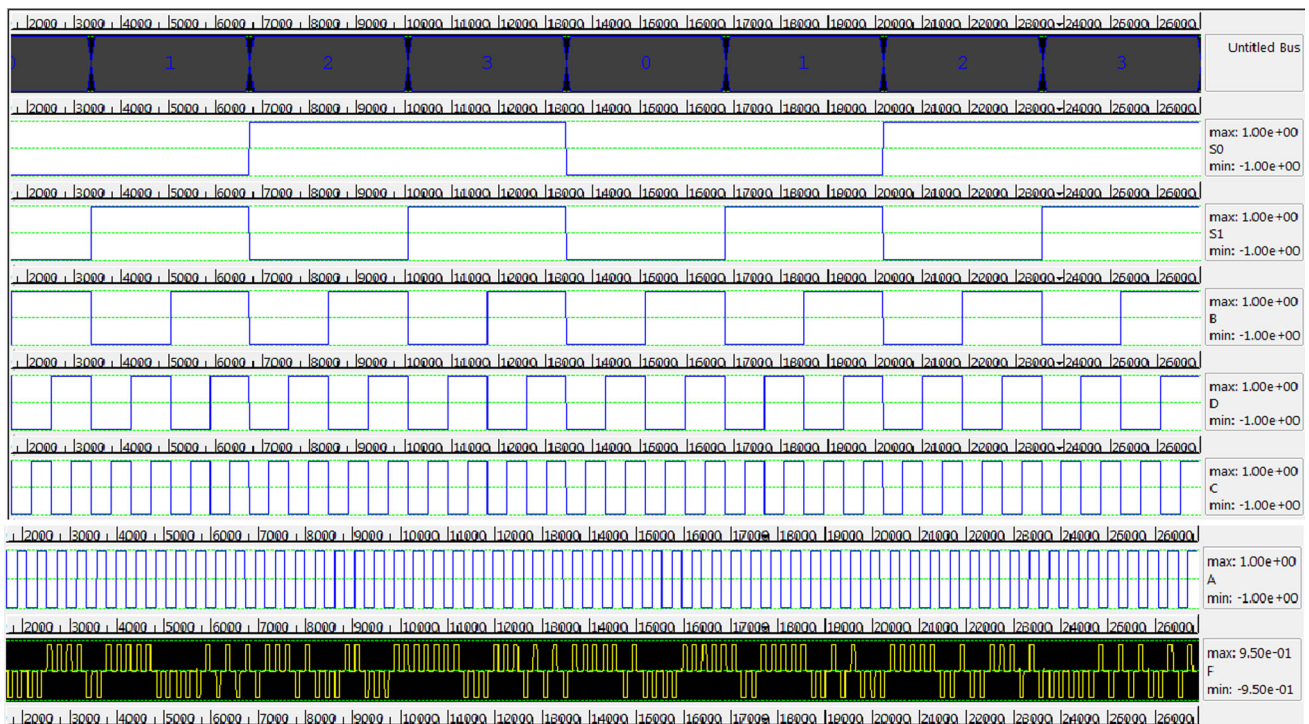


Fig. 12 The simulation results of the proposed 4:1 QCA multiplexer architecture

5 The performance comparison

The simulation results of the proposed 2:1 QCA multiplexer architecture compared to the other 2:1 QCA multiplexer architectures in [4, 12–15, 18–21, 25–28] are summarized in Table 1.

In Table 1, delay is shown in terms of the number of required clock zones, area is shown in terms of μm^2 , complexity is shown in terms of the number of required cells, the

ratio denotes the ratio of each parameter of 2:1 QCA multiplexer architecture of each reference in comparison with this parameter in the proposed 2:1 QCA multiplexer architecture, cell size is shown in terms of (nm), and L denotes the layer, for example 3L shows that this architecture is simulated in 3 layers.

Based on our simulation results, which are shown in Table 1, Figs. 8 and 11, the proposed 2:1 QCA multiplexer architecture has an improvement in resulting complexity

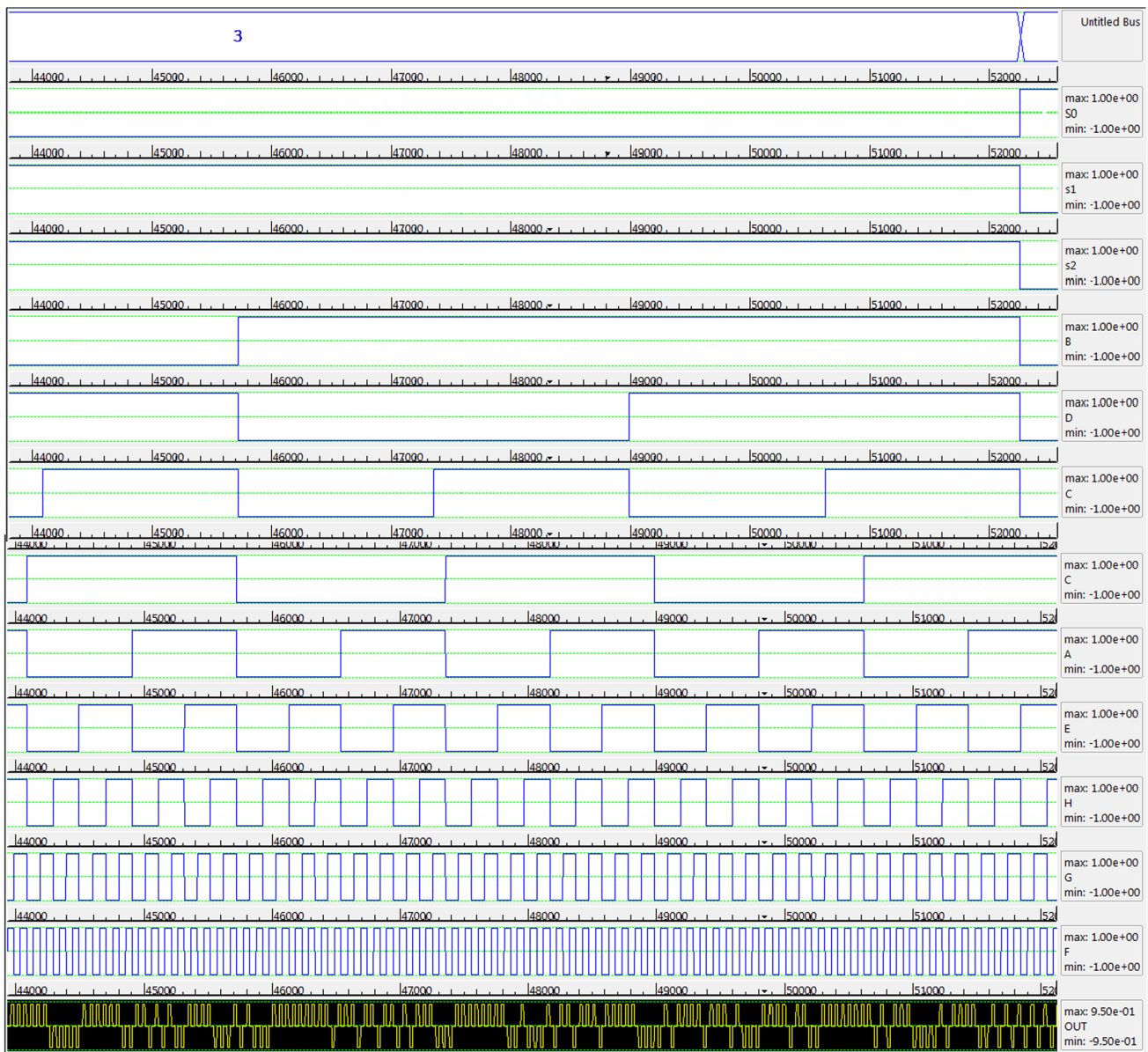


Fig. 13 The simulation results of the proposed 8:1 QCA multiplexer architecture

compared to other 2:1 QCA multiplexer architectures [4, 12–15, 18–21, 25–28].

Table 2 summarizes the simulation results of the proposed 4:1 QCA multiplexer in comparison with other 4:1 QCA multiplexer architectures [4, 14–16, 19, 20, 26, 27, 29] in terms of the complexity (cell count), delay (clock zone), and area (μm^2).

Based on our simulation results which are shown in Table 2, Figs. 9 and 12, the proposed 4:1 QCA multiplexer architecture has a better performance compared to the other 4:1 QCA multiplexer architectures in [4, 14–16, 19, 20, 26, 27, 29] in terms of complexity, delay, and area. The only 4:1 QCA multiplexer architectures that have a slightly better area and

the complexity are the 4:1 QCA multiplexer architectures of [15]. However, these advantages have been resulted from the increased number of layout layers utilized for logic structures and interconnections, not from logic design.

Table 3 summarizes the simulation results of the proposed 8:1 QCA multiplexer in comparison with other 8:1 QCA multiplexer architectures [4, 16, 19, 20, 29] in terms of the complexity (cell count), delay (clock zone), and area (μm^2).

Based on our simulation results, which are shown in Table 3, Figs. 10 and 13, the proposed 8:1 QCA multiplexer architecture provides an improvement on resulting complexity, delay, and area in comparison with the other 8:1 QCA multiplexer architectures in [4, 16, 19, 20, 29].

Table 1 The comparative table for the 2:1 QCA multiplexer architectures

Reference	Complexity (# cells)	Ratio	Area (μm^2)	Delay (clock zones)	Ratio	Wire crossing	Cell size (nm \times nm)
[18] using QCALG	146	8.5	0.28	8	4	Multilayer	18 \times 18
[18] handmade	88	5.9	0.14	4	2	Multilayer	18 \times 18
[25]	46	3.1	0.08	4	2	Coplanar	Not available
[26]	67	4.5	0.14	4	2	Coplanar	18 \times 18
[21]	36	2.4	0.06	4	2	Multilayer	Not available
[27]	35	2.3	0.04	4	2	Coplanar	18 \times 18
[20]	56	3.8	0.07	4	2	Coplanar	18 \times 18
[28]	27	1.8	0.03	3	1.5	Coplanar	18 \times 18
[13]	19	1.3	0.02	3	1.5	Coplanar	18 \times 18
[19]	26	1.7	0.02	2	1	Coplanar	18 \times 18
[12]	19	1.8	0.02	2	1	Coplanar	18 \times 18
[15] 3L	23	1.5	0.01	2	1	Multilayer	18 \times 18
[15] 4L	22	1.5	0.01	2	1	Multilayer	18 \times 18
[4]	23	1.5	0.02	2	1	Coplanar	18 \times 18
This paper	15	1	0.01	2	1	Coplanar	18 \times 18

Table 2 The comparative table for the 4:1 QCA multiplexer architectures

Reference	Complexity (# cells)	Ratio	Area (μm^2)	Delay (clock zones)	Ratio	Wire crossing	Cell size (nm \times nm)
[26]	215	2	0.25	6	1.5	Coplanar	18 \times 18
[29]	223	2	0.22	6	1.5	Multilayer	18 \times 18
[27]	124	1.2	0.25	8	2	Coplanar	18 \times 18
[20]	290	2.7	0.35	7	1.8	Coplanar	18 \times 18
[19]	271	2.5	0.37	19	4.8	Coplanar	18 \times 18
[15] 3L	103	0.97	0.08	7	1.8	Multilayer	18 \times 18
[15] 4L	94	0.88	0.07	6	1.5	Multilayer	18 \times 18
[4]	155	1.5	0.24	5	1.3	Coplanar	18 \times 18
[16]	251	2.4	0.2	5	1.3	Multilayer	18 \times 18
[16]	199	1.9	0.27	6	1.8	Coplanar	18 \times 18
This paper	107	1	0.15	4	1	Coplanar	18 \times 18

Table 3 The comparative table for the 8:1 QCA multiplexer architectures

Reference	Complexity (# cells)	Ratio	Area (μm^2)	Delay (clock zones)	Ratio	Cell size (nm \times nm)
[29]	576	1.97	0.82	9	1.5	18 \times 18
[20]	633	2.2	0.67	11	1.8	18 \times 18
[19]	1312	4.5	1.83	42	7	18 \times 18
[4]	462	1.6	0.87	7	1.5	18 \times 18
[16]	608	2.1	0.71	9	1.5	18 \times 18
[16]	494	1.7	0.58	9	1.5	18 \times 18
This paper	293	1	0.58	6	1	18 \times 18

Therefore, the proposed QCA multiplexer architectures have a better performance compared to other QCA multiplexer architectures in [4, 12, 13, 15, 16, 18–21, 25–29].

6 Conclusions

Multiplexers play a vital role in circuit designs. Hence, this paper proposed, simulated and evaluated new and efficient architectures for 2:1, 4:1, and 8:1 QCA multiplexers. We have used the coplanar crossover approach for implementing the proposed QCA multiplexer architectures. The proposed QCA multiplexer architectures are simulated using QCADesigner version 2.0.1. The simulation results showed that the proposed QCA multiplexer architectures provide an improvement on the resulting complexity (cell count), delay (clock zone), and area (μm^2) in comparison with other QCA multiplexer architectures in [4, 12, 13, 15, 16, 18–21, 25–29].

References

- Compano, R., Molenkamp, L., Paul, D.J.: Roadmap for Nanoelectronics. (2001)
- Sen, B., Dutta, M., Mukherjee, R., Nath, R.K., Sinha, A.P., Sikdar, B.K.: Towards the design of hybrid QCA tiles targeting high fault tolerance. *J. Comput. Electron.* (2015). doi:10.1007/s10825-015-0760-7
- Rezai, A., Keshavarzi, P., Mahdiye, R.: A novel MLP network implementation in CMOL technology. *Eng. Sci. Technol. Int. J. (JESTECH)* **17**(3), 165–172 (2014)
- Sen, B., Goswami, M., mazumdar, S., Sikdar, B.K.: Towards modular design of reliable quantum-dot cellular automata logic circuit using multiplexers. *Comput. Electr. Eng.* **45**, 42–54 (2015)
- Lent, C.S., Tougaw, P.D.: A device architecture for computing with quantum dots. *Proc. IEEE* **85**, 541–557 (1997)
- Roohi, A., Demara, R., Khoshavi, N.: Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder. *Microelectron. J.* **46**, 531–542 (2015)
- Hayati, M., Rezaei, A.: Design of novel efficient adder and subtractor for quantum-dot cellular automata. *Int. J. Circuit Theory Appl.* **43**(10), 1446–1454 (2015)
- Pudi, V., Sridharan, K.: New decomposition theorems on majority logic for low-delay adder designs in quantum dot cellular automata. *IEEE Trans. Circuits Syst.* **59**(10), 678–682 (2012)
- Perri, S., Corsonello, P.: New methodology for the design of efficient binary addition in QCA. *IEEE Trans. Nanotechnol.* **11**(6), 1192–1200 (2012)
- Lu, L., Liu, W., O'Neill, M., Swartzlander Jr., E.E.: QCA systolic array design. *IEEE Trans. Comput.* **62**(3), 548–560 (2013)
- Wood, J.D., Tougaw, D.: Matrix multiplication using quantum-dot cellular automata to implement conventional micro-electronics. *IEEE Trans. Nanotechnol.* **10**(5), 1036–1042 (2011)
- Sen, B., Dutta, M., Goswami, M., Sikdar, B.K.: Modular design of testable reversible ALU by QCA multiplexer with increase in programmability. *Microelectron. J.* **45**, 1522–1532 (2014)
- Sen, B., Dutta, M., Saran, D., Sikdar, B.K.: An efficient multiplexer in quantum-dot cellular automata. In: *Progress in VLSI Design and Test. Lecture Notes in Computer Science*, vol. 7373, pp. 350–351. Springer, Berlin (2012)
- Sen, B., Nag, A., De, A., Sikdar, B.K.: Multilayer design of QCA multiplexer. In: *Proceedings of the IEEE India Conference (INDICON)*, pp. 1–6 (2013)
- Sen, B., Nag, A., A, De, Sikdar, B.K.: Towards the hierarchical design of multilayer QCA logic circuit. *J. Comput. Sci.* **11**, 233–244 (2015)
- Cocorullo, G., Corsonello, P., Frustaci, F., Perri, S.: Design of efficient QCA multiplexers. *Int. J. Circuit Theory Appl.* **44**(3), 602–615 (2016)
- Tung, C.C., Rungta, R.B., Peskin, E.R.: Simulation of a QCA-based CLB and a Multi- CLB application. In: *Proceedings of the IEEE International Conference on Field-Programmable Technology (FPT 2009)*, pp. 62–69 (2009)
- Teodósio, T., Sousa, L.: QCA-LG: A tool for the automatic layout generation of QCA combinational circuits. In: *Proceedings of the 25th IEEE Norchip Conference*, pp. 1–5 (2007)
- Sabbaghi-Nadooshan, R., Kianpour, M.: A novel QCA implementation of MUX-based universal shift register. *J. Comput. Electron.* **13**, 1–13 (2013)
- Mardiris, V.A., Karafyllidis, I.G.: Design and simulation of modular 2^n to 1 quantum-dot cellular automata (QCA) multiplexers. *Int. J. Circuit Theory Appl.* **38**, 771–785 (2010)
- Hashemi, S., Azghadi, M., Zakerolhosseini, A.: A novel QCA multiplexer design. In: *Proceedings of the IEEE International Symposium on Telecommunications*, pp. 692–696 (2008)
- waj, M.G., dakhole, P.K.: Design and Simulation of New XOR Gate and Code converters using Quantum Dot Cellular Automata with reduced number of wire crossings. In: *Proceedings of the IEEE International Conference on Circuit, Power and Computing Technologies, (ICCPCT 2014)*, pp. 1245–1250 (2014)
- Walus, K., Dysart, T., Jullien, G.A., Budiman, R.: QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata. *IEEE Trans. Nanotechnol.* **3**, 26–29 (2004)
- Gin, A., Williams, S., Meng, H., Tougaw, P.D.: Hierarchical design of quantum-dot cellular automata devices. *J. Appl. Phys.* **85**(7), 3713–3722 (1999)
- Kim, K., Wu, K., Karri, R.: The robust QCA adder designs using composable QCA building blocks. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **26**, 76–183 (2007)
- Mardiris, V., Mizas, C.H., Fragidis, L., Chatzis, V.: Design and simulation of a QCA 2 to 1 multiplexer. In: *Proceedings of the 12th WSEAS International Conference on Computers*, pp. 572–576 (2008)
- Askari, M., Taghizadeh, M., Farhad, K.: Digital design using quantum-dot cellular automata (a nanotechnology method). In: *Proceedings of the IEEE International Conference on Computer and Communication Engineering. (ICCCE 2008)*, pp. 952–955 (2008)
- Roohi, A., Khademolhosseini, H., Sayedsalehi, S., Navi, K.: A novel architecture for quantum-dot cellular automata multiplexer. *Int. J. Comput. Sci. Issues* **8**, 55–60 (2011)
- Vankamamidi, V., Ottavi, M., Lombardi, F.: Two-dimensional schemes for clocking/timing of QCA circuits. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **27**(1), 34–44 (2008)