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Dual-material double-gate tunnel FET: gate threshold voltage modeling and extraction

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Abstract A new analytical model for the gate threshold voltage (V_{TG}) of a dual-material double-gate (DMDG) tunnel field-effect transistor (TFET) is reported. The model is derived by solving the quasi-two-dimensional Poisson's equation in the lightly doped Si film and employing the physical definition of V_{TG}. A numerical simulation study of the transfer characteristics and V_{TG} of a DMDG TFET has been carried out to verify the proposed analytical model. In the numerical calculations, extraction of V_{TG} is performed based on the transconductance change method as already used for conventional metal–oxide–semiconductor FETs (MOSFETs). The effects of gate length scaling, Si film thickness scaling, and modification of the gate dielectric on V_{TG} are reported. The dependence of V_{TG} on the applied drain bias is investigated using the proposed model. The proposed model can predict the effect of variation of all these parameters with reasonable accuracy.

Keywords Dual-material double gate · Tunnel FET · Threshold voltage · Poisson's equation · Transconductance

1 Introduction

Due to the nonscalability of the subthreshold swing (SS), increasing power density is a major challenge for continued MOSFET scaling. The SS of a MOSFET is limited to 60 mV/dec, resulting in increased leakage current in the subthreshold region. One of the promising device designs to replace MOSFETs is the TFET, which has shown potential to overcome the SS limit of MOSFETs [1–5]. Because of their low OFF currents (in the range of femtoamps), they are ideally suited for low-power and low-standby-power logic applications operating at moderate frequencies [6]. Other promising applications of TFETs include ultralow-power specialized analog integrated circuits with improved temperature stability [7,8]. Although TFETs seem to be well adapted as candidates for ultimately scaled quasi-ideal switches, their unacceptably low ON current [lower than International Technology Roadmap for Semiconductors (ITRS) requirements] is the greatest challenge to their application. Besides, TFETs often exhibit delayed saturation in their output characteristic, which is detrimental for complementary metal–oxide–semiconductor (CMOS) applications. In addition, strong drain-induced barrier lowering (DIBL) effects are sometimes manifested in TFETs, which may severely limit the utility of such devices. Additive combination of many technology boosters has been proposed to increase the tunneling current and optimize device performance [9–16].

Some work has used bandgap engineering or heterostructuring of the channel (strained SiGe) [9,10] or source material (low-bandgap Ge) [11]. Several studies have shown how gate work-function engineering [12] or use of high-k dielectric [13] can help to improve the coupling between the gate and tunnel junction to boost the ON current. In [14–16], the effect of device structure engineering on TFET performance was investigated. Multiple-gate structures have also been explored for improvement of TFET device performance. Saurabh and Kumar [17] proposed the application of a dual-material double-gate (DMDG) structure in TFET devices for optimization of ON current, threshold voltage, SS, and immunity to DIBL effects.

The most important electrical parameter for a solid-state switch is probably its threshold voltage. While a number of

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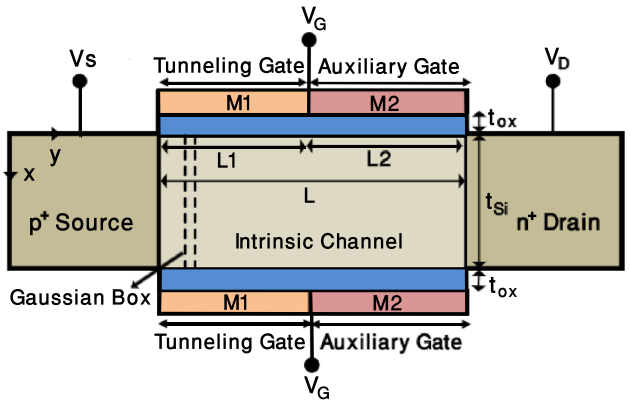

Fig. 1 Schematic of *n*-type DMDG TFET

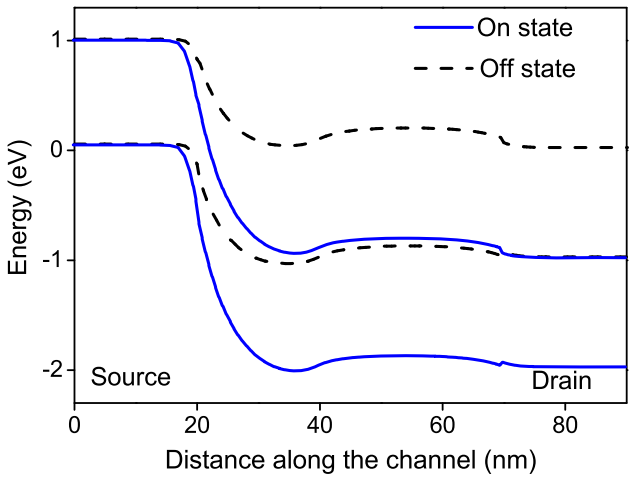

Fig. 2 Band diagrams for DMDG TFET in OFF state (*dotted lines*; $V_{DS} = 0\,V$, $V_{GS} = 0\,V$) and ON state (*solid lines*; $V_{DS} = 0.5\,V$, $V_{GS} = 1\,V$)

analytical models [18–21] have been proposed for the potential, electric field, and drain current of the DMDG structure, no threshold voltage models have been proposed to date. Since analytical models are useful to provide further insight into the working principles of a device, in this work, a threshold voltage model for a DMDG TFET is proposed. Model validation has been carried out by comparing model results with two-dimensional (2-D) device simulation results. The effects of device physical parameters such as the gate length, channel thickness, and gate dielectric, as well as the effect of the drain bias on the gate threshold voltage have been observed. The proposed model can be used as an efficient tool for design and fabrication of DMDG TFET devices.

2 Device structure and parameters

A schematic diagram of the structure of an *n*-type DMDG TFET is shown in Fig. 1. A DMDG TFET is a gated *p*–i–*n* diode with gates made from two metals with different work functions. The metal gate near to the drain is called the auxiliary gate; its work-function variation mainly controls the OFF-state current. The metal gate near the source side is called the tunnel gate; it controls the tunneling in the source–body junction. When the tunneling gate has a lower work function than the auxiliary gate, higher I_{ON}, lower I_{OFF}, and better SS are achieved. Electrons tunnel from the valence band of the source to the conduction band of the intrinsic body and then move towards the drain end through a drift–diffusion mechanism. Tunneling occurs in the region of high electric field (source–body interface), where local band bending reduces the width of the energy barrier. Band bending is achieved by applying a reverse bias at the gate, which pushes the energy band downwards and turns on the device (Fig. 2).

The values of the metal work functions used in this work are $\Phi_{tunnel} = 4\,eV$ (e.g., Ni–Ti, Mo) and $\Phi_{auxiliary} = 4.4\,eV$ (e.g., W, Ta). The source and drain are made of highly doped *p*-type and *n*-type regions with doping levels of $N_{source} = 10^{20}\,cm^{-3}$ and $N_{drain} = 10^{19}\,cm^{-3}$, respectively. The body region is lightly *n*-type doped with $N_{channel} = 10^{17}\,cm^{-3}$. Other device parameters are: channel length, $L = 100\,nm$ where $L_1 = 50\,nm$, $L_2 = 50\,nm$; silicon film thickness, $t_{Si} = 10\,nm$; oxide thickness, $t_{ox} = 2\,nm$. The dielectrics used here are SiO_2 ($\epsilon_{ox} = 3.9$), Si_3N_4 ($\epsilon_{ox} = 7.5$), HfO_2 ($\epsilon_{ox} = 21$), and La_2O_3 ($\epsilon_{ox} = 27$). Electron affinity of $\chi_{Si} = 4.17\,eV$ and silicon bandgap of $E_g = 1.1\,eV$ are used.

3 Model for gate threshold voltage (V_{TG}) of DMDG TFET

3.1 Tunnel FET V_{TG}

DMDG TFETs have outstanding I_D–V_{GS} characteristics, which are controlled by the width of the energy barrier. Figure 3 depicts how the energy barrier narrowing is controlled by the applied gate voltage in DMDG TFETs. Here, values of barrier width have been extracted by taking the energy bands across the length of the TFET and then measuring the narrowest barrier width for these bands. This technique works well at applied voltages above several hundred mV, due to the exponential dependence of the tunneling probability on the barrier width. This can be realized from Fig. 4, which shows the dependence of the drain tunneling current on the barrier width.

For MOS transistors, the physical definition of the threshold voltage is the gate voltage at which the density of carriers in the inversion channel at the surface equals the doping level of the substrate. Since the current conduction mechanism is completely different in TFETs, many previous works [22,23] used a constant-current method for extraction of the

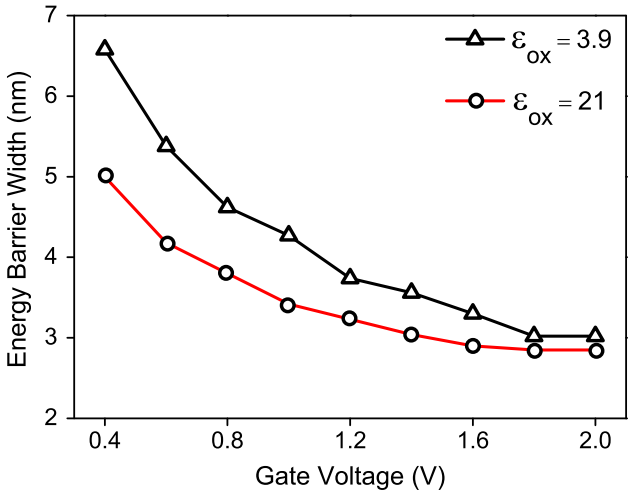

Fig. 3 Energy barrier width versus V_{GS} for $\epsilon_{ox} = 3.9, 21$ at $V_{DS} = 1$ V

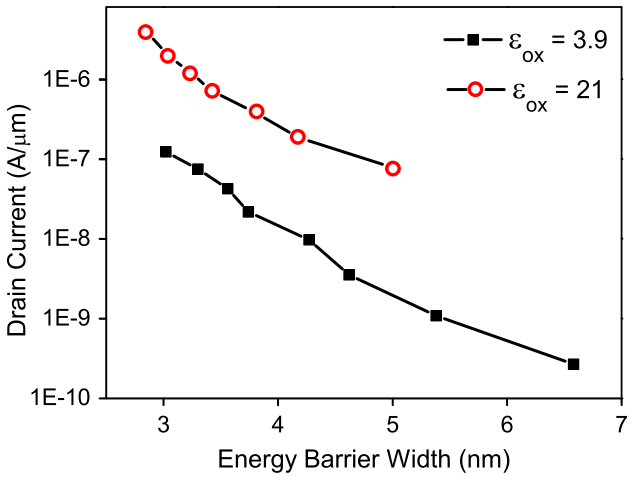

Fig. 4 Drain current versus energy barrier width for $\epsilon_{ox} = 3.9, 21$ at $V_{DS} = 1$ V

threshold voltage. In this method, the gate voltage at which the drain current equals 10^{-7} A/μm represents the threshold value. From Fig. 4, the constant-current method would suggest that the threshold voltage for the device in Fig. 1 corresponds to a barrier width of 4.5 nm, which is in the region of strong dependence of barrier width on gate bias. Since the constant-current method has no physical meaning, Boucart and Ionescu [24] proposed a new physical definition of the TFET threshold voltage (V_{TG}) as the gate voltage for which the energy barrier narrowing starts to saturate with gate bias. Herein, this new definition is used to extract the DMDG TFET threshold voltage.

3.2 Model derivation

Assuming a Gaussian box in the lightly doped body region of the DMDG TFET structure of Fig. 1 and neglecting mobile-charge, source–drain depletion regions, the following equation can be derived [25]:

$$\frac{\epsilon_{Si} t_{Si}}{\eta} \frac{\partial E_{sf(i)}(y)}{\partial y} + \epsilon_{ox} \frac{V'_{GS(i)} - \psi_{sf(i)}(y)}{t_{ox}} + \epsilon_{ox} \frac{V'_{GS(i)} - \psi_{sb(i)}(y)}{t_{ox}} = q N_{channel} t_{Si}, \quad (1)$$

where $i = 1, 2$ indicates regions under metal 1 and metal 2, respectively. $E_{sf(i)}(y)$ and $\psi_{sf(i)}(y)$ are the electric field and potential at the top oxide–semiconductor interface, respectively. η is the channel spreading parameter which accounts for the nonuniformity of the lateral field across the channel thickness. η is constant for a given technology, varying between 1 and 1.3 [25]. In this work, η is considered to be 1. $V'_{GS(i)} = V_{GS(i)} - V_{FB(i)}$, where the flatband voltage is $V_{FB(i)} = \phi_{m(i)} - \phi_S$. Here, $\phi_{m(i)}$ is the metal work function, and the semiconductor work function is $\phi_S = \chi_{Si} + E_g/2$.

In (1), the first term on the left-hand side represents the net lateral electric flux entering the Gaussian box, while the second and third term represent the fluxes entering from the top and bottom surface. The right-hand side is the total charge in the Gaussian box. Now, solving the one-dimensional (1-D) Poisson's equation in the x-direction of Fig. 1, the bottom interface potential, $\psi_{sb}(y)$, can be found.

$$\psi_{sb(i)}(y) = \psi_{sf(i)}(y) - E_{sf(i)}(y) t_{Si} - \frac{q N_{channel} t_{Si}^2}{\epsilon_{Si}}. \quad (2)$$

We then apply the continuity condition for the electric displacement vector at the top oxide–semiconductor interface:

$$E_{sf(i)}(y) = \epsilon_{ox} \frac{V'_{GS(i)} - \psi_{sf(i)}(y)}{t_{ox} \epsilon_{Si}}. \quad (3)$$

Substituting Eqs. (2) and (3) into (1) yields

$$\frac{\partial^2 \psi_{sf(i)}(y)}{\partial y^2} - \lambda^2 \psi_{sf(i)}(y) = \delta_{(i)}, \quad (4)$$

where

$$\lambda^2 = \eta \frac{C_{ox}}{t_{Si}^2 C_{Si}} \left(2 + \frac{C_{ox}}{C_{Si}}\right),$$

$$\delta_{(i)} = \eta \frac{q N_{channel}}{2\epsilon_{Si}} \left(2 + \frac{C_{ox}}{C_{Si}}\right) - \lambda^2 V'_{GS(i)}.$$

Here, the oxide capacitance is $C_{ox} = \epsilon_{ox}/t_{ox}$, and the silicon film capacitance is $C_{Si} = \epsilon_{Si}/t_{Si}$.

The solution of (4) for both channel regions under M1 and M2 is

$$\psi_{sf1}(y) = A\exp(\lambda y) + B\exp(-\lambda y) - \frac{\delta_1}{\lambda^2}, \quad 0 \le y \le L_1, \tag{5}$$

$$\psi_{sf2}(y) = C\exp(\lambda y) + D\exp(-\lambda y) - \frac{\delta_2}{\lambda^2}, \quad L_1 \le y \le L_2. \tag{6}$$

Now, to find the values of A, B, C, and D, the following boundary conditions are applied at the source edge, drain edge of the channel, and the point where M1 and M2 contact each other:

$$\psi_{sf1}(0) = -\frac{kT}{q}\ln\frac{N_{source}}{N_{channel}} = -V_{bi},$$
$$\psi_{sf2}(L) = \frac{kT}{q}\ln\frac{N_{drain}}{N_{channel}} + V_{DS} = V'_{bi} + V_{DS},$$
$$\psi_{sf1}(L_1) = \psi_{sf2}(L_1),$$
$$\frac{\partial\psi_{sf1}(L_1)}{\partial y} = \frac{\partial\psi_{sf2}(L_1)}{\partial y}.$$

Using these boundary conditions, the constants in (5) and (6) are obtained as

$$A = \frac{\gamma\exp(-\lambda L) + \theta}{2\sinh(\lambda L)} + \frac{\Delta V_{FB}\exp(-\lambda L_1)}{2},$$
$$B = \frac{-\gamma\exp(\lambda L) - \theta}{2\sinh(\lambda L)} + \frac{\Delta V_{FB}\exp(\lambda L_1)}{2},$$
$$C = \frac{\gamma\exp(-\lambda L) + \theta}{2\sinh(\lambda L)},$$
$$D = \frac{-\gamma\exp(\lambda L) - \theta}{2\sinh(\lambda L)},$$

where $\Delta V_{FB} = V_{FB1} - V_{FB2}$, $\sigma_1 = \frac{\delta_1}{\lambda^2}$, $\sigma_2 = \frac{\delta_2}{\lambda^2}$, $\theta = V'_{bi} + V_{DS} + \sigma_2$, and $\gamma = V_{bi} - \sigma_1 + \Delta V_{FB}\cosh(\lambda L_1)$. At the gate threshold voltage, the tunneling barrier width (w_b) exhibits a transition from strong to weak dependence on the gate voltage. At this inflection point, $y = w_b$ and $\psi_{sf1}(y) = V_{DS} + \frac{kT}{q}\ln\frac{N_{drain}}{N_{channel}}$ [26].

Substituting these values into (5), the threshold voltage of the DMDG TFET can be modeled as

$$V_{TG} = \frac{qN_{channel}t_{Si}}{2C_{ox}} + \frac{(\alpha-1)(V'_{bi}+V_{DS}) - \beta V_{bi}}{\alpha+\beta-1} + \frac{(\delta+\beta-1)V_{FB1} + (\alpha-\delta)V_{FB2}}{\alpha+\beta-1}, \tag{7}$$

where

$$\alpha = \frac{\sinh(\lambda w_b)}{\sinh(\lambda L)},$$
$$\beta = \exp(-\lambda w_b) - \alpha\exp(-\lambda L),$$
$$\delta = \alpha\exp(-\lambda L)\cosh(\lambda L_1) + \exp(-\lambda L_1)\sinh(\lambda w_b).$$

4 Results and discussion

The model was tested against simulation results for different parameter values. The n-type DMDG TFET investigated here has been simulated with Silvaco Atlas [27]. In all simulations, junctions were quasiperfectly abrupt. The models used were concentration-dependent mobility, electric-field-dependent mobility, Shockley–Read–Hall (SRH) recombination, concentration-dependent SRH lifetime, Auger recombination, bandgap narrowing, and Kane's band-to-band tunneling. In the simulation, the transconductance change (TC) method was used to derive V_{TG}. In this method, V_{TG} is the gate voltage corresponding to the maximum of the transconductance derivative, dg_m/dV_{GS}. In Fig. 5a, the drain currents for different gate dielectrics are plotted. Figure 5b shows the value (g_m) and first (dg_m/dV_{GS}) and second derivatives (d^2g_m/dV_{GS}^2) of the drain current for HfO_2 at $V_{DS} = 1$ V. At $V_{GS} = 1.15$ V, an inflection point in the g_m curve and a

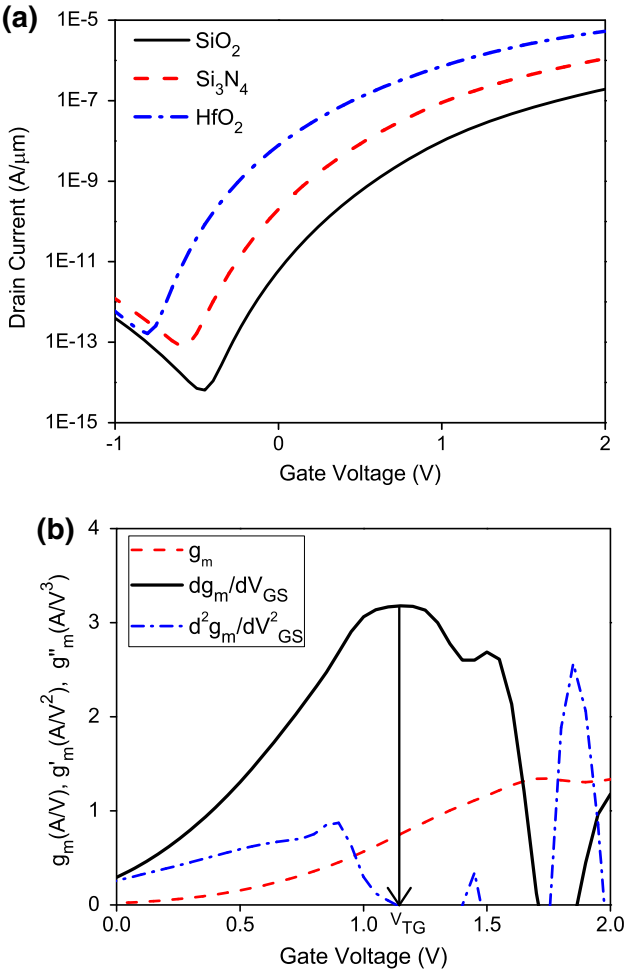

Fig. 5 **a** I_D–V_{GS} (log scale) for different gate dielectrics. **b** V_{TG} extraction for HfO_2 using TC method. Given scaled values of g_m, dg_m/dV_{GS}, d^2g_m/dV_{GS}^2. $V_{DS} = 1$ V

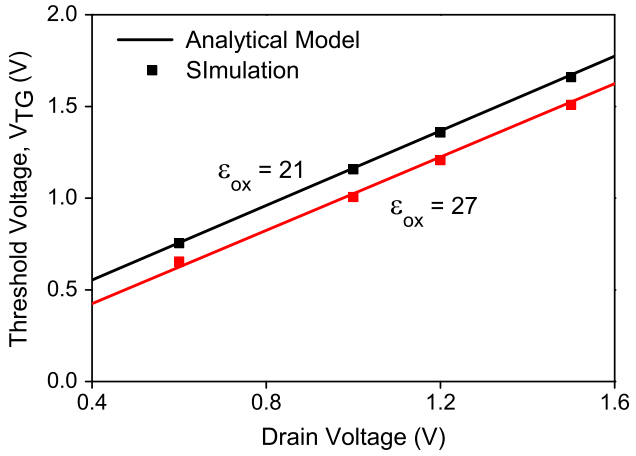

Fig. 6 V_{TG} versus V_{DS} for $\epsilon_{ox} = 21, 27$

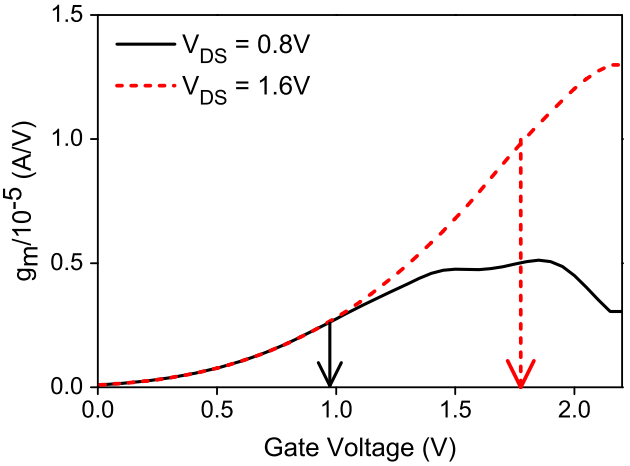

Fig. 7 g_m versus V_{GS}. *Points* marked correspond to maximum of dg_m/dV_{GS}. $\epsilon_{ox} = 21$

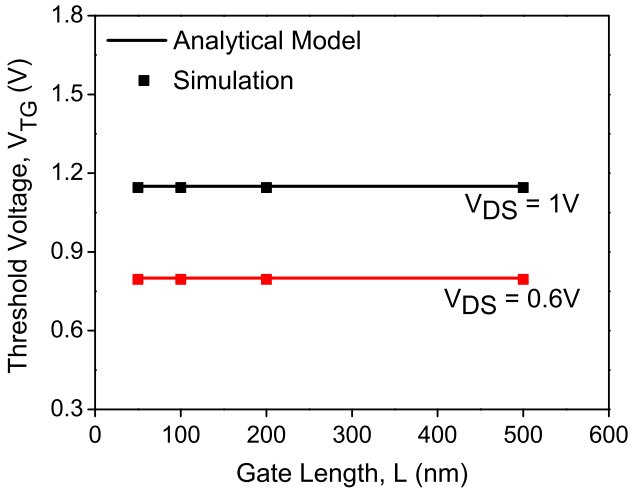

Fig. 8 V_{TG} versus L for $V_{DS} = 0.6, 1$ V. $\epsilon_{ox} = 21$

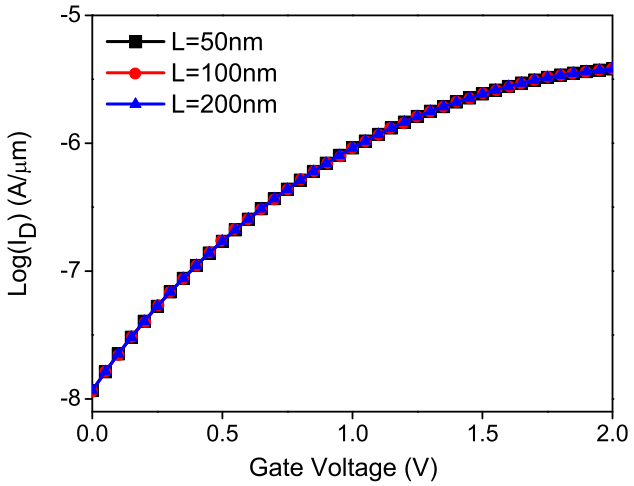

Fig. 9 I_D–V_{GS} curves for different gate lengths. $\epsilon_{ox} = 21$

peak in the dg_m/dV_{GS} curve occur, representing the transition point between quasiexponential and linear dependence of I_D on V_{GS}. The extracted V_{TG} is 1.15 V, much higher than the value obtained from the constant-current method.

Figure 6 plots the variation of V_{TG} with the applied drain bias for two high-k dielectrics with $\epsilon_{ox} = 21, 27$. It can be seen that the model shows good agreement with the simulation results. V_{TG} is higher for higher V_{DS}. The reason for this can be understood from Fig. 7, which shows that, for higher drain voltage, the gate retains quasiexponential control of the current over a larger voltage range. The effect of length scaling on V_{TG} is investigated in Fig. 8. It is found that V_{TG} is independent of device length. This is due to the limiting effect of gate length on V_{TG}, as depicted in Fig. 9. The conduction mechanism in the TFET is completely different from that in a MOSFET. The maximum electric field is always at the source–body junction, and is independent of the device length. The proposed model is able to describe this effect also.

V_{TG} increases when the Si layer thickness is increased, as presented in Fig. 10. The DMDG TFET is sensitive to the body thickness; this can be understood from the shape of the I_D–V_{GS} curve, as shown in Fig. 11. As the film becomes thinner, the electric field lines change. In turn, this increases the gate control of the barrier width in the tunnel junction, which results in a decreased V_{TG}. Figure 12 shows that use of high-k dielectric lowers V_{TG}. This is due to the fact that high-k dielectric aids the gate to have better capacitive control over the barrier width at the tunnel junction. The proposed model can predict this effect too.

Inversion charge was not included in the model derivation. The inversion voltage V_{inv} in a TFET can be calculated using the method described in [28]. The same approach was used here for a DMDG TFET to calculate the inversion voltage, as shown in Fig. 13. For the DMDG structure with HfO_2 gate dielectric, the numerical simulation shows that, at $V_{DS} = 1$ V, inversion occurs at 1.2 V, while Fig. 3 shows

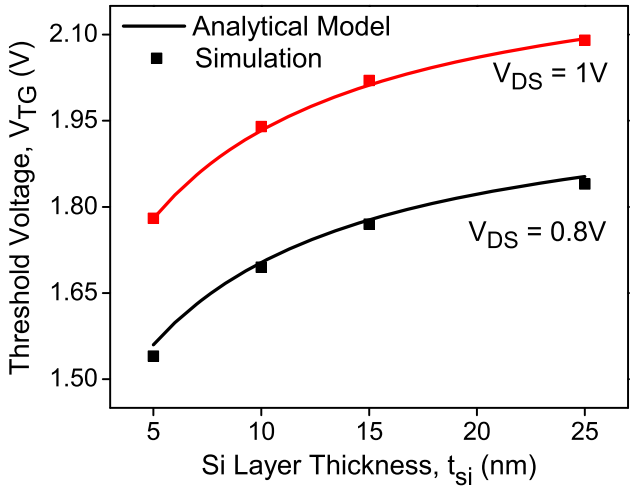

Fig. 10 V_{TG} versus t_{Si} for $V_{DS} = 0.8, 1$ V. $\epsilon_{ox} = 7.5$

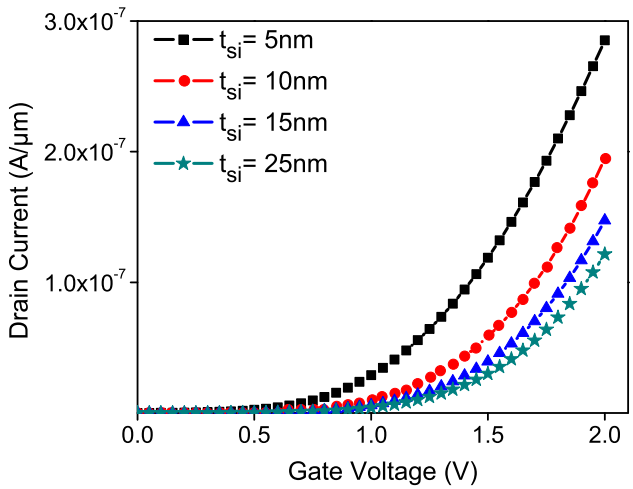

Fig. 11 I_D–V_{GS} curves (linear scale) for different Si layer thicknesses. $\epsilon_{ox} = 3.9$, $L = 50$ nm

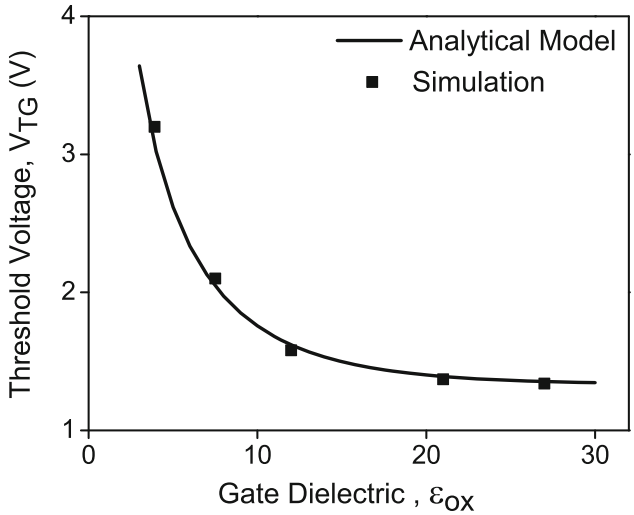

Fig. 12 V_{TG} versus ϵ_{ox}. $V_{DS} = 1$ V

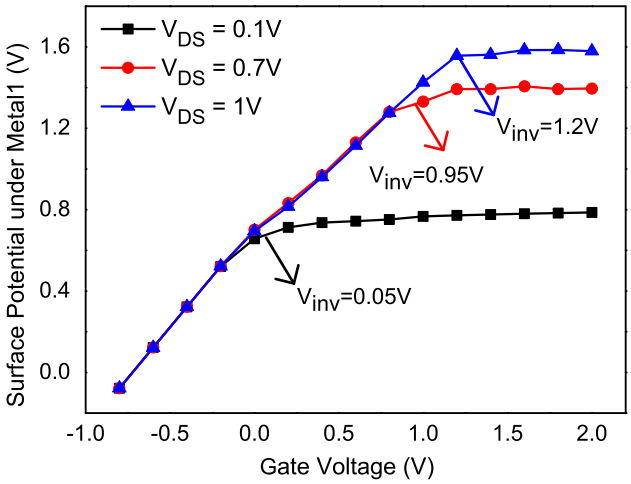

Fig. 13 Surface potential versus V_{GS}

that $V_{TG} = 1.14$ V. Similarly, at $V_{DS} = 0.7$ V, $V_{inv} = 0.95$ V while $V_{TG} = 0.9$ V. Since inversion occurs after the threshold point, the effect of inversion charge is negligible. Another fact to mention is that, when the source doping is very high, the band profile of a TFET resembles that of a MOSFET [29,30]. In this case, the conditions for deriving the threshold voltage from the surface potential will change. Therefore, this model might not predict the threshold voltage accurately in such cases.

5 Conclusions

A model for the gate threshold voltage of a DMDG TFET has been developed based on its physical definition. A numerical simulation study was carried out to verify the proposed model. The transconductance change method was employed to extract V_{TG} from the simulation. Model results are consistent with simulation results for different drain biases and varying device physical parameters. The effect of scaling of gate length and Si layer thickness on V_{TG} can be well predicted by the model. The proposed model shows improved device performance in terms of threshold voltage when high-k dielectric is used. Since the threshold voltage is one of the most significant parameters of a device, this model will be useful for further investigation of device performance.

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