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A modified macro model approach for SPICE based simulation of single electron transistor

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Abstract A new macro model of single electron transistor (SET) for SPICE based simulation of SET circuits is proposed. Two voltage controlled current sources and some scaling factors are incorporated in the existing model to derive our model. The V–I characteristics of the proposed SET is promising enough to be used as the basic element for designing circuits based on SETs. A comparison with the previous models establishes the fact that our model efficiently removes the drawbacks of the existing models. Our model also agrees well with the results obtained from popular SIMON simulator. To verify the accuracy, we have designed a SET inverter cell and investigated its characteristics. The work includes the effect of the parameters on the noise margin and voltage transfer characteristics of the inverter circuit. Further, to verify the applicability, a multi peak negative differential resistance circuit based on the proposed model is designed and simulated.

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Keywords Single electron transistor (SET) · Macro model · Tanner spice · Inverter · Noise margin · Multi peak negative differential resistance (NDR) circuit

1 Introduction

With the rapid advancement of the nano-scale fabrication, the single electron transistor (SET) [1,2] has become one of the most attractive and promising nano device due to its small size, low power consumption and sensitive charge measurement property [3–5]. SETs are being used and proposed as promising devices for quantum systems, including quantum computers and quantum dots and also as logic elements [6–9]. The main principles behind the operation of SETs are tunneling effect and Coulomb blockade oscillation [10,11].

SETs show completely different electrical characteristics from MOS transistors and basically based on few electron transport. In recent times, maximum attention has been given in design and simulation of SET-based circuits [12–16]. To understand the characteristics of SET based circuits and to explore its applications, simulation and device modeling of this device has become very important. Mainly three different approaches are used for simulation of SET: Macro-modeling, Monte-Carlo method and analytical modeling. The Monte Carlo approach is based on probability calculation of the tunnel events for all the Coulomb islands. This is a tedious job to perform and takes lot of time [17]. SETs have some serious drawbacks which can be overcome by the co-design of MOSFET and SET. Several works have been reported in the literature on hybrid SET-MOS based circuit design [18–24]. SET-MOS hybrid circuits cannot be simulated in Monte Carlo based simulators like SIMON, but with macro model approach hybrid circuits can be easily simulated in SPICE.

Other than macro model, several other approaches have also been reported in literature, which are based on master equation method [25–27]. In the master equation method, a set of equations is solved to obtain the characteristics curves of single electron transistor. In this approach, to obtain an accurate result one needs to consider a large number of states. This increases the complexity of the process and also the computation time [11]. A macro model can be defined as an equivalent circuit of a particular device, designed using basic microelectronics components like voltage and current sources, diodes and resistors. In macro modeling approach, we solely concentrate on solving KCL and KVL equations rather than calculating the probability of tunnel events or solving a set of equations. Therefore, the computation time of this approach is much lesser compared to other approaches. For circuits with a small number of tunnel junctions, the master equation method is much faster compared to Monte Carlo method. In case of large circuits, the master equation method is not feasible and the macro model approach is faster compared to the other two approaches. Single electronic circuits based on macro model approach can be easily simulated using SPICE. In this approach, a SET is replaced by its equivalent electrical circuit called the macro model. For simulation of multiple SET-based circuits, we just have to call the corresponding macro model or the sub circuit. There are two main assumptions for macro modeling: (1) after determining the parameters of SET equivalent model, it can be used in a whole circuit, and (2) the I–V characteristic of the SET is influenced by neighbouring transistors only through the changes of terminal voltages [28]. The macro model proposed by Yu et al [29] is based on parameter based modeling and line fitting. In the V–I characteristic curves of Yu's model, it is observed that the I_{ds}–V_{ds} curves are not parallel to each other. Wu and Lin later modified the model to make the current flowing from gate to source negligibly small [29]. Karimian et al further modified it to calculate the timing of electron tunneling through the barrier by employing a switch capacitor circuit in the model [30]. Recently we proposed a macro model [31], which removes the drawbacks of the existing models and works as an ideal single electron transistor. However, none of the models reported above have yielded the expected characteristics of practical SETs, since there are still some drawbacks with these models. Therefore, in this work, we have modified our previous model to make it more accurate and practical, by employing two voltage controlled current sources in Yu's model. Also, to reduce the complexity the number of design parameters has been reduced compared to our previous model. The V–I characteristics of the proposed SET is thoroughly studied to verify its applicability for designing single electronics circuits. The simulation results are compared with previously reported models. To confirm the validity of the model, different benchmarked circuits have been designed using the proposed model and their characteristics are thoroughly investigated.

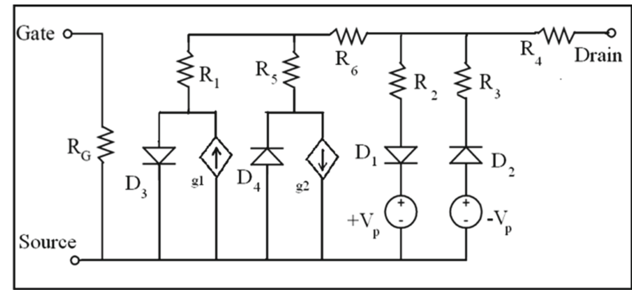

Fig. 1 The proposed macro model of SET with two voltage controlled current sources g1 and g2. Resistors R2, R3 along with diodes D1and D2 work for the non-Coulomb part of the characteristics. R1, D3, g1and R5, D4, g2 are included to generate the Coulomb blockade part of the characteristics

2 Design and analysis of the proposed model

The proposed macro model of SET is shown in Fig. 1. The V–I characteristics of SETs can be divided into two parts; the Coulomb blockade and non-Coulomb blockade parts. The non-Coulomb blockade part of the characteristics which shows symmetric nature of the drain current as a function of V_{ds} has been incorporated in our model by using two branches of circuit elements consisting of diodes (D1,D2), resistors (R2,R3) and voltage source V_p. Here, D2, R3, $-V_p$ and D1, R2, $+V_p$ are responsible for the positive and negative parts of the characteristics curve, respectively. When the value of the critical voltage is greater than V_p, diode D1 is ON and current flows through R2. If the critical voltage is less than the $-V_p$, diode D2 is ON and current flows through the resistor R3. Two more branches consisting of R1, D3, g1 and R5, D4, g2 have been used to generate the Coulomb blockade part of the characteristics. In the positive part of the Coulomb blockade characteristics, current flows through R5 and g2 bypassing D4, and a very small current also flows through R1 and D3. In the negative part of the Coulomb blockade characteristics, current flows through R1 and g1 bypassing D3 and a very small current also flows through R5 and D4. RG is used in the circuit to isolate the gate terminal from the source terminal by restricting the current flowing through it. Also the value of RG has been chosen much higher compared to other resistor values so that it acts like an open circuit. From designer point of view, R6 has no significance, it only helps in plotting the overall drain current. We have used two voltage controlled current sources (g1 and g2) which are functions of gate to source voltage. The voltage source V_p has been used for defining the range of Coulomb blockade region. The values of resistors R1, R5, R2 and R3 (written as RR1, RR5, RR2 and RR3) can be expressed as [28]

$$RR1 = RR5 = CR1 + CR2 \times \cos\left(CF1 \times \pi \times Vgs\right) \tag{1}$$

$$RR2 = RR3 = \frac{CV_p}{CI2 - \frac{2CV_p}{\left(2\times CR1 + CR2\times\cos\left(CF1\times\pi\times Vgs\right)\right)}} \tag{2}$$

The parameters CF1, CV_p, CI2, CR1 and CR2 are used to fit the I–V characteristics curve at various gate biases. CF1, which determines the frequency of Coulomb oscillation in I_{ds}–V_{gs} characteristics curve, can be expressed as [28]

$$CF1 = \frac{2C_g}{e} \tag{3}$$

In a SET, the gate to source voltage is responsible for shifting the Id-Vds curve vertically, keeping the nature of the curve intact. Taking this factor into account, the novel components, g1 and g2, are expressed as

$$g1 = g2 = \left(\left(\frac{1}{k1 \times CR1}\right) \times \sin\left(\pi \times VGs\right)\right) \times k2 \tag{4}$$

Initially the basic structure of the equation is obtained using curve fitting technique. Though the values of other parameters cannot be calculated directly, we can get an approximate range through the nomenclature of these parameters. CVp, as the name implies is a peak voltage value which represents the maximum range of the Coulomb blockade region. CI2 is related to the current in nano range. CR1 and CR2 are related to the tunnel junction resistance which should be in mega range. Initially, the values for these parameters are taken from Ref. [28] and thereafter different parameter values are obtained using parametric analysis of the designed model. According to the orthodox theory of single electron tunneling, the Coulomb energy or the charging energy must be bigger than the thermal energy [20], and it can be expressed as

$$E_c = \frac{e^2}{2C} >> K_B T \tag{5}$$

where, E_C is the Coulomb energy, K_B is the Boltzmann constant and T is the operating temperature in Kelvin. C is the total capacitance of the island and is calculated as

$$C = C_g + 2C_j \tag{6}$$

Here C_g and C_j are the gate capacitance and junction capacitance respectively. If the thermal energy becomes greater than the charging energy, electron tunneling occurs due to thermal fluctuations in energy thereby causing instability of the circuit. From (5), it can be observed that the charging energy is totally dependent on the overall capacitance of the respective island, and the maximum operating temperature is inversely proportional to the total capacitance of the island. The sub circuit code for the proposed macro model circuit, which also includes the parameter declaration of the model, is given in Fig. 2.

```
.SUBCKT set 8 2 3
.param
+pi=3.14
+CF1=40
+CI2=0.2e-9
+CR1=300e+6
+CR2=100e+6
+CVp=0.02
V2 5 3 DC 0.02
V3 7 3 DC -0.02
RG 2 3 100G
RR1 13 9 R='(CR1+CR2*cos (CF1*pi*V (2, 3)))'
RR6 1 13 1
RR5 13 10 R='(CR1+CR2*cos (CF1*pi*V (2, 3)))'
RR2 1 4  R='(CVp/(CI2-2*CVp/(2*CR1+CR2*cos(CF1*pi*V(2, 3)))))'
RR3 1 6 R='(CVp/ (CI2-2*CVp/(2*CR1+CR2*cos(CF1*pi*V(2, 3)))))'
RR4 1 8 1
D1 4 5 DIODE
D2 7 6 DIODE
D3 9 3 DIODE
D4 3 10 DIODE
MODEL DIODE D (N=0.01)
g1 9 3 cur='((1/ (k1*CR1))*sin (pi*V (2, 3)))*k2'
g2 10 3 cur='((1/ (k1*CR1))*sin (pi*V (2, 3)))*k2'
.ends
```

Fig. 2 Sub circuit code of the proposed macro model

In the code, CF1, CI2, CR1, CR2, CR3, CR4, and CVp are macro model parameters; K_1 and K_2 are scaling factors. The components g1 and g2 represent two voltage control current sources which are the main design component of the design. Assuming the value of CF1 as 40 [28], the value of C_g is calculated as 3.2 aF. Again from (4), it is seen that C_g directly controls the operating temperature of the SET. So, a temperature controlling parameter is incorporated in the proposed sub circuit code, by including CF1. The code shows the dependency of the two current sources, g1 and g2, on the gate to source voltage. k1 and k2 are scaling factors for adjusting the slope of the I–V graphs .

3 Simulation results

The code is executed in Tanner SPICE environment using the following parameters: Cg = 3.2 aF, Cj = 1.6 aF, T = 30 K [28]. The values for the fitting parameters are chosen as CF1 = 40, CVp = 0.02, CI2 $= 0.2 \times 10^{-9}$, CR1 $= 300 \times 10^{+6}$ and CR2 $= 220 \times 10^{+6}$. The variation of drain current (I_{ds}) with V_{gs}, considering V_{ds} as a parameter is

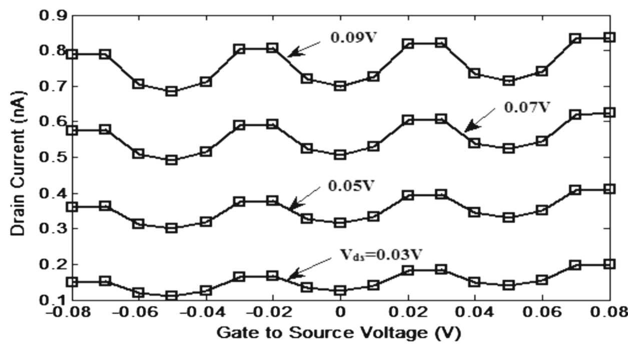

Fig. 3 Coulomb oscillation characteristics of the proposed macro-model for different values of gate to source voltage

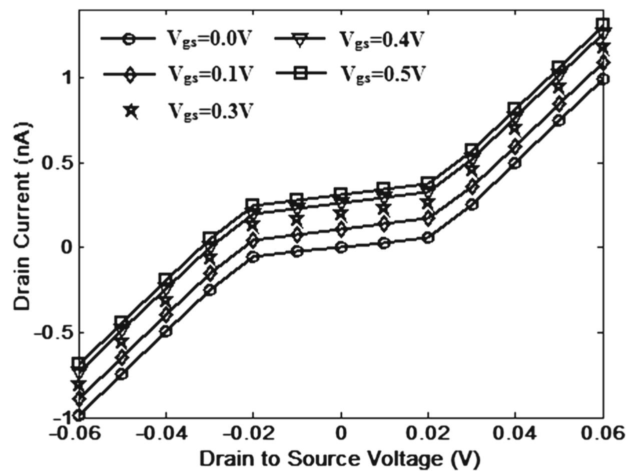

Fig. 4 V–I characteristics of the proposed macro-model for different gate biases. Here Vgs is varied from 0.0 to 0.5 V with an increment of 0.1 V

shown in Fig. 3. It can be observed that drain current oscillates periodically for a constant value of V_{ds}. This characteristic is known as the Coulomb blockade oscillation or single electron current oscillation which is considered as one of the most important property of SET.

The I_{ds}–V_{ds} characteristics plotted using our proposed modified macro-model is shown in Fig. 4. From the characteristics curve, the Coulomb blockade region can be identified for drain to source voltage range of −20 to 20 mV. The drain to source voltage on both side of the Coulomb blockade region represents the non-Coulomb blockade features. Ideally, the drain current is zero in the Coulomb blockade region but in reality, a very small amount of current flows due to tunneling of thermally activated carriers at small finite temperatures.

This justifies the small variation of the drain current in the Coulomb blockade region as visible in Fig. 4. With increase in Vgs the graph shifts along the Y-axis. This shift is also observed in case of Yu's model, but the nature of the shift was not fixed there. If we go on increasing V_{ds} beyond Coulomb

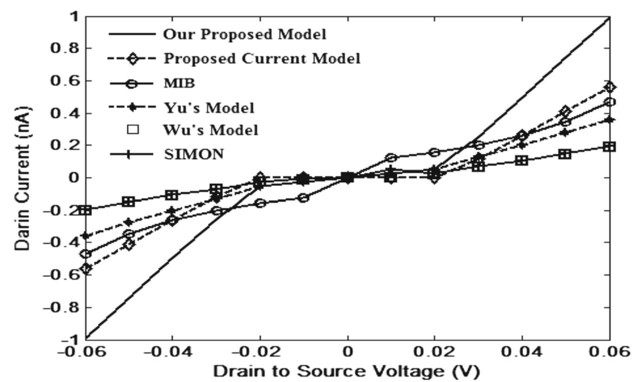

Fig. 5 Comparison of the I_{ds}–V_{ds} characteristics of the proposed model, for both Coulomb blockade and non-Coulomb blockade regions, with Yu's model, Wu and Lin's model, SIMON, MIB model and our previous model. The parameters for other models are $R_D = R_S = 100M\Omega$, $C_{TD} = C_{TS} = 1.6$ aF, and T = 30 K. The parameters for our macro model are CF1 = 40, $C_{VP} = 0.02$, CI2 $= 0.5 * 10^{-9}$, CR1 $= 300 * 10^{+6}$, CR2 $= 10 * 10^{+6}$. The value of RG is taken as $100*10^9$ Ω

blockade region, the number of electrons charging the island increases one-by-one. Since we have considered the junction to be symmetric, the current increases linearly outside the Coulomb blockade region.

The I_{ds}–V_{ds} characteristics of the proposed model, for both Coulomb blockade and non-Coulomb blockade regions, are compared with other models in Fig. 5. It can be observed that the simulation result of our model closely matches with that of popular simulation software SIMON. The values of the parameter taken as Rj = 100 MΩ, Cj = 3.2 aF and T = 30 K. CF1 = 40, $CV_P = 0.02$, CI2 $= 0.2 * 10^{-9}$, CR1 $= 300 * 10^{+6}$, CR2 $= 220 * 10^{+6}$ and $V_{gs} = 0$ V. It is also observed that the proposed model covers the maximum range of the drain current.

4 Single electron inverter

To check the validity of the proposed model, an inverter is designed using the proposed model as shown in Fig. 6. The transient response of the single electron inverter has been tested by applying an input pulse to its input. The output wave form is found to be an exact opposite replica of the input and it is shown in Fig. 7.

The variation of voltage transfer characteristics of the designed SET inverter for different values of RG is depicted in Fig. 8. The output voltage is found to increase with increasing value of RG. No significant changes are observed in the characteristic curve for RG above 100 GΩ, therefore we have restricted the value of RG to 100 GΩ. The voltage transfer characteristics with RG = 100 GΩ and $V_{dd} = 0.03$ V is shown separately in Fig. 9 to calculate the corresponding noise margins [high noise margin (NM_H) and low noise margin (NM_L)] [32]. We have further investigated the effect of

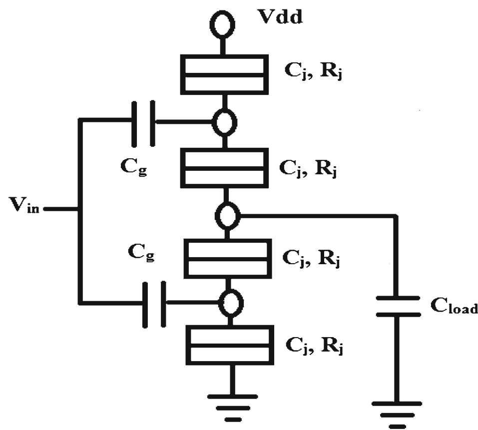

Fig. 6 Single electron transistor inverter cell with Cj and Rj are the tunnel junction capacitance and resistance respectively. Cload is the load capacitance

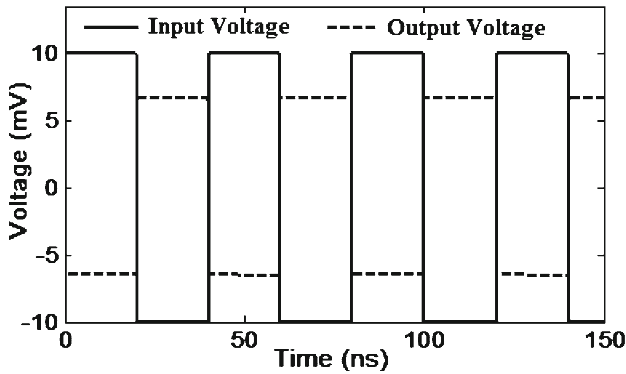

Fig. 7 Transient characteristic of the SET inverter circuit. Here *solid line* and *dashed line* represents input waveform and output waveform respectively. The parameters for the macro model is CF1 = 40, $CV_P = 0.02$, $CI2 = 0.2 * 10^{-9}$, $CR1 = 340 * 10^{+6}$, $CR2 = 100 * 10^{+6}$. The value of RG is taken as $100*10^9$ Ω

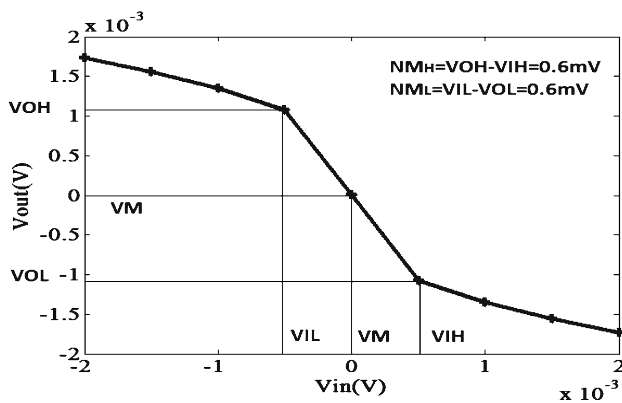

Fig. 8 Effect of RG on the voltage transfer characteristics of the inverter where the maximum value of the RG is considered as 100 GΩ

parameter RG on the noise margin of the inverter cell as it has the maximum effect on the SET logic robustness compare to other parameters.

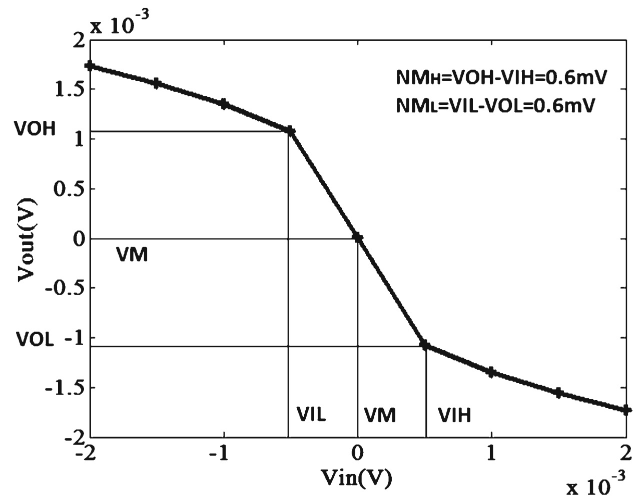

Fig. 9 Noise margin calculation from voltage transfer characteristics of inverter for RG = 100 GΩ

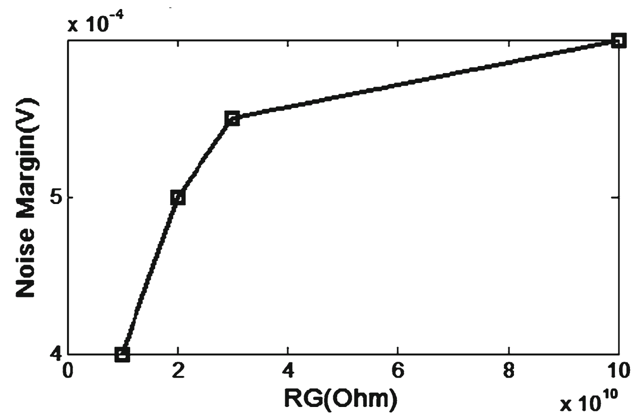

Fig. 10 Variation of noise margin for different values of RG

The variation of high/low noise margin with different values of RG can be obtained from Fig. 10. It can be seen from the plot that high/low noise margin improves with increasing values of RG up to 100 GΩ after which it gets saturated. By evaluating the overall performance, it can be said that the designed inverter shows sufficient accuracy in both static and dynamic regimes. The gain of the inverter cell for different input voltage has been given in Fig. 11. It is observed that, in the transition region the gain decreases rapidly in both side of the transition point, otherwise the gain remains almost constant.

5 Multiple peak NDR circuit

Ultra high speed and reducing circuit complexity are the two important properties of multi peak NDR circuits [33–35], which makes it suitable for designing multiple values

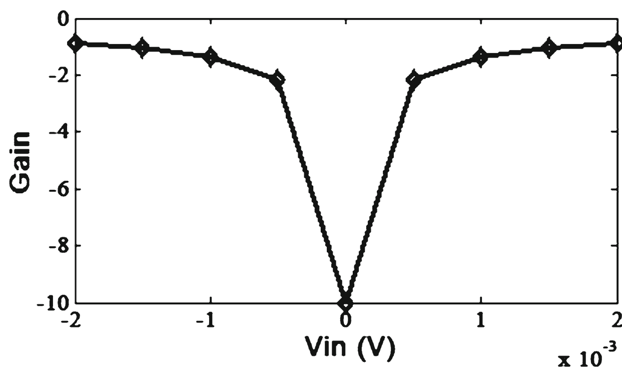

Fig. 11 Variation of gain with input voltage (V_{in}) for the proposed SET inverter cell

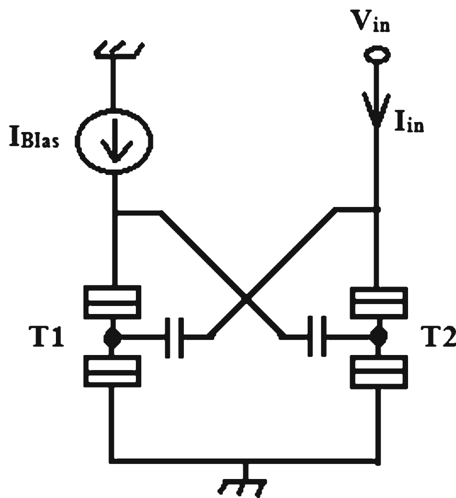

Fig. 12 Schematic diagram of the multi peak NDR circuit with two cross coupled single electron transistors and one current source used for biasing the transistor T1. The parameter values used are CF1 = 40, $CV_P = 0.02$, $CI2 = 0.2 * 10^{-9}$, $CR1 = 270 * 10^{+6}$, $CR2 = 70 * 10^{+6}$ (for T1) and $CR1 = 280*10^{+6}$, $CR2 = 280*10^{+6}$ (for T2). The value of RG is taken as $10*10^8\ \Omega$

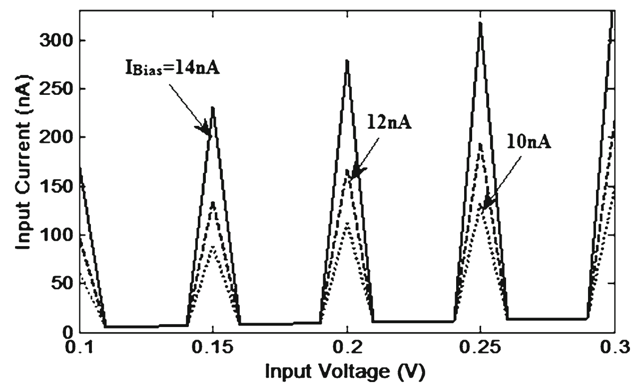

Fig. 13 Characteristics of the designed multi peak NDR circuit for different bias current simulated in SPICE environment. The parameter values used are CF1 = 40, $CV_P = 0.02$, $CI2 = 0.5*10^{-9}$, $CR1 = 270*10^{+6}$, $CR2 = 70*10^{+6}$ (for T1) and $CR1 = 280*10^{+6}$, $CR2 = 280*10^{+6}$ (for T2). The value of RG is taken as $10*10^8\ \Omega$

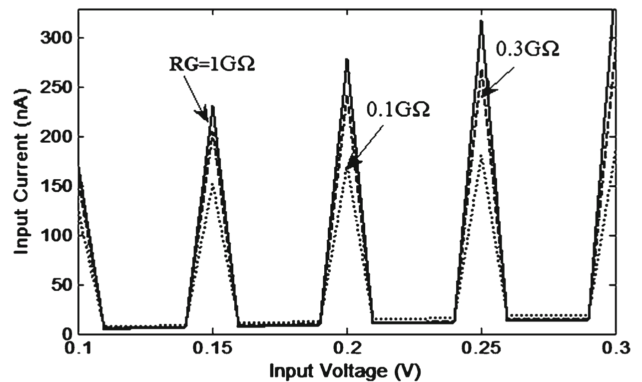

Fig. 14 Effect of Rg on the characteristics of the multi peak NDR circuit. The parameter values used are CF1 = 40, $CV_P = 0.02$, $CI2 = 0.5*10^{-9}$, $CR1 = 270*10^{+6}$, $CR2 = 70*10^{+6}$ (for T1) and $CR1 = 280*10^{+6}$, $CR2 = 280*10^{+6}$ (for T2). The value of the bias current is 14 nA

memory circuits, frequency multiplier and multiple valued logic circuits. We have designed a multi peak NDR circuit based on single electron transistor [7]. The designed circuit is consisting of two cross coupled SETs as shown in Fig. 12. The transistor T1 controls the current flowing through T2 by creating a feedback loop. Clear peaks are observed in the I–V characteristics of the designed circuit as depicted in Fig. 13. It can be noticed that the height of the peaks increases with increase in bias current. The further investigation is laid upon the effect of RG on the I–V characteristics of the designed multi peak NDR circuit as shown in Fig. 14. with increase in RG the height of the peaks are increasing and it has been observed that beyond 1 GΩ, the effect of RG starts diminishing and after 50 GΩ there is no effect at all.

6 Conclusion

An improved version of our previous macro model of SET suitable for SPICE based simulation of single electron circuits is proposed by incorporating two voltage controlled current sources and some scaling factors. The proposed model was simulated in SPICE environment. The simulation results clearly demonstrate the Coulomb blockade and Coulomb oscillation characteristic of the SET. It was found that our model overcomes the drawbacks of all existing models. Our model also agrees well with the results obtained from monte carlo based simulator SIMON. The proposed SET model is used to design an inverter cell. Simulation results of the inverter are promising enough to justify the validity of the proposed model for designing SET based circuits. The investigation about the effect of the parameters reveals that RG has maximum effect on the noise margin of the inverter cell and the noise margin gets affected by the values of the

RG up to 100 GΩ. The corresponding voltage transfer characteristic and noise margin plots are also shown to validate our proposal. Prominent peaks are observed in the simulation results of the designed multi peak NDR circuit. It is observed that with increase in bias current and RG the height of the peaks increases.

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