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Model for threshold voltage instability in top-gated nanocrystalline silicon thin film transistor

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Abstract The analytical model for the threshold voltage instability in top-gated staggered nanocrystalline silicon thin-film transistor is reported. This novel model includes the effect of various physical parameters like grain size, gate insulator thickness, doping density and grain boundary trapping state on the threshold voltage shift which is never reported earlier. It is observed that the higher trap density, greater doping concentration and larger gate insulator thickness provide lesser threshold voltage shift. Further, it is found from the results of grain size analysis that if grain size is smaller than threshold voltage shift decreases with decrease in grain size. However, if grain size is larger ($D_g > 20$ nm) then device become stable and shows negligible threshold voltage shift. In this paper, threshold voltage shift under gate bias voltage is also analyzed and result reveals that threshold voltage increases with the bias voltage. The calculated results are compared with experimental data. The close match between the two confirms the validity of proposed study.

Keywords Hydrogenated amorphous silicon (a-Si:H) · Nanocrystalline silicon (nc-Si) · Threshold-voltage (V_T) · Thin-film transistors (TFTs) · Threshold-voltage shift (ΔV_T)

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1 Introduction

Thin film technologies have already grown to a big industry which is centered on the new generation of displays such as organic light-emitting diode (OLED) and liquid crystal display (LCD). On this display panels, thin film transistor (TFT) basically controls the operation of each pixel forming the image. The hydrogenated amorphous silicon (a-Si:H) is widely used as an active layer in TFT. However the low temperature plasma enhanced chemical vapour deposition (PECVD) process used for a-Si:H deposition causes the formation of a-Si with low electron mobility [1]. In addition to low electron mobility, a-Si:H also suffers from drain current degradation under bias and illumination stress. This drain current degradation causes threshold voltage shift in a-Si:H TFT and therefore degrade the performance of display devices.

Nowadays, nanocrystalline silicon (nc-Si) has proven as the best alternative material over a-Si:H due to the advancement of deposition technique used for it. Hot wire chemical vapour deposition (HWCVD) technique is commonly used for the deposition of nc-Si which allows direct deposition of nc-Si over large area at low substrate temperature and high deposition rates (about 1 nm/s) [2]. Therefore it provides nc-Si with higher silicon crystallites as well as increased doping efficiency which led to the formation of nc-Si TFT with higher field effect mobility and better stability under bias stress as compared to a-Si:H TFT [3].

For the production of new generation large displays, an active matrix addressing scheme is required for display panels where pixels are located at row and column interactions in order to minimize capacitive losses in column and row lines. This addressing scheme basically consist of two TFTs per pixel, of which one is operated under continuous gate bias and hence requiring a high stability. Although various

researchers claimed that nc-Si TFTs have better stability than a-Si:H TFT however electrical instability mechanisms have not been deeply analyzed so far. In this paper, the novel analytical model which includes the effect of various physical parameters like grain size, gate insulator thickness, doping density and grain boundary trapping state on electrical instability of nc-Si TFT is proposed.

This paper consists of four sections. Section 1 explains the theory and model for developing the analytical model, Sect. 2 gives the result and discussion about the effect of various physical parameters and last section concludes the work presented in this paper.

2 Theory and model

The TFTs suffers from drain current degradation under bias stress due to two possible instability mechanisms, charge trapping in the gate dielectric and defect state creation in the active layer. Under electrical stress, the charge trapping take place in the gate insulator and/or in the interface between the gate insulator and channel material. Various proposed mechanisms responsible for the charge transfer from semiconductor to insulator are illustrated in Fig. 1 which includes (1) Direct tunneling from valence band [4,5], (2) Fowler–Nordheim injection [6,7], (3) trap assisted injection [8], (4) constant energy tunneling from silicon conduction band [9], (5) tunneling from conduction band to E_f (phonon assisted or via surface states) [10] and (6) hopping at the fermi level [11].

Another possible mechanism for electrical instability is defect state creation. When the electrical stress is applied on

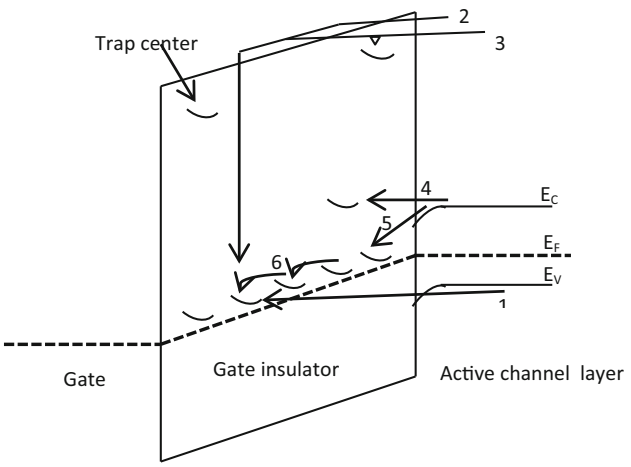

Fig. 1 Charge trapping mechanisms. *1* Direct tunneling from valence band, *2* Fowler–Nordheim injection, *3* trap assisted injection, *4* constant energy tunneling from silicon conduction band, *5* tunneling from conduction band to E_f (phonon assisted or via surface states), *6* hopping at the fermi level

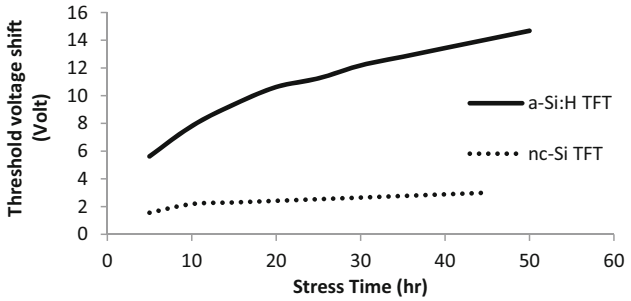

Fig. 2 Comparison between the threshold voltage shift in a-Si TFT and nc-Si TFT as a function of stress time at temperature 75 °C and stress current of 10 μA [12]

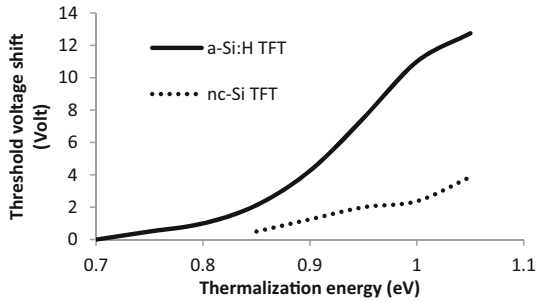

Fig. 3 Comparison between the threshold voltage shift in a-Si TFT and nc-Si TFT as a function of thermalization energy at temperature 75 °C and stress current 15 μA [12]

the TFTs then the density of electrons which take part in conduction increases in the active layer. These electrons interact with the weak Si-Si bond and cause the breaking of bonds which in turn leads to the formation of new dangling bonds in the channel layer due to which electrons gets frequently trapped into and released from defect states. This effectively increases the total density of defect states and decreases the drain current or increase the threshold voltage.

Limited work on the electrical instability of nc-Si:H TFT are published so far and most of these works focus on the gate bias stability. Esmaeili-Rad et al. [12] compared the threshold voltage shift of the nc-Si TFTs with that of the a-Si:H TFTs, under similar operation conditions and found two major differences in the behavior of nc-Si TFTs as compared to that of the a-Si:H TFTs, first one is the threshold voltage shift in nc-Si TFT saturates at prolonged stress times, but that of a-Si:H TFT does not as shown in Fig. 2 and second one is that threshold voltage shift in nc-Si TFT is weakly temperature dependent, as compared to that of a-Si:H device as shown in Fig. 3.This behavior of threshold voltage shift in nc-Si TFTs shows absence of defect state creation. The weak temperature dependence validate that the instability in nc-Si TFTs is due to the charge trapping mechanism proposed by Powell et al. [11]. The threshold voltage shift in nc-Si TFT thus also follows the stretched exponential time dependence [13,14]. Kim et al. [15] proposed that the nc-Si TFT shows less thresh-

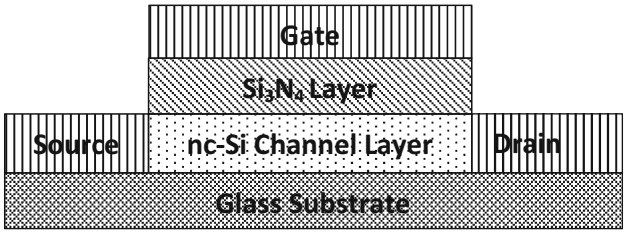

Fig. 4 Schematic view of top-gated nc-Si TFTs

old voltage shift as compared to a-Si TFTs. When the drain bias applied to the nc-Si TFT increases, the concentration of channel charge decreases and due to which less defect states are created and thus decreases the threshold voltage shift. In addition to this, they examined that in case of top gated nc-Si TFT, the defect state creation is much lower due to the presence of well-crystallize region of the nc-Si film. They also proposed that the ratio of depleted charges (Q_G) to the total charges (Q_{G0}) increases with the decreasing channel length. Since short channel TFT has lower concentration of channel charge thus it shows less threshold voltage degradation as compared to long channel TFT.

Figure 4 shows the schematic view of top-gated nc-Si TFT considered for the study. Since threshold voltage shift (ΔV_T) in nc-Si TFT follows the stretched exponential time dependence [13,14] which basically contains the parameter ΔV_{T0} where $\Delta V_{T0} = V_{gs} - V_T$, thus it is important to study how the threshold voltage (V_T) in nc-Si TFTs is affected by various other parameters like gate insulator thickness and grain boundary trapping states at different doping density and temperature.

The surface potential which under strong inversion can be given as

$$\varphi_{s(inv)} \approx 2\varphi_F \approx 2\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \tag{1}$$

In the above equation, φ_F is the Fermi potential, k is Boltzmann's constant, T is the temperature, N_a is the acceptor doping density (cm^{-3}) and n_i is the intrinsic charge density which is given as [16]

$$n_i = 2\left(\frac{2\pi kT}{h^2}\right)^{\frac{3}{2}}\left(m_n^* m_p^*\right)^{\frac{3}{4}} e^{-\frac{E_g}{2kT}} \tag{2}$$

where h is the Planck's constant, E_g is the bandgap energy (= 1.12eV) and m_n^* and m_p^* are the effective electrons and holes masses in nc-Si given as $m_n^* = 0.34m_o$ and $m_p^* = 0.55m_o$ [17].

The threshold voltage is given as

$$V_T = \varphi_s + V_i(inv) \tag{3}$$

where $V_i(inv)$ is the voltage across the insulator and is simply equal to $t_i E_i$ i.e.

$$V_i(inv) = t_i E_i \tag{4}$$

where t_i is the insulator thickness and E_i is the gate insulator electric field and can be calculated by using the equation given as

$$E_i = \frac{\varepsilon_{nc-Si}}{\varepsilon_i} E_S \tag{5}$$

where ε_i is the dielectric constant of insulating layer, E_S is the surface electric field and ε_{nc-Si} is the dielectric constant of nc-Si channel layer which can be determined as [17]:

$$\varepsilon_{nc-Si} = 1 + \frac{10.4}{1 + \left(\frac{1.38}{D_g \times 10^7}\right)^{1.37}} \tag{6}$$

where D_g is the average grain size in cm

The surface electric field E_s in Eq. (5) can be calculated by using one dimensional Poisson's equation along the direction perpendicular to the gate insulator and nc-Si channel layer interface of the TFT given as

$$\frac{\partial^2 \varphi}{\partial x^2} = -\frac{\rho}{\varepsilon_{nc-Si}} \tag{7}$$

where φ is the electrostatic potential, ρ is the density of trapping states N_t ($cm^{-3}eV^{-1}$) in channel layer and can be given as

$$\rho = -q^2 N_t \varphi \tag{8}$$

Poisson's equation (Eq. 7) can be written in the form of electric field E as

$$E\frac{\partial E}{\partial \varphi} = q^2 N_t \frac{\varphi}{\varepsilon_{nc-Si}} \tag{9}$$

Integrating Eq. (9) from bulk towards the surface can provide the surface electric field E_s as

$$E_s = q\varphi_s\sqrt{\frac{N_t}{\varepsilon_{nc-Si}}} \tag{10}$$

At threshold, the gate insulator electric field can be determined by using Eqs. (5), (6) and (10) as

$$E_i(inv) = \frac{q\varphi_s}{\varepsilon_i}\sqrt{N_t \times \left[1 + \frac{10.4}{1 + \left(\frac{1.38}{D_g \times 10^7}\right)^{1.37}}\right]} \tag{11}$$

Therefore from Eqs. (3), (4) and (11), the threshold voltage becomes

$$V_T = \varphi_s \left[1 + \frac{q t_i \sqrt{N_t}}{\varepsilon_i} \sqrt{1 + \frac{10.4}{1 + \left(\frac{1.38}{D_g \times 10^7} \right)^{1.37}}} \right] \tag{12}$$

The stretched exponential equation for threshold voltage shift calculation is given as [13]

$$|\Delta V_T| = \left(V_{gs} - V_T \right) \left\{ 1 - \exp \left[- \left(\frac{t}{\tau} \right)^{\beta} \right] \right\} \tag{13}$$

From Eqs. (12) and (13), the final expression for threshold voltage shift is given as:

$$|\Delta V_T| = \left(V_{gs} - \varphi_s \left[1 + \frac{q t_i \sqrt{N_t}}{\varepsilon_i} \sqrt{1 + \frac{10.4}{1 + \left(\frac{1.38}{D_g \times 10^7} \right)^{1.37}}} \right] \right) \left\{ 1 - \exp \left[- \left(\frac{t}{\tau} \right)^{\beta} \right] \right\} \tag{14}$$

3 Result and discussion

Table 1 shows the typical values of the model parameters used in the calculations.

Figure 5a illustrate the variation of calculated value for threshold voltage shift as a function of time for different values of trap density. It is observed that at a particular time the threshold volatge shift decreases with increase in trap density. This is attributed to the fact that the channel charge concentration reduces due to increase in trap states which in turn decreases the threshold voltage shift [15]. Similarly, Fig. 5b shows the effect of doping concentration over threshold volatge shift. It is seen that threshold voltage shift decreases with increase in doping concentration. This is due to the fact that bandgap alongwith trap density increases with increase in doping concentration which results into the reduction of threshold volatge shift value.

Table 1 Model parameters used in the calculations [19–22]

Parameters	Symbols	Values
Channel length	L	50 μm
Channel width	W	200 μm
Grain size	D_g	25 nm
Gate voltage	V_{gs}	20 V
Drain voltage	V_{ds}	1 V
Density of trapping states	N_t	2.5×10^{17} cm^{-3} eV^{-1}
Temperature	T	300 K
Dielectric strength of insulator layer	ε_i	7.5
Insulator layer thickness	t_i	300 nm
Characteristic trapping time	τ	1.46×10^6 s
Stretched-exponential exponent	β	0.45

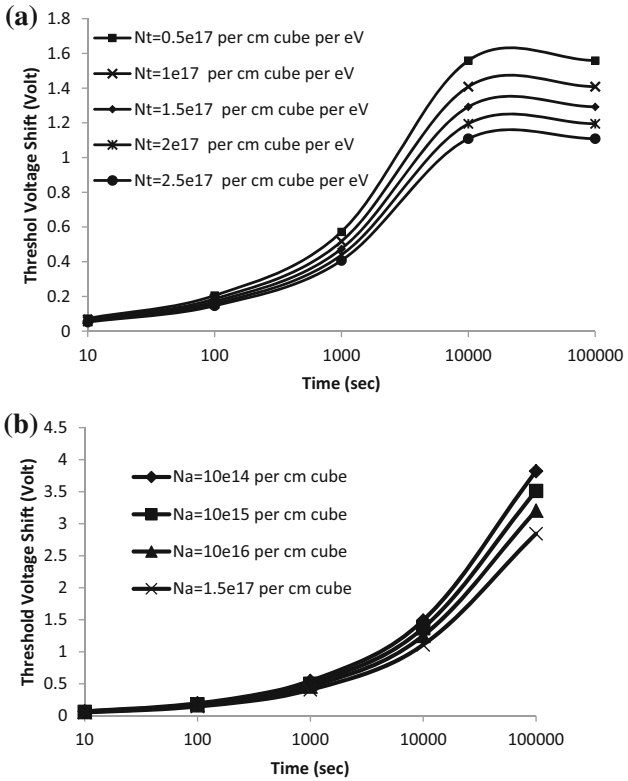

Fig. 5 **a** Computed variations of threshold voltage shift in the top gated nc-Si TFTs as a function of time for different trap state densities. **b** Computed variations of threshold voltage shift in the top gated nc-Si TFTs as a function of time for different values of doping concentration

Figure 6 shows the effect of grain size over threshold voltage shift. It is observed from the figure that for smaller grain size, threshold volatge shift increases with increase in grain size. This may be attributed to the fact that trap density decreases with increase in grain size [18] and therefore increase the threshold voltage shift values. However, for larger grain size ($D_g > 20$ nm), effect of dopant concentration dominates over the trap density effect and provide stability to the device. This implies that grain size must be larger in order to provide stability to the device by preventing the threshold voltage variation due to various device fabrication processes.

Figure 7 demonstrate the effect of gate dielectric thickness over threshold voltage shift. The result shows that threshold voltage shift reduces with increase in gate insulator thickness. This is due to the fact that as the insulator thickness

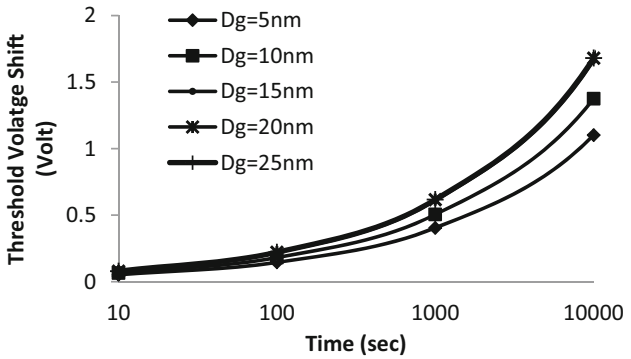

Fig. 6 Computed variations of threshold voltage shift in the top gated nc-Si TFTs as a function of time for different grain sizes

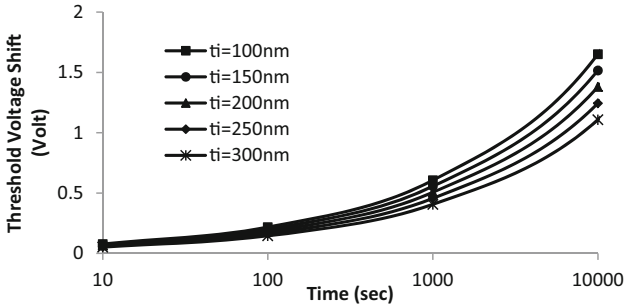

Fig. 7 Computed variations of threshold voltage shift in the top gated nc-Si TFTs as a function of time for different value of gate insulator thickness

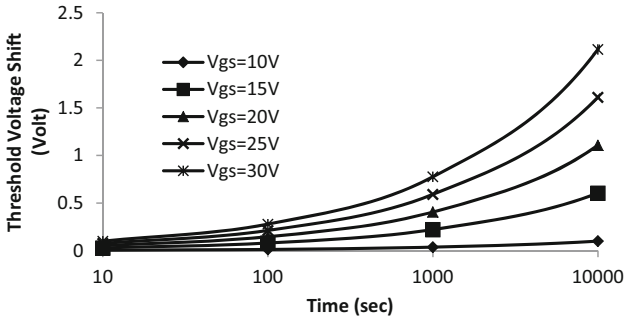

Fig. 8 Computed variations of threshold voltage shift in the top gated nc-Si TFTs as a function of time under different gate bias stress

increases it causes the increase in trap states available at insulator-channel interface which reduces the available carrier for transport and therefore reduces the threshold voltage shift.

Figure 8 shows the effect of bias voltage over threshold voltage shift. It is observed that threshold voltage shift increases with the bias voltage applied to the gate. For all values of bias voltage, threshold voltage shift increases with increase in bias stress time and after few hour (∼2 h), the threshold voltage saturates. Furthermore, it was observed that shift of the threshold voltage is symmetric among all the values of gate bias.

Table 2 Calculated and experimental [19] threshold volatge shift at different Vgs

	Theoretical ΔV_T	Experimental ΔV_T
$V_{gs} = 20$ V	0.42	0.35
$V_{gs} = 30$ V	0.81	0.77

The measured values of threshold voltage shift computed using Eq. (14) and the experimental values of Lee et al. [19] is shown in Table 2. It is clearly seen from the Table 2 that the results from analytical model using Eq. (14) are in considerable good agreement with experimental data [19]. However, the small difference may be due to the fact that the actual device used for the experiment may be slightly different in terms of purity of nc-Si channel layer.

4 Conclusion

This paper presented the instability mechanism involved in top-gated nc-Si TFT. The proposed analytical model includes the effect of various parameters like gate insulator thickness, doping concentration, grain size and grain boundary trapping states. The calculated threshold voltage shift is compared with the experimental data and considerable match between the two validate our model. This model can be used to estimate the threshold voltage shift in better form which may be used for improving the performance of new generation display application like OLED and LCD.

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