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Towards the design of hybrid QCA tiles targeting high fault tolerance

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Abstract The increasing fabrication cost of CMOS-based computing devices and the ever-approaching limits of their fabrication have led to the search for feasible options with high device density and low power waste. Quantum-dot cellular automata (QCA) is an emerging technology with such potential to match the design target beyond the limits of state-of-the-art CMOS. But nanotechnologies, like QCA are extremely susceptible to various forms of flaws and variations during fabrication at nano scale. Thus, the exploration of ingenious fault tolerant structure around QCA is gaining high importance. This work targets a new robust QCA tile structure hybridizing rotated and non-rotated cell together resulting lesser kink energy. Different QCA logic primitives (majority/minority logic, fanout tiles, etc.) are made using such hybrid cell structure. The functional characterization using the kink energy and the polarization level of such QCA structures under different cell defects have been thoroughly investigated. The results suggest that the proposed QCA logic primitives have achieved high fault tolerance of 97.43 %. Also, 100 % fault tolerance can be ascertained if the proposed logic circuit drives the correct output with the application of $\langle 001, 011 \rangle$ as a primitive test vector only. A comparative performance of the proposed logic over existing structure makes it more reliable.

Keywords Quantum-dot cellular automata · Fault tolerance · QCA defects · QCA tiles · Majority logic · QCA testing

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1 Introduction

Downscaling of CMOS devices is not possible beyond a certain limit and may phase out in future due to its inability to function at nanoscale level [1,2]. Quantum dot cellular automata (QCA) is intended to be the promising alternative in this direction that overcomes the limitations of CMOS [3] as it depends mainly on quantum effects and takes specific advantage of tunnelling to create a new compute fabric in nano scale [4,5]. The key aspect of QCA is that interaction between cells is purely coulombic and there is no transport of charge between cells.

Two arrangements of quantum-dot within in a cell referred to as the 45° ('×') normal cell and the 90° ('+') rotated cell can be utilized to compute the binary information. The rotated cell is identical in all ways to the standard cell except it is rotated by '45°' [6,7]. The fundamental QCA logic primitives are the three-input majority gate, wire, and inverter [4]. In coplanar wire-crossing, the rotated and non-rotated array of cells are placed together orthogonally to propagate the signals. Recent studies have also shown the feasibility of implementing logic gates and computing circuits by QCA [8–10].

Circuit reliability is an increasingly important design consideration for advanced logic circuits [11]. According to [12], the predictable huge complexity of nano architectures enforces the requirement of a high fault tolerance. Most

important, challenging issues for exploiting the complete potential of QCA circuits is fault tolerance and design complexity as described in [13]. Besides resolving the critical manufacturing issues, it has become utmost necessity to increase the fault tolerance capability of the QCA logic circuit [14,15].

On the other hand, the cell misplacement (cell misalignment, presence/absence of a cell) has been identified as the prime source of blockage to achieve reliable QCA logic circuit [16,17]. The cell misplacement defect has higher possibility to occur than stray charge defect and rotational cell defect for QCA because the process of cell deposition is very sensitive to the fabrication process of self-assembly [18]. Since QCA logic is based on a majority gate primitive, it's becoming an extreme necessity to achieve high fault tolerant structure (≈100 %) around the majority logic that is robust to cell misplacement defect. Several attempts are made to realize fault tolerant structure around majority logic [19–26].

Till date, tile structure in QCA is well recognized as a reliable inherent fault tolerant architecture by increasing redundant cells and up to 66.67 % fault tolerance is achieved as reported in [19,27–29] with detail characterization under manufacturing and misalignment defects. Also, in order to achieve more stability, electrons of QCA cell are ordered in such a way that it reaches minimum kink energy [6,30,31]. Molecular QCA tile with hybrid cell (rotated and non-rotated) can be developed through synthetic chemistry and patterning [7,18]. At this point, designing QCA is an "in-principle" activity meant to explore what might be possible if and when the fabrication issues are resolved [7].

Thus, all these motivate us to design an effective fault tolerant QCA architecture with proper analysis of the effect of kink energy and fault reporting. The issue of fault tolerance has been so far analysed from an implementation technology point of view [12,14] and very few from an architectural point of view [25,26]. In this paper, we study the issue of fault tolerance from an architectural point of view. So, without considering fabrication issues, this work only focuses on the architectural issues associated with cell deposition defects which occur during manufacturing of circuits. The remarkable contributions of this work can be summarized as follows:

- Realization of fault tolerant architecture (majority/minority) hybridizing rotated and non-rotated cell together.
- Impact of different orientation of quantum-dot and kink energy on fault tolerance are investigated implementing majority-minority logic.
- Analysis of robustness with regard to cell deposition defect.
- Design of two vector testable logic ensuring 100 % fault tolerance.
- Finally, synthesis of high level complex logic circuit using proposed robust majority is also established.

All the effects are verified based on physical proofs as well as simulation results using QCADesigner [32].

2 Preliminaries

In QCA based design, a single device (QCA-cell) is used for the construction of all components of an entire circuit (computational elements and wires). The schematic diagram of a four-dot QCA cell is shown in Fig. 1a. The cell consists of four quantum dots positioned at the corners of a square and contains two free electrons [3]. A quantum dot is a region where an electron is quantum-mechanically confined. Coulombic repulsion will cause classical models of the electrons to occupy only the corners of the QCA cell, resulting either in polarization P = −1 (logic 0) or in P = +1 (logic 1) as shown in Fig. 1a. The rotation of '45°' in normal cell causes the dots within the cell to have a vertical and horizontal placement relative to each other (called rotated cell). Unlike normal cells (×-cell), the polarizations of neighbouring rotated cells ('+'-cell) tend to align opposite each other.

The basic structure realized with QCA is the 3-input majority gate, $MV(A, B, C)$=$Maj(A, B, C)$=$AB + BC + CA$ (Fig. 1b). The majority gate can also function as a 2-input AND or a 2-input OR by fixing one of the three input cells to P = −1 or p = +1 respectively. Clocking plays a vital role in signal transition and propagation in QCA circuit. The cascaded clocking of four distinct and periodic phases (Relax, Switch, Hold and Release) as shown in Fig. 1c accomplish the task of synchronization in QCA [3].

Electrostatic interaction between charges in two QCA cells, i and j, is-

$$E^{m,n} = \frac{1}{4\pi\varepsilon_o\varepsilon_r}\sum_{i=1}^{4}\sum_{j=1}^{4}\frac{q_i^m q_j^n}{|r_{i,j}|} \tag{1}$$

Here ε_0 is the permittivity of the free space, ε_r is the relative permittivity of the material system, q_i^m is the charge in i^{th} dot of cell m and $r_{i,j}$ is the distance between the i^{th} dot of cell m and the j^{th} dot in cell n as shown in Fig. 1d. The kink energy is the difference in energy between two cells, which have opposite polarization and those same two cells having the same polarization (see Fig. 1d). Kink energy between two cells depends on the dimension of the QCA cell as well as the spacing between adjacent cells but not on the temperature.

2.1 Defects in QCA

In QCA, the cells must be precisely aligned at nano scales to provide correct functionality, so proper testing of these devices for manufacturing defects plays a major role in the

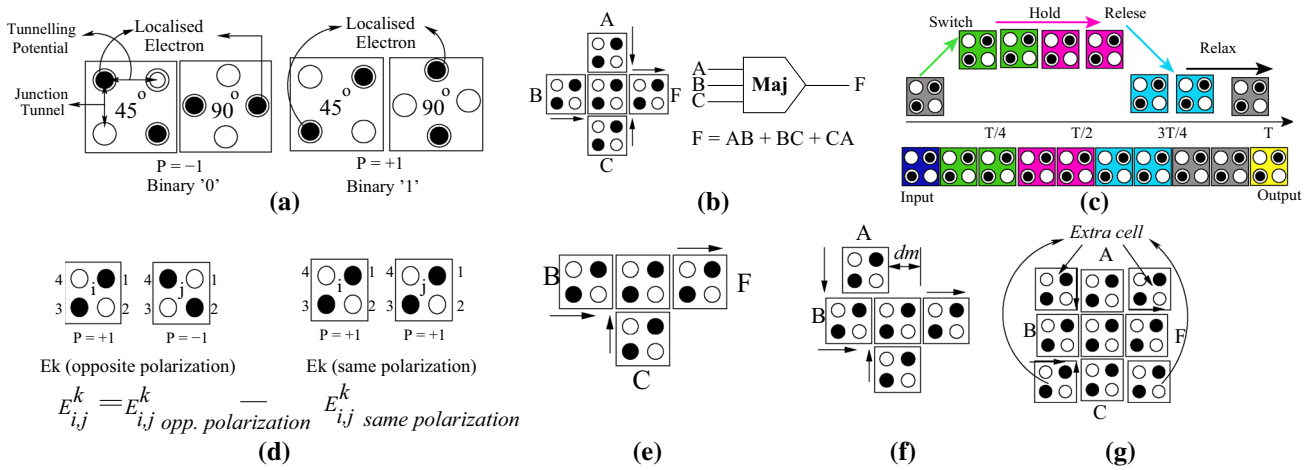

Fig. 1 **a** QCA cell with two different polarization and rotation, **b** fault free majority gate, **c** clocking, **d** Kink energy, **e** majority gate with missing cell defect, **f** majority gate with cell displacement defect, **g** majority gate with additional cell defect

quality of QCA based circuits. Defects can occur in both chemical synthesis phases as well as in deposition phases during the process of manufacturing. Defects are more likely to occur in the deposition phase than in the chemical synthesis phase, which may result in perfectly manufactured but imperfectly placed cells. The various defects which are likely to occur are:

1. Missing cell defect (see Fig. 1e),
2. Cell displacement defect (see Fig. 1f) and
3. Additional cell defect (see Fig. 1g).

To perform the defect characterization of QCA devices and circuits and study their effects at the logic - level, appropriate defect mechanisms and models must be considered.

3 Related work

The conventional majority gate (Fig. 2a) provides only 20 % fault tolerance under single cell deposition defect and this limited capability drastically becomes poor under multiple cell deposition. A new approach was proposed for the design of QCA-based Majority gate by considering two-dimensional arrays of QCA cells (tiles) rather than a single cell in the design of such a fate [27,29]. A fully/non-fully populated tile structures are investigated to obtain a fault tolerant design in [13,19,26,27]. Different useful nano structures, reduced size and efficient design of Nand Nor Inverter (NNI), 3×3 tile structures for implementing NNI, And Or Logic, and AOI are explored in [19]. Fault tolerance of the redundant version of the majority gate (orthogonal tile) achieves 66.67 % fault tolerance [27]. Another attempt to make fault tolerance architecture coupling majority of majority is explored in [23]. Wire-crossings are one of the most error prone zones in QCA. To improve the reliability in QCA logic circuit, a XOR ($\oplus$) logic module is also investigated in [33] to minimize the wire-crossings. This circuit can also be used for implementing as baseline tile as shown in the block diagram (Fig. 2d). Several variations of the XOR gate and wire crossing circuit have been created in order to properly route signals. Recently, two new fanout with complementary outputs are explored in [34] for efficient wire crossing in QCA. These are solely useful wiring in QCA only. But the use of unreliable units for the logical crossing may decreases its reliability to deposition defects.

In [27], the fault tolerance properties of PBW (processing by wire) are investigated when tiles are employed using molecular QCA cells. Based on a 3×3 QCA array of cells (Fig. 2c), with different input/output arrangements, different tiles are realized [19]. However, fault tolerance of this scheme is limited by the redundancy rate that the overall system can afford. The functional characterization and polarization level of these tiles for undeposited cell defects are covered. It is shown that novel features of PBW are possible due to spatial redundancy and QCA tiles are robust and inherently fault tolerant.

However, no such architecture in QCA is found which have high ($\approx$100 %) fault tolerance. In [35], different fault tolerant schemes to implement robust QCA, such as TMR (Triple Modular Redundancy), NAND- multiplexing and Maj-MUX, are analysed in terms of fault tolerance capacity and signal propagation speed. A TMR system generates a correct result at the output when at most one module is faulty. But it requires more number of cells and with its increased cells results in more deposition defects. Also, it will require at least two clock zones to obtain the output which will increase the delay. TMR will also have some wire-crossing and L-shaped tiles which will decrease the fault tolerance of the structure. Similarly, such redundancy exists in NAND-

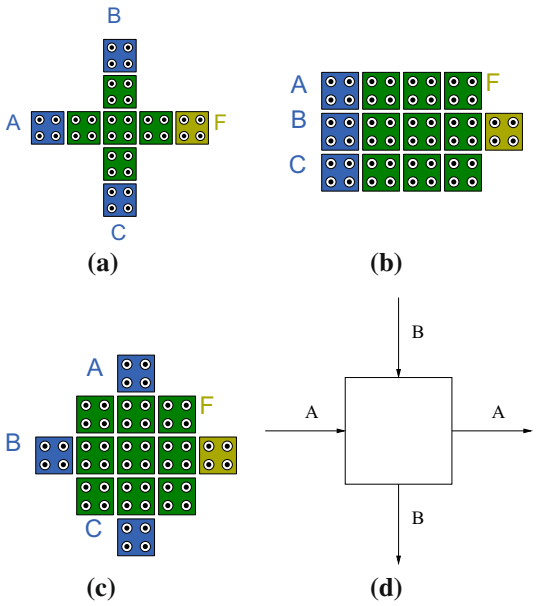

Fig. 2 **a** Majority voter, **b** cascaded tiles, **c** orthogonal tiles, **d** XOR(⊕) logic in [33]

multiplexing and Maj-MUX. On the other hand, an analysis of how QCA system reliability may be impacted by using various N-modular redundancy (NMR) schemes are reported in [36]. Experimental results describe that NMR in QCA can improve reliability in some cases, but can harm reliability in others [36]. All the earlier attempts mostly addressed the different scheme to enhance the defect tolerance in QCA logic circuit. However, the inherent architecture associated with the cell layout of logic primitives, considering fault tolerance in QCA has received less attention. Hence, all these factors motivate more research work on fault tolerant architecture around QCA logic primitives.

4 Impact of kink energy on QCA cell

It has already been identified that QCA tile structure has an inherent property of fault tolerance, which enables designing of more efficient circuits. In search of a more stable tile architecture with higher fault tolerance capability, we have designed a hybrid tile structure, placing alternately cross (×) and plus ('+') orientation cells (Fig. 3c). Following premises are considered for all of the calculations:

- The model involves $18 \times 18\,\text{nm}^2$ cells with inter cellular separation of 2 nm. The quantum dot diameter is 5 nm. The centre-to-centre distance of two quantum dots is taken as 9 nm. Using this definition other geometric distance between inter cellular quantum dots is calculated.
- Two or more cells in the same clock zone do not change the last outcome as per simulation output.

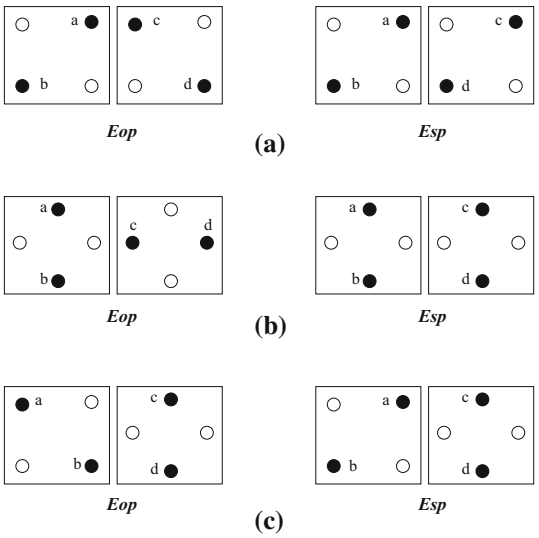

Fig. 3 Kink energy of QCA cells **a** with same orientation ×× **b** with same orientation ++ **c** with hybrid orientation

- In all figures, squares illustrate a QCA cell and the circles describes the electron position inside the cell.

The electrostatic energy between two electron charges is computed using Eq. (2). In this equation, $E_{i,j}$ is kink energy between i and j electron, k is fixed constant, q_1 and q_2 are electric charges, and r_{ij} is the distance between two electric charges i and j. By putting the values of k and q, we obtain the Eq. (2); $where, Kq_1q_2 = 9 \times 10^9 \times (1.6)^2 \times 10^{-38} = 23.04 \times 10^{-29}$.

$$E_{i,j} = \frac{kq_1q_2}{r} = \frac{23.04 \times 10^{-29}}{r}; \tag{2}$$

Total electrostatic energy for a given orientation of a cell is then given by $E = \sum E_{i,j}$. Kink energy is then calculated as $E_{kink} = E_{opp.} - E_{same}$.

For two cells with same orientation i.e. cross-cross and plus-plus adjacent cells (Fig. 3a, b) kink energies are estimated as described in Table 1. E_{xy} is the kink energy existing between electrons x and y. Also, r_{xy} is the distance between two electron charges. Then we calculate the total kink energy (E) in both states (opposite and same) using Eq. 2. Here, E_{op} means kink energy between two cells having opposite polarization states and E_{sp} means kink energy between two cells having same polarization states. Table 1 summarizes the kink energy for QCA cell with similar and different orientations (Fig. 3). Kink energy for QCA cell of same orientation is reduced to lesser kink energy using cell with different orientation.

It is evident from Table 1, cell orientation in Fig. 3a and b will be less stable than in Fig. 3c due to higher kink energy value. *In the following section we have synthesized a new*

Table 1 Estimation of kink energy for different cell-orientation

Distance (r_{xy})	Electrostatic energy, $E_{xy} = \frac{23.04\times10^{-29}}{r}$
QCA ××-cell with similar orientation (Fig. 3a)	
$r_{ac} = 2 \times 10^{-9}$	$E_1 \approx 11.52 \times 10^{-20}(j)$
$r_{ad} = 26.9 \times 10^{-9}$	$E_2 \approx 0.856 \times 10^{-20}(j)$
$r_{bc} = 26.9 \times 10^{-9}$	$E_3 \approx 0.856 \times 10^{-20}(j)$
$r_{bd} = 38 \times 10^{-9}$	$E_4 \approx 0.606 \times 10^{-20}(j)$
$E_{op} = \sum_{i=1}^{4} E_i = 13.838 \times 10^{-20}(j)$	
$r_{ac} = 20 \times 10^{-9}$	$E_1 \approx 1.152 \times 10^{-20}(j)$
$r_{ad} = 18.11 \times 10^{-9}$	$E_2 \approx 1.272 \times 10^{-20}(j)$
$r_{bc} = 42.04 \times 10^{-9}$	$E_3 \approx 0.548 \times 10^{-20}(j)$
$r_{bd} = 20 \times 10^{-9}$	$E_4 \approx 1.152 \times 10^{-20}(j)$
$E_{sp} = \sum_{i=1}^{4} E_i = 4.124 \times 10^{-20}(j)$	
$E_{kink} = E_{op} - E_{sp} = 9.714 \times 10^{-20}(J)$	
QCA ++-cell with similar orientation (Fig. 3b)	
$r_{ac} = 14.21 \times 10^{-9}$	$E_1 \approx 1.621 \times 10^{-20}(j)$
$r_{ad} = 30.36 \times 10^{-9}$	$E_2 \approx 0.759 \times 10^{-20}(j)$
$r_{bc} = 14.21 \times 10^{-9}$	$E_3 \approx 1.621 \times 10^{-20}(j)$
$r_{bd} = 30.36 \times 10^{-9}$	$E_4 \approx 0.759 \times 10^{-20}(j)$
$E_{op} = \sum_{i=1}^{4} E_i = 4.760 \times 10^{-20}(j)$	
$r_{ac} = 20 \times 10^{-9}$	$E_1 \approx 1.152 \times 10^{-20}(j)$
$r_{ad} = 26.9 \times 10^{-9}$	$E_2 \approx 0.856 \times 10^{-20}(j)$
$r_{bc} = 26.9 \times 10^{-9}$	$E_3 \approx 0.856 \times 10^{-20}(j)$
$r_{bd} = 20 \times 10^{-9}$	$E_4 \approx 1.152 \times 10^{-20}(j)$
$E_{sp} = \sum_{i=1}^{4} E_i = 4.016 \times 10^{-20}(j)$	
$E_{kink} = E_{op} - E_{sp} = 0.744 \times 10^{-20}(J)$	
QCA cell with different orientation (Fig. 3c)	
$r_{ac} = 29 \times 10^{-9}$	$E_1 \approx 0.794 \times 10^{-20}(j)$
$r_{ad} = 34.13 \times 10^{-9}$	$E_2 \approx 0.675 \times 10^{-20}(j)$
$r_{bc} = 21.09 \times 10^{-9}$	$E_3 \approx 1.092 \times 10^{-20}(j)$
$r_{bd} = 11 \times 10^{-9}$	$E_4 \approx 2.094 \times 10^{-20}(j)$
$E_{op} = \sum_{i=1}^{4} E_i = 4.655 \times 10^{-20}(j)$	
$r_{ac} = 11 \times 10^{-9}$	$E_1 \approx 2.094 \times 10^{-20}(j)$
$r_{ad} = 21.09 \times 10^{-9}$	$E_2 \approx 1.092 \times 10^{-20}(j)$
$r_{bc} = 34.13 \times 10^{-9}$	$E_3 \approx 0.675 \times 10^{-20}(j)$
$r_{bd} = 29 \times 10^{-9}$	$E_4 \approx 0.794 \times 10^{-20}(j)$
$E_{op} = \sum_{i=1}^{4} E_i = 4.655 \times 10^{-20}(j)$	
$E_{kink} = E_{op} - E_{sp} = 0(J)$	

QCA tile with the target to achieve high fault tolerance using proposed structure described in Fig. 3c.

5 Fault tolerant majority logic using QCA tiles

Despite the efficiency in design and demonstration, there are some difficulties in practical application and purpose of a QCA-based Majority Gate. Some initial efforts were made in [13,27] to implement a fault tolerant architecture of majority logic, but most of them incur either huge size or more latency ensuring average reliability.

As it is described earlier that hybridizing 90° and 45° cell together, kink energy can be lowered signifying more robust structure can be made feasible. Thus, in this work a new fault tolerant majority gate (called ft-Maj) is designed based on hybrid (90° and 45° orientation) cell as shown in Fig. 4. Three input cells (A, B, C) are connected to the gate at distinct positions, while an output cell (OUT) is offered at the remaining side. The design has a cell-count of 43 and covers

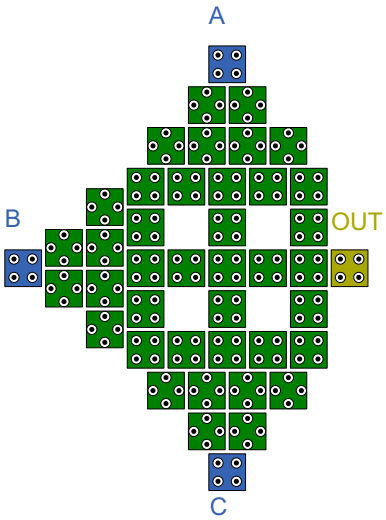

Fig. 4 Fault tolerant majority gate (ft-Maj)

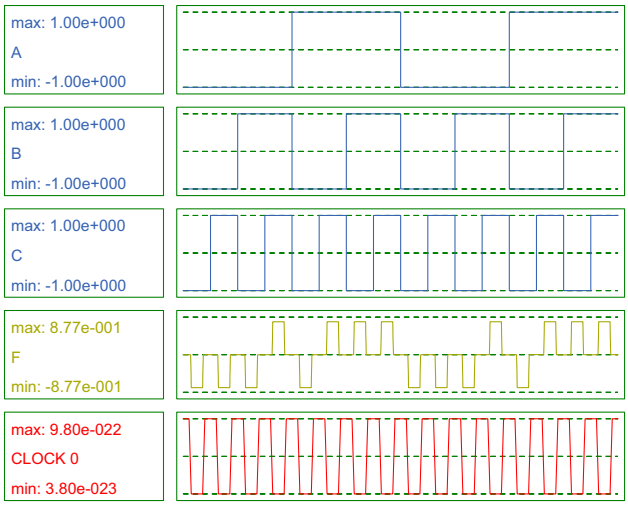

Fig. 5 Simulation of fault tolerant majority gate (ft-Maj)

an area of 0.04 μm^2. The proposed ft-Maj gate has a delay of one clocking zone (0.25 clock cycle). In the fault-free case, the production of this gate is Maj (A, B, C) = AB + BC + CA as shown in Fig. 5.

5.1 Physical verification of ft-Maj gate

In this section, a physical verification of logic/signal propagation in the proposed ft-Maj gate is provided. The proposed design has total 20 driver cells where signal stability is maintained by the 1–6, 12, 16, 17, 23, 24, 28 and 34–39 cells. All the faults that may occur in driver cells should be checked properly due to their capability in logic propagation. It has been found that an application of any input vector, the driver calls 7, 8, 9, 10, 11, 13, 14, 15, 18, 19, 20, 21, 22, 25, 26, 27, 29, 30, 31, 32, 33 attains the same polarity as that of the

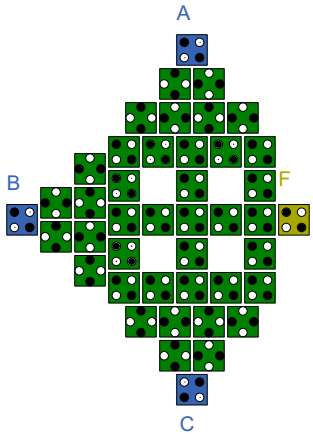

Fig. 6 Cell orientation of ft-Maj during the execution of vector 001

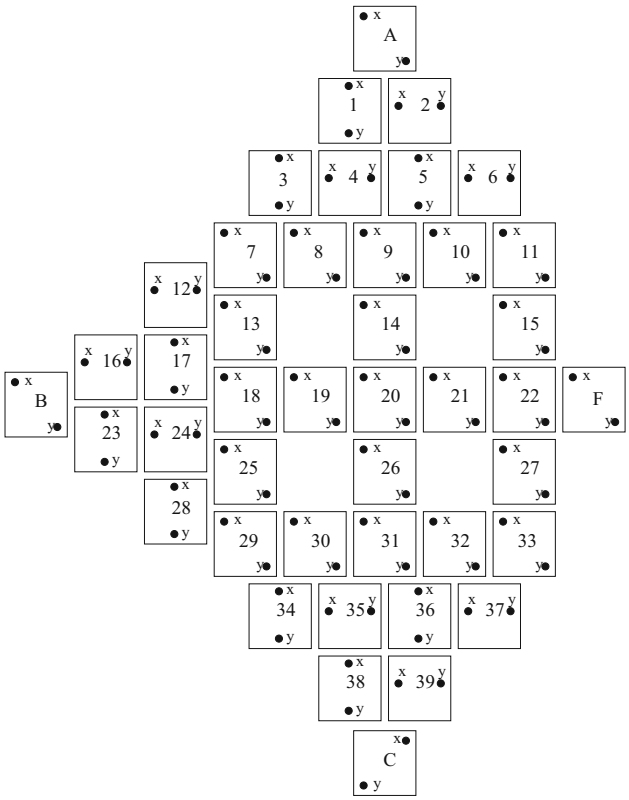

Fig. 7 Cell position of ft-Maj during the execution of vector 001

output. Thus, the polarization of the driver cell 22 is driven by the same polarity as that of the above mentioned cells. For instance, application of vector 001 the electrons in the cells orient themselves as shown in Fig. 6. For establishing why all these cell attains same polarity we calculate the kink energy for these mentioned cells' layout of Fig. 6 as shown in Fig. 7.

To work out the kink energy for any cell X, we calculate total electrostatic energy of those cells in its vicinity which are next to it. Interactions with other cells are considered to

Table 2 Physical verification for cell 7

Electron x	Electron y
Case A (Fig. 8a)	
$U_1 = 0.856 \times 10_{-20}$	$U_1 = 0.606 \times 10_{-20}$
$U_2 = 1.272 \times 10_{-20}$	$U_2 = 1.152 \times 10_{-20}$
$U_3 = 1.152 \times 10_{-20}$	$U_3 = 1.272 \times 10_{-20}$
$U_4 = 0.548 \times 10_{-20}$	$U_4 = 0.152 \times 10_{-20}$
$U_5 = 0.905 \times 10_{-20}$	$U_5 = 0.606 \times 10_{-20}$
$U_6 = 1.272 \times 10_{-20}$	$U_6 = 1.152 \times 10_{-20}$
$U_7 = 1.152 \times 10_{-20}$	$U_7 = 1.272 \times 10_{-20}$
$U_8 = 0.548 \times 10_{-20}$	$U_8 = 1.152 \times 10_{-20}$
$U_T = 16.069 \times 10^{-20}(J)$	
Case B (Fig. 8b)	
$U_1 = 1.152 \times 10_{-20}$	$U_1 = 0.548 \times 10_{-20}$
$U_2 = 11.52 \times 10_{-20}$	$U_2 = 0.856 \times 10_{-20}$
$U_3 = 11.52 \times 10_{-20}$	$U_3 = 0.856 \times 10_{-20}$
$U_4 = 0.856 \times 10_{-20}$	$U_4 = 0.606 \times 10_{-20}$
$U_5 = 0.548 \times 10_{-20}$	$U_5 = 11.52 \times 10_{-20}$
$U_6 = 0.856 \times 10_{-20}$	$U_6 = 1.152 \times 10_{-20}$
$U_7 = 0.856 \times 10_{-20}$	$U_7 = 11.52 \times 10_{-20}$
$U_8 = 0.606 \times 10_{-20}$	$U_8 = 0.856 \times 10_{-20}$
$U_T = 55.828 \times 10^{-20}(J)$	

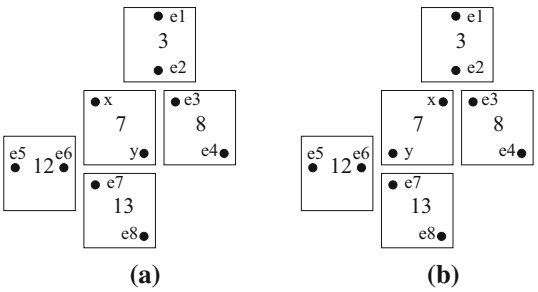

Fig. 8 Layout of cell 7 **a** Case A, **b** Case B

be very small. Like for cell 7, the total energy for the cells 3, 7, 8, 12, 13 are calculated with two different orientations of cell 7. The orientation of the electrons having the least energy is believed to be its target location. The calculations for cell 7 is shown in Table 2. From the table, it is evident that cell 7 will orient as a Fig. 8a due to its king energy.

Similar calculations are shown for cell 8 and 29 in Tables 3 and 4 which verifies the correct orientation for the cells. The main reason for showing the kink energy of cell 7, 8 and 29 is that it formalizes an idea how electrons are arranged in these cells.

As the proof method is similar for all cells, all the other cells can also be verified in a similar fashion. In this way all the cells 7, 8, 9, 10, 11, 13, 14, 15, 18, 19, 20, 21, 25, 26, 27, 29, 30, 31, 32, 33 drives the logic of the cell 22 i.e. the driver cell.

Table 3 Physical verification for cell 8

Electron x	Electron y
Case A (Fig. 9a)	
$U_1 = 1.152 \times 10_{-20}$	$U_1 = 0.548 \times 10_{-20}$
$U_2 = 11.52 \times 10_{-20}$	$U_2 = 0.856 \times 10_{-20}$
$U_3 = 1.621 \times 10_{-20}$	$U_3 = 0.759 \times 10_{-20}$
$U_4 = 0.743 \times 10_{-20}$	$U_4 = 0.759 \times 10_{-20}$
$U_5 = 1.152 \times 10_{-20}$	$U_5 = 0.548 \times 10_{-20}$
$U_6 = 1.272 \times 10_{-20}$	$U_6 = 1.152 \times 10_{-20}$
$U_7 = 1.152 \times 10_{-20}$	$U_7 = 1.272 \times 10_{-20}$
$U_8 = 0.548 \times 10_{-20}$	$U_8 = 1.152 \times 10_{-20}$
$U_9 = 0.815 \times 10_{-20}$	$U_9 = 0.605 \times 10_{-20}$
$U_{10} = 0.605 \times 10_{-20}$	$U_{10} = 0.814 \times 10_{-20}$
$U_{11} = 0.815 \times 10_{-20}$	$U_{11} = 8.419 \times 10_{-20}$
$U_{12} = 0.429 \times 10_{-20}$	$U_{12} = 0.815 \times 10_{-20}$
$U_T = 39.253 \times 10^{-20}(J)$	
Case B (Fig. 9b)	
$U_1 = 0.905 \times 10_{-20}$	$U_1 = 0.606 \times 10_{-20}$
$U_2 = 1.272 \times 10_{-20}$	$U_2 = 1.152 \times 10_{-20}$
$U_3 = 1.621 \times 10_{-20}$	$U_3 = 0.759 \times 10_{-20}$
$U_4 = 1.621 \times 10_{-20}$	$U_4 = 0.581 \times 10_{-20}$
$U_5 = 0.606 \times 10_{-20}$	$U_5 = 0.856 \times 10_{-20}$
$U_6 = 0.856 \times 10_{-20}$	$U_6 = 11.52 \times 10_{-20}$
$U_7 = 11.52 \times 10_{-20}$	$U_7 = 0.856 \times 10_{-20}$
$U_8 = 0.856 \times 10_{-20}$	$U_8 = 0.606 \times 10_{-20}$
$U_9 = 0.536 \times 10_{-20}$	$U_9 = 1.146 \times 10_{-20}$
$U_{10} = 0.536 \times 10_{-20}$	$U_{10} = 1.146 \times 10_{-20}$
$U_{11} = 1.146 \times 10_{-20}$	$U_{11} = 1.146 \times 10_{-20}$
$U_{12} = 0.536 \times 10_{-20}$	$U_{12} = 0.536 \times 10_{-20}$
$U_T = 42.921 \times 10^{-20}(J)$	

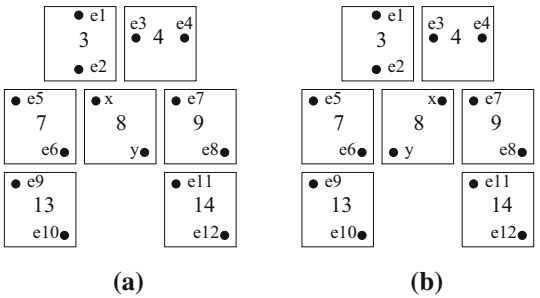

Fig. 9 Layout of cell 8 **a** Case A, **b** Case B

5.2 Characterization of fault tolerance of ft-Maj tiles

The different cell position of ft-Maj are pointed in Fig. 11. The exhaustive simulation is performed for the single missing and additional cell deposition defect on ft-Maj which are summarised in Table 5. The first part of the Table 5 shows the simulation results when at most one cell is undeposited from

Table 4 Physical verification for cell 29

Electron x	Electron y
Case A (Fig. 10a)	
$U_1 = 1.152 \times 10_{-20}$	$U_1 = 0.548 \times 10_{-20}$
$U_2 = 1.272 \times 10_{-20}$	$U_2 = 1.152 \times 10_{-20}$
$U_3 = 1.621 \times 10_{-20}$	$U_3 = 0.790 \times 10_{-20}$
$U_4 = 1.621 \times 10_{-20}$	$U_4 = 1.621 \times 10_{-20}$
$U_5 = 1.152 \times 10_{-20}$	$U_5 = 1.272 \times 10_{-20}$
$U_6 = 0.548 \times 10_{-20}$	$U_6 = 1.152 \times 10_{-20}$
$U_7 = 0.856 \times 10_{-20}$	$U_7 = 11.52 \times 10_{-20}$
$U_8 = 0.548 \times 10_{-20}$	$U_8 = 1.152 \times 10_{-20}$
$U_T = 27.977 \times 10^{-20}(J)$	
Case B (Fig. 10b)	
$U_1 = 0.856 \times 10_{-20}$	$U_1 = 0.606 \times 10_{-20}$
$U_2 = 11.52 \times 10_{-20}$	$U_2 = 0.856 \times 10_{-20}$
$U_3 = 0.759 \times 10_{-20}$	$U_3 = 0.790 \times 10_{-20}$
$U_4 = 0.799 \times 10_{-20}$	$U_4 = 1.621 \times 10_{-20}$
$U_5 = 11.52 \times 10_{-20}$	$U_5 = 0.856 \times 10_{-20}$
$U_6 = 0.856 \times 10_{-20}$	$U_6 = 0.606 \times 10_{-20}$
$U_7 = 1.152 \times 10_{-20}$	$U_7 = 1.272 \times 10_{-20}$
$U_8 = 0.606 \times 10_{-20}$	$U_8 = 0.856 \times 10_{-20}$
$U_T = 35.491 \times 10^{-20}(J)$	

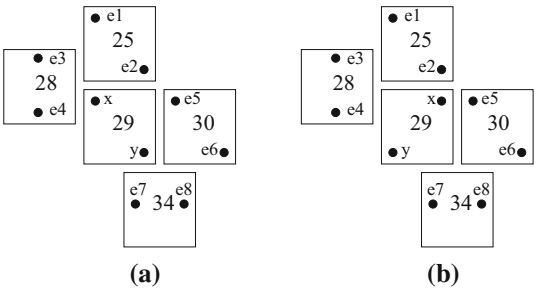

Fig. 10 Layout of cell 29 **a** Case A, **b** Case B

the ft-Maj tile. Once undeposited cell defects are present, the three input signals may also interact, such that different functions can be generated at the output, i.e., the relation between the inputs and placement of the cells for tile may be changed. In particular, variants of the majority function (with complemented input variables) are expected due to possible input inversion through the cells of the tile. The variants of the majority function are referred to as MV-like functions.

The following observations can be established from the Table 5:

(i) In all cases of missing cell defect, ft-Maj gate results into MV/MV-like function.
(ii) Almost all (97.43 %) cases of single missing-cell deposition defect does not change the logic function of the proposed ft-Maj gate, thus conforming defect-tolerant (robust) design of a majority voter.
(iii) Whenever only cell 22 is undeposited, the output of ft-Maj gate gets inverted with respect to the fault- free output.
(iv) Single additional cell at positions II, IV has no effect on the output of ft-Maj gate.
(v) For additional cell at position I and III only, ft-Maj gate becomes faulty.

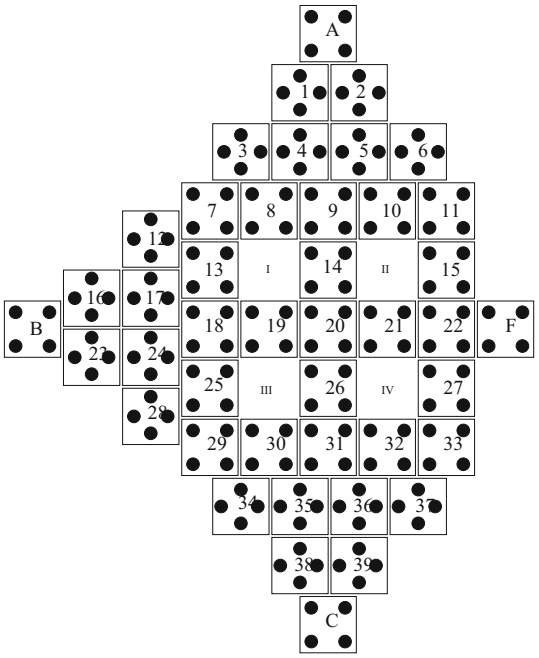

Fig. 11 ft-Maj gate with different cell position

Further, the statistical results in the presence of up to two undeposited cells are summarized in Table 6. Due to multiple cell deposition defect, the three input functions interact to form a new output function which may be like the MV-like function or some wire like function. It also generates some partially polarized or polarization, less than 0.1 as output, which we consider as undefined states. The probability of generating different majority functions versus the number of undeposited cells is shown in Table 6.

A relative performance on different orthogonal tiles is reported in Table 7 which shows the high quality of the proposed tiles over conventional tiles. The probability of generating different functions successfully signifying the fault tolerance capability shown in Fig. 12. It is evident from the Fig. 12 that even with multiple undeposited cell, in **atleast** 80 % of the cases ft-Maj can still function as a majority logic whereas the conventional tiles degrades performance with increase of cell deposition. This is done by its spatial redundancy, therefore, an excellent point of resilience in functionality is attained.

Table 5 Impact of missing cell and additional cell defect

Missing cell defect			
Missing cell	Output	Missing cell	Output
None	MV	11	MV
1	MV	12	MV
2	MV	13	MV
3	MV	14	MV
4	MV	15	MV
5	MV	16	MV
6	MV	17	MV
7	MV	18	MV
8	MV	19	MV
9	MV	20	MV
10	MV	21	MV
21	MV	31	MV
22	MV'	32	MV
23	MV	33	MV
24	MV	34	MV
25	MV	35	MV
26	MV	36	MV
27	MV	37	MV
28	MV	38	MV
29	MV	39	MV
30	MV		
Additional cell defect			
Additional cell	Output	Additional cell	Output
I	C	II	MV
III	A	IV	MV

Here, MV = AB+BC+CA and
MV' = Inverse of MV

Apart from the tabulated result, the following observations have been made from the simulation results of the ft-Maj:

- Average polarization of the correct output function is in the range of ±0.86 to ±0.89.
- Highest polarization of ±0.93 is observed when the cell no 15 and 27 is missing.
- Faulty outputs resulting from cell undeposition have an average polarization of ±0.77 to ±0.79 and a minimum of ±0.59 is observed when cells (15, 22) and (22, 27) are missing.
- Inputs A and C that is the vertical inputs generates more wire like function than input B which indicates signal propagation in horizontal direction is much stronger than in vertical cases.

The faulty behaviour of ft-Maj gate in the presence of all possible input vector of length three is reported in Table 8.

Table 6 Functional characterization of ft-Maj tile with multiple cell defects

Function	# Cell deposition defect	
	1	2
A	0	40
A′	0	1
B	0	5
C	0	40
C′	0	1
Undefined	0	11
Maj (A′, B, C)	0	1
Maj (A, B′, C)	0	2
Maj (A, B, C′)	0	1
Maj (A′, B′, C′)	1	25
Maj (A, B, C)	38	614
Total	39	741

From Table 8, it is evident that missing cell at position 22 generates an inversion of the fault-free production for any input vector. Hence, this defect can be discovered by any input test vector. Once more, for additional single-cell defect at positions I and III, the faulty outputs becomes C and A respectively. For input vector 001, additional cell deposition at position I produce output 1 whereas the expected output is 0. Thus, it can be detected by this input vector {001}. The test vectors that can detect all these faults are summarized in 5th and 7th column of Table 8. If the proposed ft-Maj gate operates correctly during application of the test vector {001, 011}, it can be assured that there is at least no additional cell deposition and cell 22 is not missing. If cell 22 and no additional cell deposition occur, the ft-Maj will work properly in all other cases even in the presence of any cell deposition fault. Hence, it follows that the test vectors {001, 011} can be a minimal test set for discovering all possible (100 %) single cell deposition defects in the proposed ft-Maj gate. *So, if the ft-Maj gate work properly for input vector {001, 011}, we can ensure/ascertain that it will provide 100 % fault tolerance under any single missing and additional cell deposition faults.* In the following subsection, the various tiles that can be synthesized from the proposed ft-Maj tile and a relative comparison has been made with the corresponding structures in [27].

5.3 Double fan-out tile

The double fan-out tile is shown in Fig. 13. It has one input cell B and two output cells $F1$ and $F2$. In fault free condition, both $F1$ and $F2$ have the input value B. Table 9 shows defect pattern when a single cell is missing. Table 10 shows functional characterization of double fan-out tile when 1 and

Table 7 Comparative analysis of different fault tolerant majority logic

Observations	Results			
	Orthogonal tile [27]		Proposed ft-Maj (Fig. 4)	
No. of undeposited cells	1	2	1	2
No. of defective patterns	9	36	39	741
Occurrence of wire func.	0	4	0	85
Wire func. (%)	0	11.1	0	11.47
Occurrence of INV func.	0	4	0	2
INV func. (%)	0	11.1	0	0.27
Occurrence of MV func.	6	13	38	614
MV func. (%)	66.7	36.1	97.44	82.86
Occurrence of MV like func.	3	11	1	29
MV like func. (%)	33.3	30.5	2.56	3.91
Occurrence of undefined state	0	4	0	11
Undefined state (%)	0	11.1	0	1.48

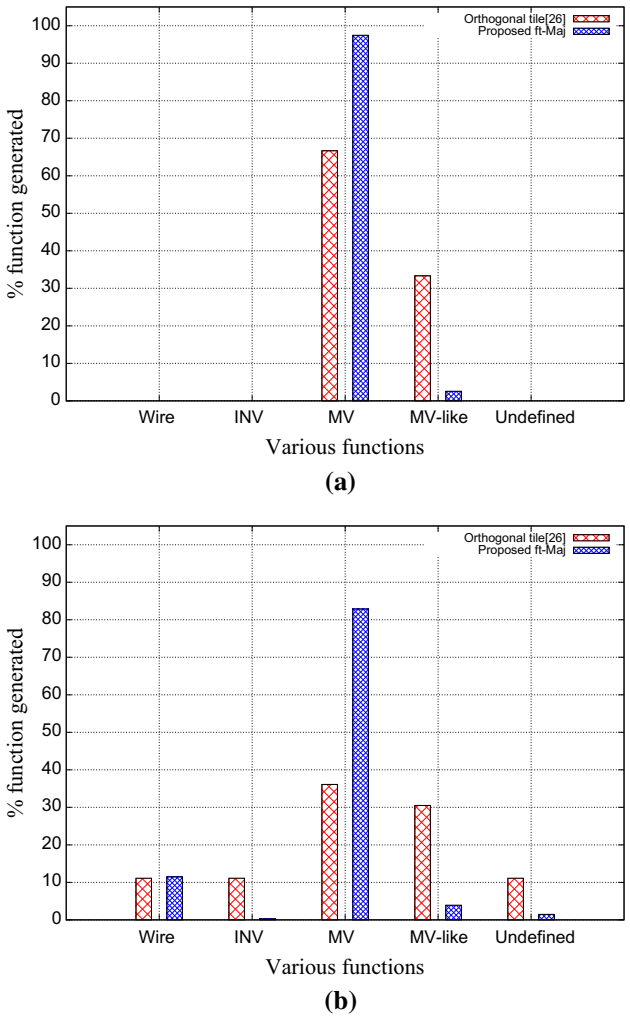

Fig. 12 Fault tolerance capability of different tiles under **a** single cell **b** double cell deposition

Table 8 Test vector for missing and additional cell defect

IV	EO	FO Cell 22	FO Cell I	TV	FO Cell III	TV
000	0	1	0	001	0	
001	0	1	1		0	
010	0	1	0		0	
011	1	0	1		0	011
100	0	1	0	110	1	100
101	1	0	1		1	
110	1	0	0		1	
111	1	0	1		1	

IV input vector, *EO* expected output, *FO* faulty output, *TV* test vector

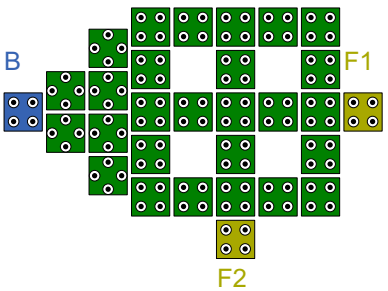

Fig. 13 Double fan-out tile

2 cells are missing as well as a relative comparison is made with that of [27]. The simulation result is shown in Fig. 14.

The following observations has been made from the simulation of the double fan-out tile (Fig. 15):

- When cell 16 is removed output is $\overline{A}$ at $F1$ and when cell 25 is removed it gives $\overline{A}$ at $F2$.
- Average polarization of the fault free output is in the range of ± 0.82 to ± 0.93.

Table 9 Single cell undeposited defect in double fan-out tile

Cell removed	F1	F2	Cell removed	F1	F2
None	B	B	1	B	B
2	B	B	3	B	B
4	B	B	5	B	B
6	B	B	7	B	B
8	B	B	9	B	B
10	B	B	11	B	B
12	B	B	13	B	B
14	B	B	15	B	B
16	B′	B	17	B	B
18	B	B	19	B	B
20	B	B	21	B	B
22	B	B	23	B	B
24	B	B	25	B	B′
26	B	B	27	B	B

- When cell 16 and 25 are removed the polarization of output $\overline{A}$ is in the range ± 0.79 to ± 0.80.
- When the cells (9, 16), (16, 21), (24, 25) and (25, 26) are removed, there is a drop in polarization of the output $\overline{A}$ to ± 0.52.
- Removal of cell (22,14) gives $\overline{A}$ of very high polarization of ± 0.94.
- When the polarization level of the output is very low (of the order of ± 0.1) we consider the state as no logic or undefined state.

A relative performance on different double fanout tiles is reported in Table 10. The probability of generating different functions successfully signifying the fault tolerance capability shown in Fig. 16. It is evident from the Fig. 16 that even with multiple undeposited cells due to defects, in **atleast** 90 % of the cases our proposed can still function as a wire whereas the conventional tiles degrades performance with increase of cell deposition.

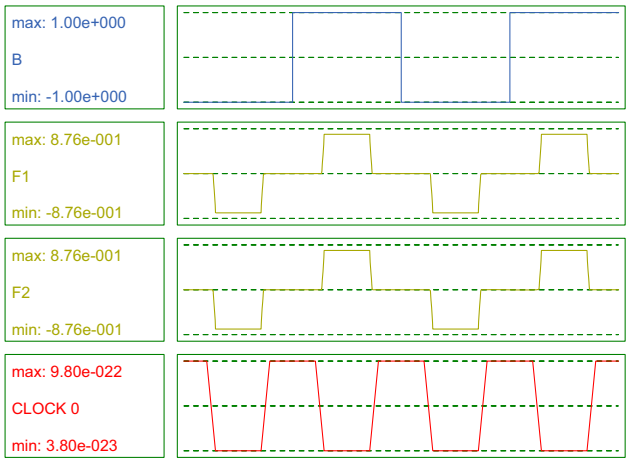

Fig. 14 Double fan-out tile simulation result

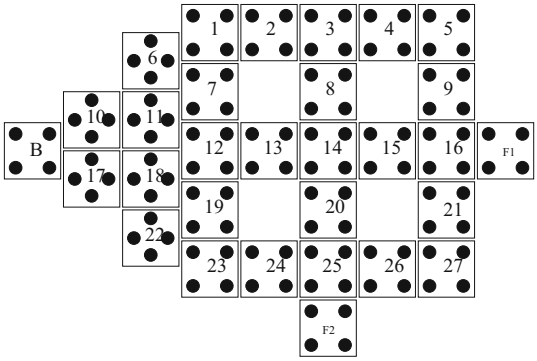

Fig. 15 Double fan-out tile with cell position

5.4 Triple fan-out tile

Figure 17 shows the triple fan-out tile. It has one input cell A and three output cells $F1$, $F2$ and $F3$. The simulation output has been shown in Fig. 18. Table 11 shows single cell missing defect pattern. Table 12 shows the functional characterization of triple fan-out tile when one and

Table 10 Functional Characterization of double fan-out tile

Observations	Results							
	Double fan-out tile of [27]				Double fan-out tile of Fig. 15			
Output Cells	F1		F2		F1		F2	
Number of undeposited cells	1	2	1	2	1	2	1	2
Number of defective patterns	9	36	9	36	27	351	27	351
Occurrence of wire func.	7	20	7	20	26	323	26	322
Wire func. (%)	77.78	55.56	77.78	55.56	96.29	92.02	96.29	91.74
Occurrence of INV func.	2	16	2	16	1	22	1	25
INV func. (%)	22.22	44.44	22.22	44.44	3.71	6.27	3.71	7.12
Occurrence of undefined state	0	0	0	0	0	6	0	4
Undefined state (%)	0	0	0	0	0	1.71	0	1.14

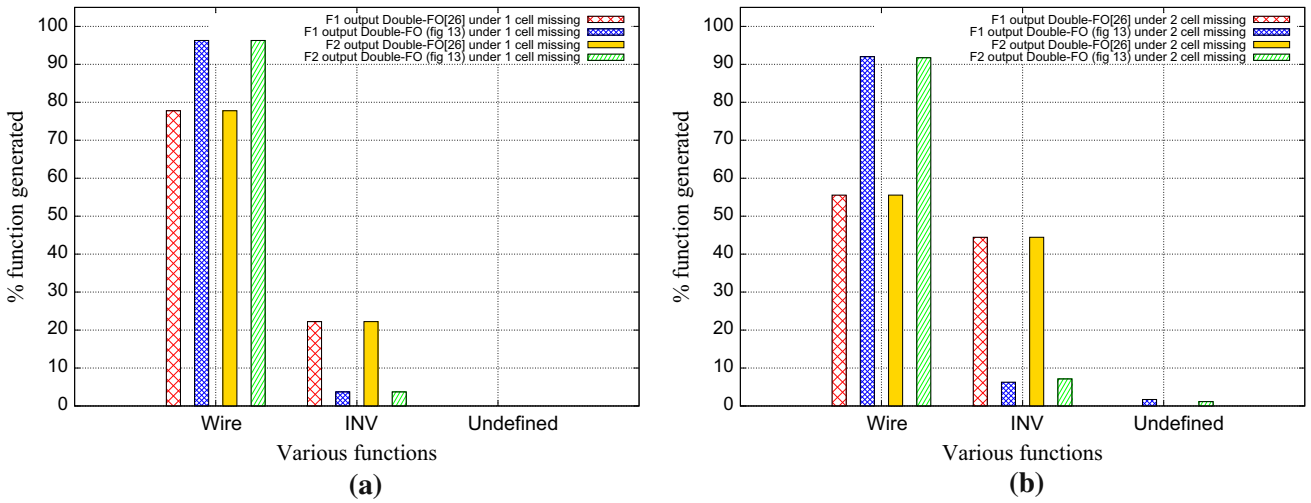

Fig. 16 Fault tolerance capability of double fanout under **a** single cell **b** double cell deposition

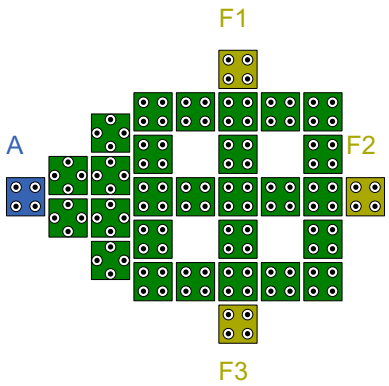

Fig. 17 Triple fan-out tile

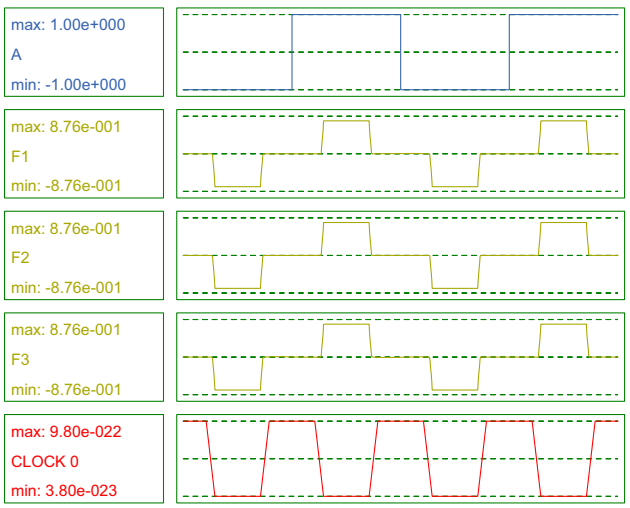

Fig. 18 Simulation of triple fan-out tile

two cells are undeposited. The following observations have been made from the simulation of the triple fan-out tile (Fig. 19):

Table 11 Single cell undeposited defect in triple fan-out tile

Cell removed	F1	F2	F3	Cell removed	F1	F2	F3
None	A	A	A	1	A	A	A
2	A	A	A	3	A′	A	A
4	A	A	A	5	A	A	A
6	A	A	A	7	A	A	A
8	A	A	A	9	A	A	A
10	A	A	A	11	A	A	A
12	A	A	A	13	A	A	A
14	A	A	A	15	A	A	A
16	A	A′	A	17	A	A	A
18	A	A	A	19	A	A	A
20	A	A	A	21	A	A	A
22	A	A	A	23	A	A	A
24	A	A	A	25	A	A	A′
26	A	A	A	27	A	A	A

- Removal of cell 3 gives $\overline{A}$ at $F1$, removal of cell 16 gives $\overline{A}$ at $F2$ and removal of cell 25 gives $\overline{A}$ at $F3$.
- Average polarization of the fault free output is in the range of ± 0.82 to ± 0.93.
- When cell 3, 16 and 25 are missing the polarization of output $\overline{A}$ is in the range ± 0.79 to ± 0.80.
- When the cell combinations of (2,3), (3,4), (9,16), (16,21), (24,25) and (25,26) are undeposited there is a drop in polarization of the output $\overline{A}$ to ± 0.52.
- Removal of cell (6,14) and cell (22,14) gives $\overline{A}$ of very high polarization of ± 0.94.
- When the polarization level of the output is very low (of the order of ± 0.1) we consider the state as no logic or undefined state.

Table 12 Functional characterization of triple fan-out tile

Observations	Results											
	Triple fan-out tile of [27]						Triple fan-out tile of Fig. 19					
Output cells	F1		F2		F3		F1		F2		F3	
Number of undeposited cells	1	2	1	2	1	2	1	2	1	2	1	2
Number of defective patterns	9	36	9	36	9	36	27	351	27	351	27	351
Occurrence of wire func.	7	20	7	20	7	20	26	322	26	323	26	322
Wire func. (%)	77.78	55.56	77.78	55.56	77.78	55.56	96.29	91.74	96.29	92.02	96.29	91.74
Occurrence of INV func.	2	16	2	16	2	16	1	25	1	22	1	25
INV func. (%)	22.22	44.44	22.22	44.44	22.22	44.44	3.71	7.12	3.71	6.27	3.71	7.12
Occurrence of undefined state	0	0	0	0	0	0	0	4	0	6	0	4
Undefined state (%)	0	0	0	0	0	0	0	1.14	0	1.71	0	1.14

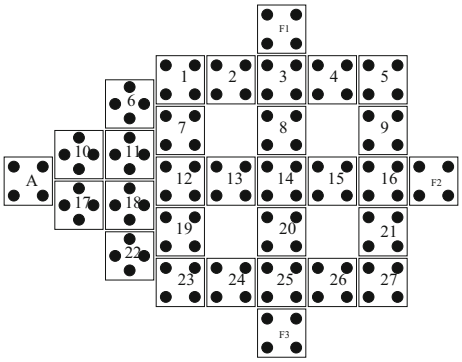

Fig. 19 Triple fan-out tile with cell position

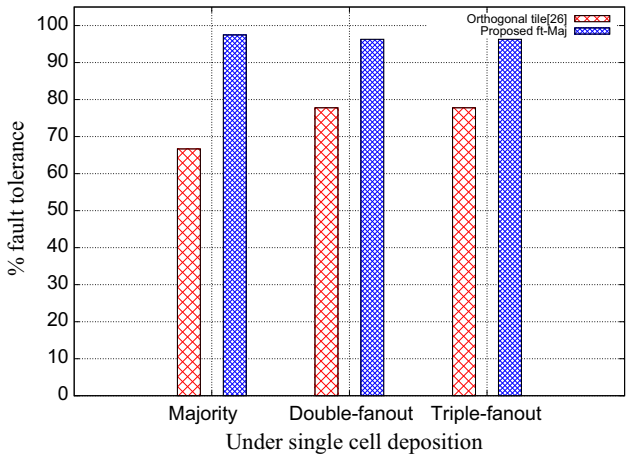

Fig. 21 Overall performance of the QCA tiles

The probability of generating different function by triple fanout tile under single cell deposition is presented in Fig. 20.

An overall performance of different tiles implementing majority, double and triple fanout is shown in Fig. 21.

The Fig. 21 indicates the superiority of the proposed logic showing enviable ≈100 % fault tolerance under single cell deposition defect.

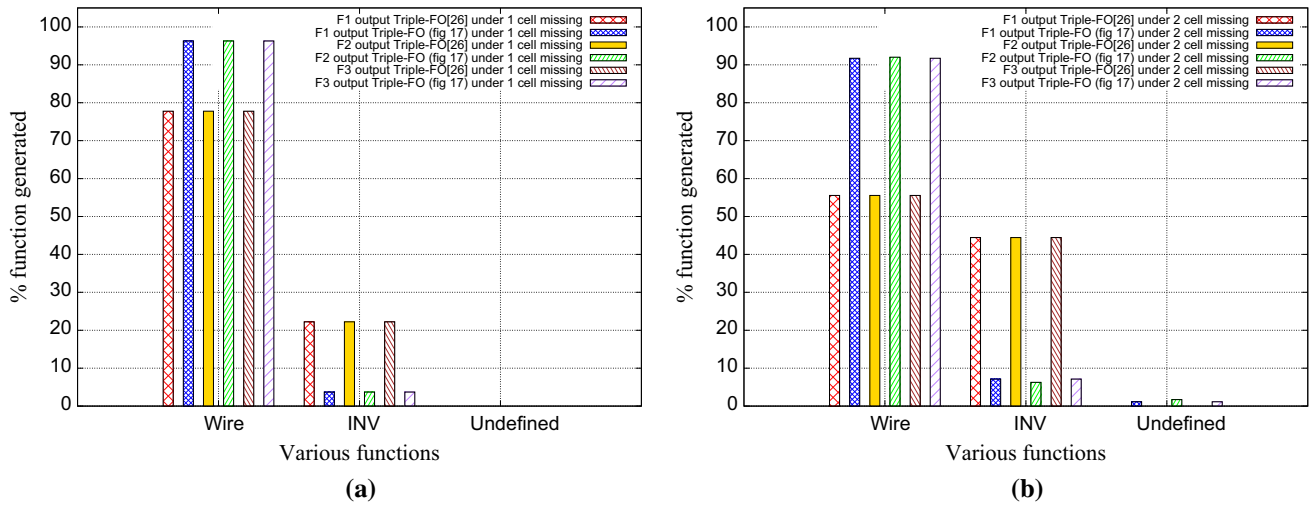

Fig. 20 Fault tolerance capability of triple fanout under **a** single cell **b** double cell deposition

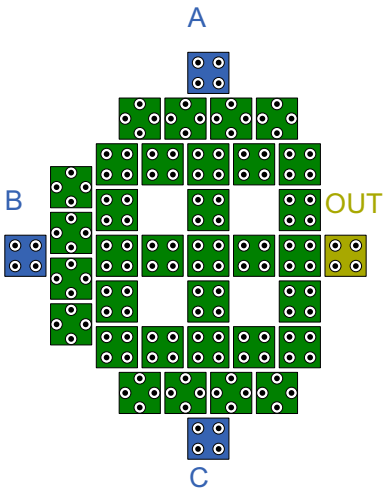

Fig. 22 Fault tolerant minority gate (ft-Min)

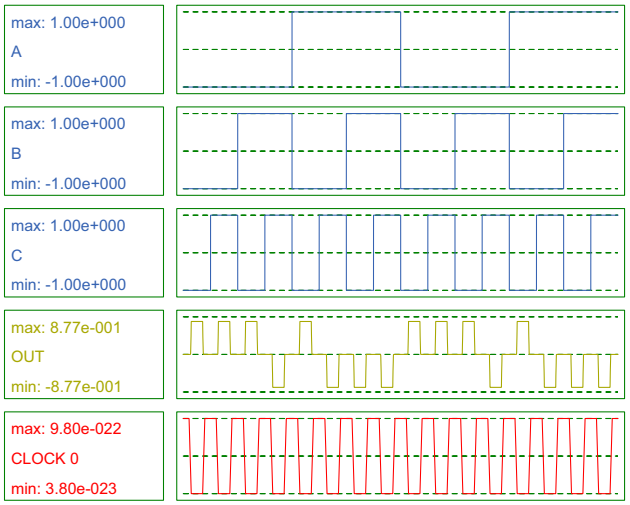

Fig. 23 Simulation result of fault tolerant minority gate (ft-Min)

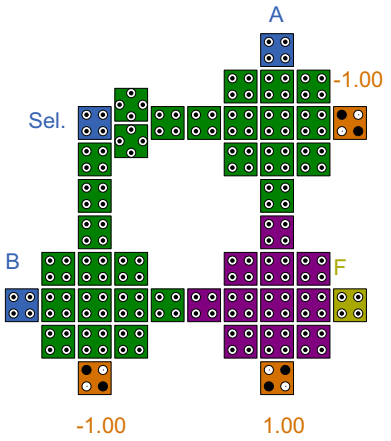

Fig. 24 2:1 Multiplexer using orthogonal tile in [27]

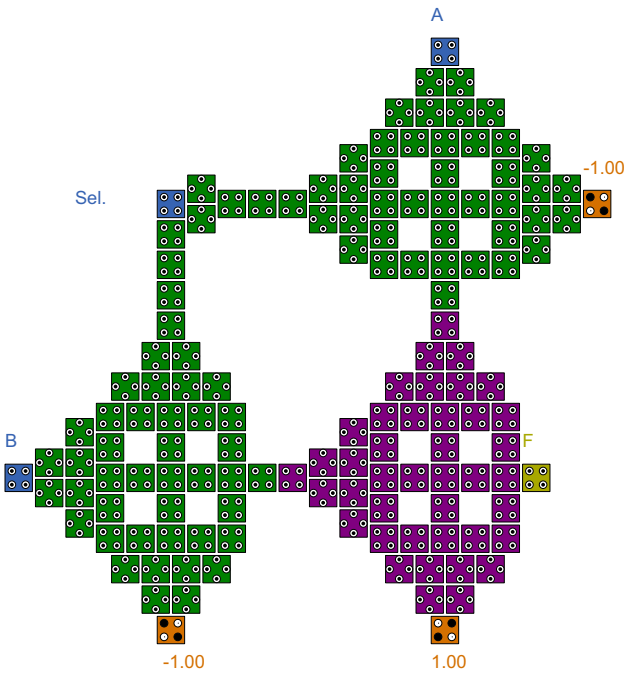

Fig. 25 2:1 Multiplexer using proposed ft-Maj tile

6 Design of fault tolerant minority logic (ft-Min)

The robustness of the fault tolerant structure with hybrid cell can be extended to other logic circuit also, like minority logic (called ft-Min) as shown in Fig. 22. The design has a cell-count of 37 and covers an area of 0.04 μm^2. The proposed ft-Min gate has a delay of the one clocking zone. The simulation result of ft-Min is shown in Fig. 23.

In all faulty cases, a ft-Min gate results into MV/MV-like function. Single missing-cell deposition defect on almost all (96.97 %) cases does not change the logic function of the proposed ft-Min gate, thus conforming fault-tolerant (robust) design of a minority voter. Whenever cell 19 is undeposited, the output of the ft-Min gate gets inverted with respect to the fault free output To the best of our knowledge, this is the first attempt to obtain a minority gate which is robust in terms of single missing-cell deposition defect. The only fault, resulting from missing cell at position 19, can be detected by any test vector at test mode.

7 High level logic synthesis

Until now, the performance of the ft-Maj tile is explored. To put it into effect, we need to evaluate its performance in circuit level also. For this purpose, two 2:1 multiplexer is designed using the orthogonal tile [27] as shown in Fig. 24 and ft-Maj tile (Fig. 4) as shown in Fig. 25. Its simulation

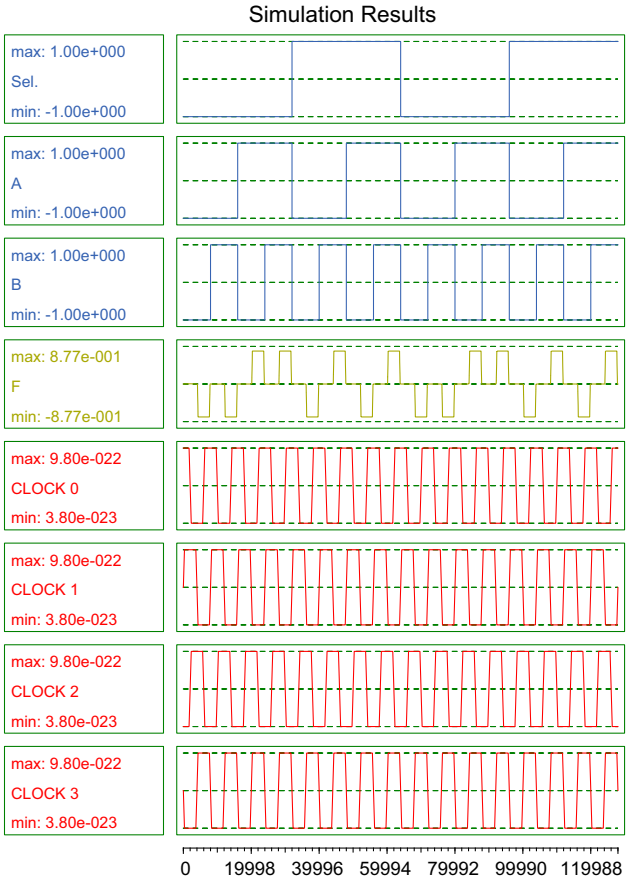

Fig. 26 Simulation result of 2:1 multiplexer

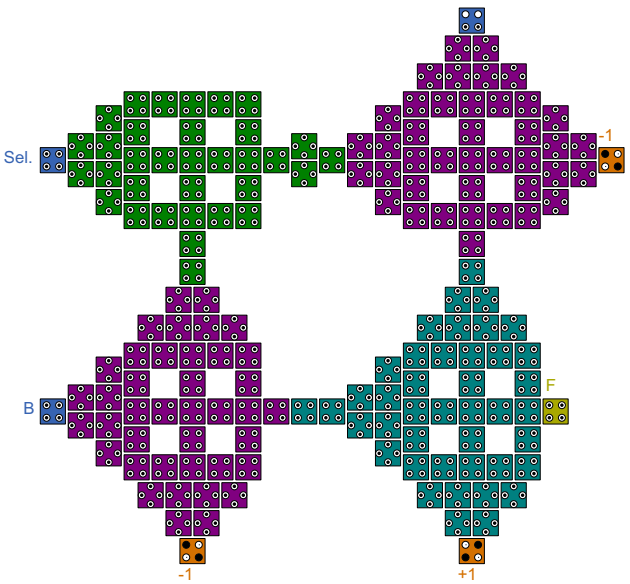

Fig. 27 2:1 Multiplexer using fanout and ft-maj tile

result is depicted in Fig. 26 verifies the functionality of the 2:1 multiplexer implemented with ft-maj. Further, the fanout (for input S, selection line) in 2:1 multiplexer is is also implemented using the proposed fanout in this work as shown in Fig. 27. The fault tolerance of the two multiplexer under single cell and double cell deposition defects are tabulated in Table 13. From the results, it is evident that the multiplexer in Fig. 25 is almost twice more fault tolerant than other one. This proves the superiority of proposed ft-Maj tile than that of orthogonal tile in [27]. The overall performance of different tiles implementing multiplexer is shown in Fig. 28. The proposed logic outperforms the conventional tiles showing high fault tolerance against cell deposition defect.

Table 13 Analysis of different 2:1 multiplexer

	2:1 MUX in Fig. 24		2:1 MUX in Fig. 25	
No of cells missing	1	2	1	2
No of defect patterns	27	108	117	2223
No of correct outputs	13	14	110	1749
No of faulty outputs	14	94	7	474
Fault tolerance (%)	48.14	12.96	94.02	78.68

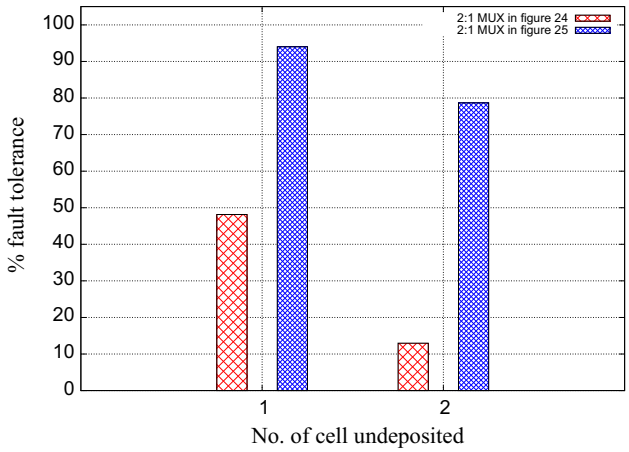

Fig. 28 Fault tolerance capability of multiplexer cell deposition defect

8 Simulation setup

The tiles and the circuits discussed in this paper are verified using QCADesigner ver. 2.0.3 [32]. In the Bistable approximation, we use the following parameters: cell size = 18 nm, dot size = 5 nm, cell separation = 10 nm, radius of effect = 65 nm, layer separation = 11.5 nm, number of samples = 128,000 and rest are set as default. In coherence vector, all the parameter are set as default.

9 Conclusion

In this paper, a fault tolerant architecture of majority logic in QCA, called ft-Maj, is explored based on hybrid cell orientation as applied to molecular QCA. The fault tol-

erance of fault tolerant majority tiles has been analysed under undeposited cell defects and an enviable fault tolerance of 97.43 % is achieved. Likewise, with the application of only two test vectors {001, 011} 100 % fault tolerance can be ascertained. The superiority of the ft-Maj is also established over existing tiles under multiple cell deposition defect.

Moreover, in the presence of multiple undeposited cells, ft-Maj have a high probability of performing some deterministic logic functions, even though it might be a different logic function (like, wire function, the inverting function, the majority-like functions) consistently appear at the output(s). Further, the fault tolerance of ft-Maj tile is extended to circuit-level by synthesizing double fanout tiles, triple fanout tiles and multiplexer using as a basic modular block. Finally, a fault tolerant minority logic has also been explored.

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