

# A new high-performance phototransistor design based on both surface texturization and graded gate doping engineering

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**Abstract** In this paper, we propose a new optically controlled field effect transistor, OC-FET, based on both surface texturization and graded gate doping engineering. The proposed design consists of a gate with both graded doping and surface texturization aspects to ensure high efficient light absorption and low dark current, respectively. Moreover, using an analytical investigation, an overall performance comparison of the proposed dual texturized gate (DTG) OC-FET device and conventional OC-FETs has been studied in order to confirm the enhanced optical and electrical performance of the proposed design in terms of increased photoresponsivity ( $R$ ), optical gain ( $G$ ),  $I_{ON}/I_{OFF}$  ratio, drain current driving capability ( $I_{DMAX}$ ) and high signal to noise ratio. Simulations show very good agreement between the results of the developed analytical models and those of TCAD software for wide range of design parameters. The developed analytical models are used to formulate the objective functions to optimize the device performance using a multi-objective genetic algorithm (MOGA). The proposed MOGA-based approach is used to search the optimal design parameters, for which the electrical and optical device performance is maximized. The obtained superior electrical performance suggests that our DTG OC-FET offers great promise as optical sensors and transducers for CMOS-based optical communications.

**Keywords** Phototransistor · Gate engineering · Texturization · MOGA · OC-FET

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## 1 Introduction

FET-based technology is a promising alternative to overcome the undesired high power consumption for high-performance submicron optical devices, due to the superior optical and electrical properties offered by CMOS technology both in analog as well as in digital applications [1–4]. High-performance phototransistors are required in order to improve the optical interconnection devices such as: emitters, receivers and optical insulators. Since appropriate wavelengths are used in optical communication (infrared and laser light), an optoelectronic circuit that is composed of an appropriate wavelength photosensor and a digital sub-circuit in one chip will be practical for high-performance CMOS-based optical communications. Although Germanium (Ge)-based materials have good performance in terms of high commutation speed and improved optical behavior, potential approaches to enhance the Ge-based devices for high frequency, optical communication applications and low power consumption are still worth investigating [1–6]. Furthermore, the high cost and complex fabrication process of the Ge-based devices limit their ability to develop high performance Integrated circuits (ICs) for Ge-based optical interconnects [5]. Therefore, Ge-based materials are preferred to be incorporated in photodetector devices with optical gain, such as phototransistors, where the transistor can be made using the Silicon (Si)-based technology. In this context, the conversion node between the two technologies (Si and Ge) is represented by near infrared and infrared Germanium on Si photodetectors, where several photodetectors have been reported and investigated during the last few years [1–6]. In these published works, each photodetector should be typically followed by a transimpedance amplifier and a limiting voltage amplifier to match the output voltage signal to the digital levels for the CMOS-based technology. However, this technique

is not suitable for high density and low cost optoelectronic devices because of the high power dissipation, which is mainly depending on the large number of the required transimpedance and voltage amplifiers. Recently, optically controlled field effect transistor, OC-FET, has been aggressively driven into submicron scales in order to achieve the desired improvement in drive current, low power consumption and operating speed [1,3]. Nevertheless, the developed OC-FET devices present the well-known problem of the low commutation speed and low optical gain, which can degrade the electrical and optical performance of the device. Most of the published works on OC-FETs mainly deal with the numerical simulation and experimental investigation of the single gate (SG) OC-FET structures, in which the gate consists of only one region *Ge* n type doping [1–8]. In these works, new numerical and design approaches have been proposed. Nevertheless, device engineering, optimization and comprehensive analytical investigation have not been fully investigated and there are still unsolved issues. Therefore, new materials, designs, modeling procedures and optimization approaches should be developed for the comprehension of the fundamentals of such device characteristics, in order to achieve a global view of OC-FETs performance under optical excitation.

In this paper, we analytically investigate and optimize a new dual texturized gate (DTG) OC-FET using multi-objective genetic algorithms (MOGAs) to improve the device performance, for high speed and low power consumption CMOS-based optical communications. The surface texturization engineering, adopted in our approach, has been widely used for improving solar cell's light trapping capability, where randomly and uniformly textured surfaces have been used and investigated for thin-film solar cell for many photovoltaic applications [9–12]. These textured surfaces are achieved through specified etching methods, where light can be trapped in the solar cell. To the best of our knowledge, no metaheuristic and analytical investigations are proposed to improve the phototransistor performance, taking into account the impact of both surface texturization and graded gate doping engineering on the device behavior. Therefore, in this work we provide an analytical modeling of the device, investigate the operation principles and optimize the proposed device performance versus design parameters, and operating conditions using MOGA-based computation.

## 2 Analytical modeling methodology

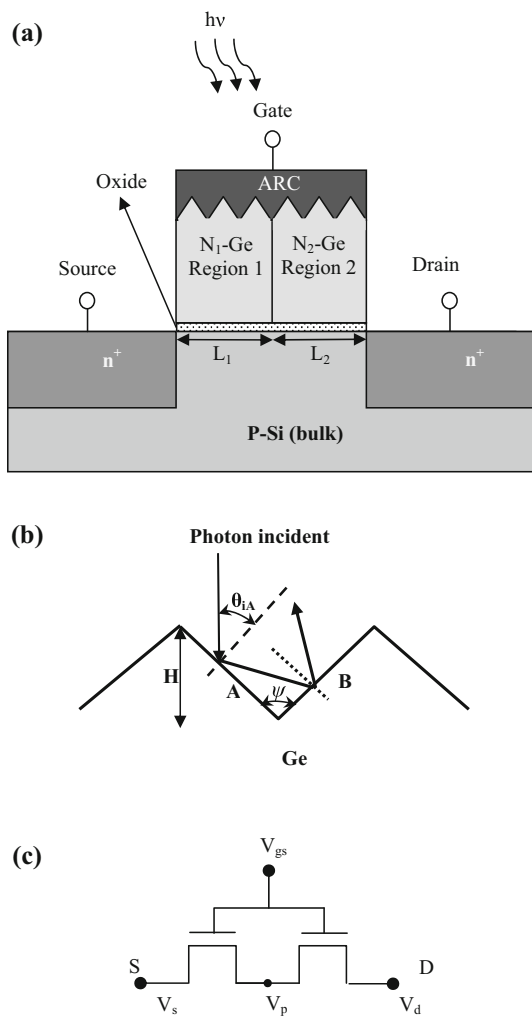
The investigated DTG OC-FET structure is shown in Fig. 1a. The gate is composed of two different *Ge* regions with two different doping concentrations, where the gate surface is texturized for both regions as it is shown in Fig. 1a. The Fig. 1b illustrates the schematic view of the *Ge* surface tex-

ture morphology assumed for our analytical investigation. It describes the triangular morphology characterized by angular parameters and deep sub-micrometric higher size. In Fig. 1b,  $\theta_{iA}$  presents the incident angle on the plan *A*,  $\psi$  is the texture angle and *H* presents the texture thickness. The *Ge*-based gate is illuminated at normal incidence with a monochromatic light at 1.55  $\mu\text{m}$ . For our analytical modeling, *d* represents the *Ge* layer thickness;  $L_1$  and  $L_2$  are the length of the first and second gate and region, respectively. *L* is the channel length;  $N_1$  and  $N_2$  represent the doping concentration of the first and second region, respectively.  $N_{ch}$  represents the silicon channel doping;  $N_{D/S}$  represents the doping concentration level of the drain/source region, respectively. The gate contacts are used to permit the voltage gate biasing  $V_{gs}$ . In this work, we focus on the role of new design parameters and operating conditions using an analytical modeling. Using an equivalent circuit analogy, the proposed DTG OC-FET device can be represented as a series combination of two SG MOSFETs with different material-gate work functions as shown in Fig. 1c. In order to understand various characteristics of the device under study, it is essential to develop a comprehensive drain current model in order to describe the device behavior against different optical and electrical design parameters.

From Fig. 1b, the surface texture is realized on the surface of the *Ge* layer (gate), where the texture morphology can be controlled by two parameters, which are: the texture angle ( $\psi$ ) and the texture thickness (*H*). The optical ray path for evaluating the reflection characteristics is shown for normal incidence (Fig. 1b). The incident light ray makes an angle with the texture front *A*. After the reflection from the plan *A*, the light beam is rereflected from front *B*. In our case, the net reflection coefficient *R*, after some mathematical manipulations, can be given by:

$$R(\psi, H) = \frac{r_{12}^2 + r_{23}^2 + 2r_{12}r_{23} \cos(2\beta)}{1 + r_{12}^2 r_{23}^2 + 2r_{12}r_{23} \cos(2\beta)} \quad (1)$$

with:  $\beta = \frac{2\pi n_i d}{\lambda}$  ( $i = 1 - 3$ ) and  $n_1, n_2$  and  $n_3$  are the refractive indices for air, anti-reflective layer and *Ge*, respectively, and *d* represents the thickness of the anti-reflective layer.  $r_{12}$  and  $r_{23}$  are optical parameters describe the mutual effect between different layers, which are mainly depending on surface texture morphology parameters ( $\psi$  and *H*), and  $\lambda$  represents the radiation wavelength. Using Snell-Descartes law for the investigated optical structure, and after some mathematical manipulations, the different parameters of Eq. 1 can be calculated (the detailed mathematical manipulations are given in our work [9]). The obtained reflection coefficient, *R*, will be used to calculate the photocurrent density generated in the *Ge* layer for each region, in order to study



**Fig. 1** **a** Cross-sectional view of the proposed DG OC-FET, **b** gate surface texture morphology, **c** equivalent circuit representation for a drain current modeling

the impact of the texturization parameters on the device performance.

Using the well-known drain current model of the conventional submicron Single Material Gate MOSFETs, the analytical drain current expression can be written [13] as

$$I_{ds} = \frac{W\mu_n C_{ox}}{L} \left( V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) V_{ds} \quad \text{for } V_{ds} < V_{gs} - V_{th} \tag{2a}$$

$$I_{ds} = \frac{W\mu_n C_{ox}}{L} (V_{gs} - V_{th})^2 (1 + \lambda_m V_{ds}) \quad \text{for } V_{ds} > V_{gs} - V_{th} \tag{2b}$$

where  $\mu_n$  represents the electron mobility in the Silicon channel region,  $C_{ox}$  is the oxide capacitance,  $L$  is the channel length,  $W$  represents the gate width,  $V_{ds}$  is the applied drain voltage,  $\lambda_m$  represents the channel length modulation coefficient and  $V_{th}$  represents the threshold voltage, which is given by:

$$V_{th} = V_{FB} + 2\psi_B + \frac{\sqrt{4\epsilon_{si}qN_{ch}\psi_B}}{C_{ox}} \tag{2c}$$

where  $\epsilon_{si}$  represents the silicon permittivity,  $q$  is the electron charge,  $\psi_B$  represents the Fermi potential level,  $N_{ch}$  represents the channel doping and  $V_{FB}$  is the flat band potential, which is given by:  $V_{FB} = \Phi_{MS} - V_{ph}$ , where  $\Phi_{MS}$  represents the difference between the silicon and germanium (gate) work functions. The optically induced voltage  $V_{ph}$ , produced in the photosensitive germanium gate by applying an input Light power  $P$ , can be calculated by following the modeling methodology used to calculate the open circuit voltage for the solar cell devices, where  $V_{ph}$  is similar to the open circuit voltage of an illuminated solar cell [1]. In this context, by applying the boundary conditions on the continuity equation at the surface  $x = 0$  (interface Ge/anti-reflective layer). In this region the recombination velocity ( $S_p$ ) can be calculated from  $D_p \frac{d(P_n - P_{n0})}{dx} = S_p (P_n - P_{n0})$  [14]. The second boundary condition should be applied at the interface between the germanium gate and oxide (interface Ge/SiO<sub>2</sub>), where the excess carrier density can be neglected ( $P_n - P_{n0} = 0$ ) [14], the final analytical expression of the photocurrent density can be found, after some mathematical manipulations, as

$$J_{ph} = \left[ \frac{q\phi(1-R)\alpha L_P}{(L_P^2\alpha^2 - 1)} \right] \times \left[ \frac{\left( \frac{S_p L_P}{D_p} + \alpha L_P \right) - \exp(-\alpha d) \left( \frac{S_p L_P}{D_p} \text{ch} \left( \frac{d}{L_P} \right) + \text{sh} \left( \frac{d}{L_P} \right) \right)}{\left( \frac{S_p L_P}{D_p} \right) \text{sh} \left( \frac{d}{L_P} \right) + \text{ch} \left( \frac{d}{L_P} \right)} \right] \left[ -\alpha L_P \exp(-\alpha d) \right] \tag{3a}$$

where  $L_P = \sqrt{D_p \tau_p}$ ,  $\tau_p$  is the free carrier life time,  $D_p$  represents the diffusion coefficient,  $R$  is the reflection coefficient, which is mainly depending on the texturization morphology and optical characteristics. The parameter  $d$  represents the germanium gate thickness and  $\phi$  is the number of the incident photons,  $\alpha$  represents the absorption coefficient, which is given by  $\alpha(\lambda) = \frac{C}{E(\lambda)} (E(\lambda) - E_{gGe})^{\frac{1}{2}}$ , with  $E_{gGe}$  is germanium band gap, and  $C$  is a fitting parameter [14].

From Eq. (3a) and after some mathematical manipulations, the optically induced voltage,  $V_{ph}$ , can be written as

$$V_{ph} = V_t \ln \left( \frac{J_{ph}}{J_s} \right) \tag{3b}$$

where  $J_s$  is the saturation current density and  $V_t$  represents the thermal voltage.

In the proposed DTG OC-FET we have two different regions, for which the work function for each region is given by  $\Phi_{MS1}$  and  $\Phi_{MS2}$ , respectively. Thus, the flat band potential  $V_{FB}$ , for each region, should be different and they are given by  $V_{FB1} = \Phi_{MS1} - V_{ph}$  and  $V_{FB2} = \Phi_{MS2} - V_{ph}$ .

From Fig. 1c, the applied drain voltage is given by  $V_{ds} = V_p + V_{dp}$ , where  $V_p$  represents the interface potential. Therefore, the drain current for each phototransistor can be derived, for the ohmic regime when  $V_{ds} < V_{gs} - V_{th}$ , using Eq. (2a) and the boundary condition, which satisfies the continuity of the drain current at the interface of two dissimilar germanium gate-doping regions, as

$$I_{ds1} = \frac{W\mu_n C_{ox}}{L_1} \left( V_{gs} - V_{th1} - \frac{V_p}{2} \right) V_p \tag{4a}$$

$$I_{ds2} = \frac{W\mu_n C_{ox}}{L_2} \left( V_{gs}^* - V_{th2} - \frac{(V_{ds} - V_p)}{2} \right) (V_{ds} - V_p) \tag{4b}$$

where  $V_{gs}^* = V_{gs} - V_p$

Using the boundary condition about the drain current expressions for each phototransistor ( $I_{ds1} = I_{ds2}$ ), the interfacial potential can be calculated from the following equation:

$$\eta_1 V_p^2 + \eta_2 V_p + \eta_3 = 0 \tag{5a}$$

where  $\eta_1, \eta_2$  and  $\eta_3$  are coefficients, which are mainly depending on the electrical, optical and geometrical parameters. The analytical solution of the Eq. 5 leads to:

$$V_p = \frac{-\left( V_{gs} \left( \frac{1}{L_1} + \frac{1}{L_2} \right) - \left( V_{th1} \frac{1}{L_1} + V_{th2} \frac{1}{L_2} \right) - V_{ds} \frac{1}{L_2} \right)}{\frac{1}{2} \left( \frac{1}{L_1} + \frac{1}{L_2} \right)} + \frac{\sqrt{\psi^*}}{\frac{1}{2} \left( \frac{1}{L_1} + \frac{1}{L_2} \right)} \tag{5b}$$

where  $\psi^*$  is an analytical function given by:

$$\psi^* = \left( \left( V_{gs} \left( \frac{1}{L_1} + \frac{1}{L_2} \right) - \left( V_{th1} \frac{1}{L_1} + V_{th2} \frac{1}{L_2} \right) - V_{ds} \frac{1}{L_2} \right) \right)^2 - 2 \left( \frac{1}{L_1} + \frac{1}{L_2} \right) \left( \frac{1}{L_2} \right) \left( V_{th2} V_{ds} - V_{gs} V_{ds} - \frac{1}{2} V_{ds}^2 \right) \tag{5c}$$

The transconductance ( $g_m$ ), which is an important parameter to evaluate the device performance, can be derived by differentiating  $I_{ds}$ , given in Eqs. (4a)–(4b), with respect to  $V_{gs}$ . The obtained analytical expression is given as

$$g_m = \frac{W\mu_n C_{ox}}{L_1} \left[ \frac{\partial V_p}{\partial V_{gs}} (V_{gs} - V_{th1} - 2V_p) + V_p \right] \tag{6a}$$

where  $\frac{\partial V_p}{\partial V_{gs}}$  is given by:

$$\frac{\partial V_p}{\partial V_{gs}} = \frac{\left( \frac{1}{L_1} + \frac{1}{L_2} \right)}{\left( \frac{-1}{L_1} + \frac{1}{L_2} \right)} + \frac{D}{\left( \frac{-1}{L_1} + \frac{1}{L_2} \right)} \tag{6b}$$

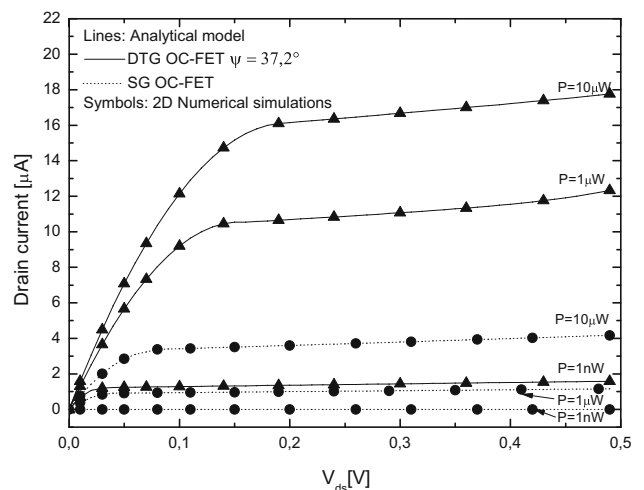
with

$$D = \frac{\left( V_{gs} \left( \frac{1}{L_1} + \frac{1}{L_2} \right) - \left( V_{th1} \frac{1}{L_1} + V_{th2} \frac{1}{L_2} \right) - V_{ds} \frac{1}{L_2} \right) + \left( \frac{-1}{L_1} + \frac{1}{L_2} \right) \left( \frac{-1}{L_2} V_{ds} \right)}{\sqrt{\psi^*}}$$

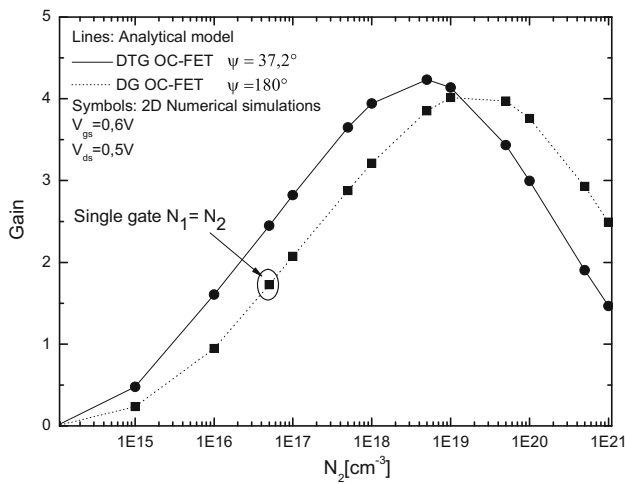
It is to note that the same methodology can be used to calculate the interfacial potential for saturation regime, where the condition  $V_{ds} > V_{gs} - V_{th}$  should be satisfied. In this context, the interfacial potential,  $V_p$ , can be determined according to the applied gate and drain voltages (saturation or ohmic working domain).

### 3 Results and discussions

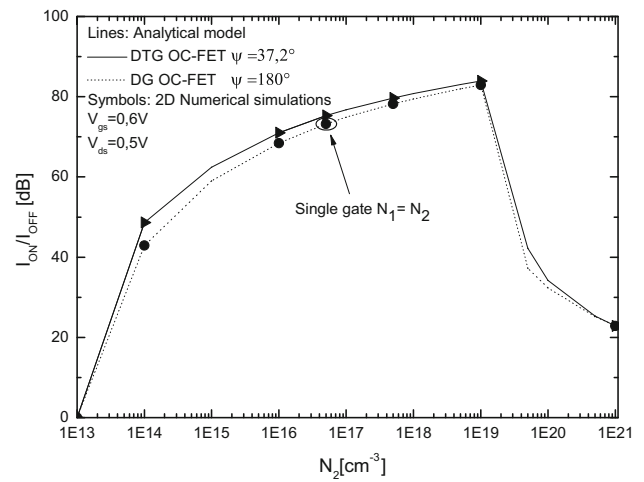
The DTG and conventional (SG) OC-FET devices are analyzed and compared in order to investigate the impact of the proposed design on the improvement of the device performance. The accuracy of the obtained analytical results is verified by comparison with the numerical simulation data using ATLAS 2D device simulator [15], where a good agreement is recorded as it is shown in Fig. 2. It is inferred from the figure that the analytical results for both designs (DTG and SG) agree well with the numerical results. It is to note that to enrich the numerical simulation in order to be very close to realistic behavior, additional effects and appropriate models are included in our numerical validation. As it is shown in Fig. 2, the obtained  $I - V$  characteristics are compared with that of the conventional SG OC-FET, where the texture angle ( $\psi$ ) fixed at  $37.2^\circ$ . It is clearly shown that the proposed DTG OC-FET device provides a better drain



**Fig. 2**  $I - V$  characteristics of the proposed DTG OC-FET compared with that of the conventional SG phototransistor for different optical powers, with  $N_1 = 5.10^{16} \text{ cm}^{-3}$ ,  $N_2 = 5.10^{17} \text{ cm}^{-3}$ , applied gate voltage  $V_{gs} = 0.6 \text{ V}$  and drain voltage  $V_{ds} = 0.5 \text{ V}$



**Fig. 3** Variation of the optical gain against the Ge doping concentration ( $N_2$ ) for different texture angles, with  $p = 10 \mu\text{W}$ ,  $t_{ox} = 5\text{nm}$ ,  $V_g = 0.6\text{V}$  and  $N_{ch} = 5 \times 10^{17} \text{cm}^{-3}$



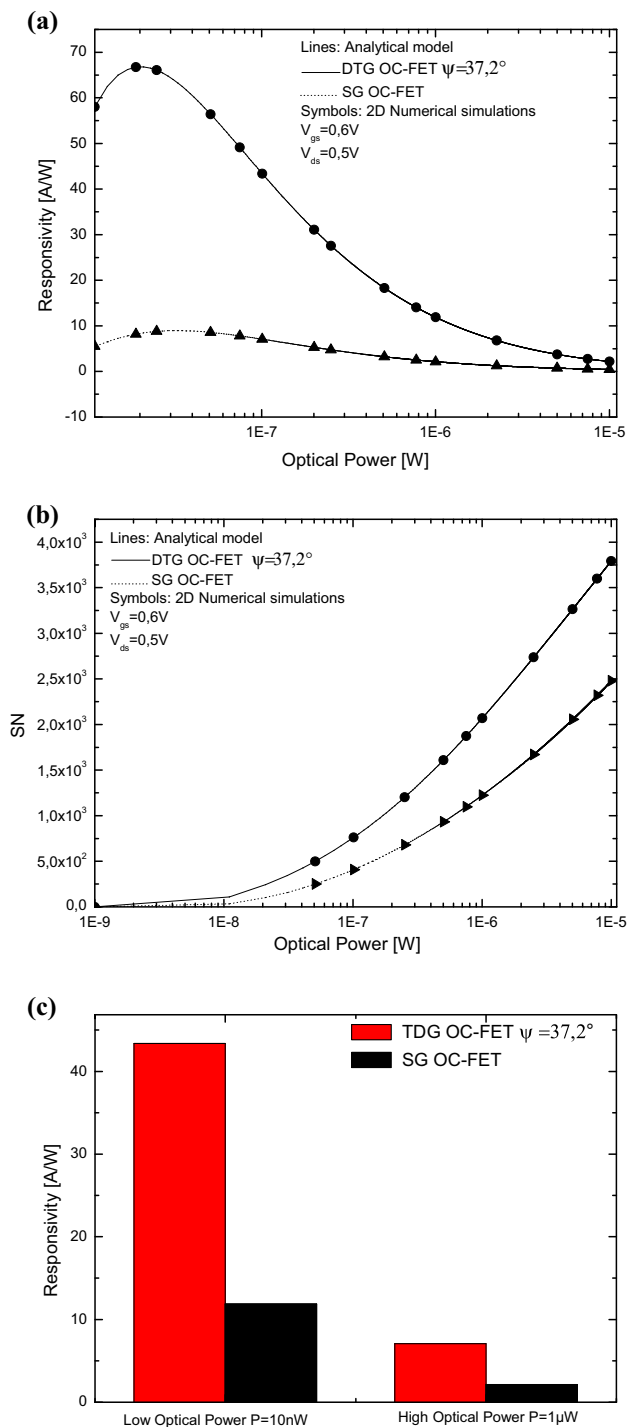
**Fig. 4** Variation of the  $I_{ON}/I_{OFF}$  ratio against the Ge doping concentration ( $N_2$ ), with  $N_1 = 5.10^{16} \text{cm}^{-3}$ ,  $V_{gs} = 0.6\text{V}$ ,  $V_{ds} = 0.5\text{V}$ ,  $L_1 = 0.1 \mu\text{m}$  and  $L_2 = 0.08 \mu\text{m}$

current behavior against the optical power. In dark working condition, the drain current is about  $0.1 \mu\text{A}$  at  $V_{ds} = 0.5\text{V}$ , while increases to  $18.5 \mu\text{A}$  for the same applied drain voltage at  $10 \mu\text{W}$  optical power, therefore, permitting an improvement of the device electrical performance in terms of power consumption and derived current, in comparison with the conventional SG OC-FET design. It is to note that the I–V characteristics are plotted for an applied gate voltage of  $V_g = 0.6\text{V}$ , where the photosensitive gate layer is illuminated at increasing optical power from  $1 \text{nW}$  up to  $10 \mu\text{W}$ . The recorded improvement in the drain current behavior can be explained by the discontinuity in the channel potential of the DTG OC-FET and the optical confinement caused by the surface texturization, where the peak electric field at the drain is decreased (while the potential at the source side under remains nearly constant) and the photogenerated current is increased substantially when compared with that of the conventional SG OC-FET. The improved electric field behavior leads to a reduced electron saturation velocity effect in the channel, and thus, the electron mobility in the channel and generated drain current will be augmented. The obtained results demonstrate that the DTG OC-FET design offers an important enhancement, especially, for high optical power values. Therefore, the proposed DTG OC-FET offers great promise as optical sensors, where high derived current and low device power consumption are required.

Figure 3 shows the variation of the optical gain against the second region Ge doping concentration ( $N_2$ ) for different texture angles, when a  $10 \mu\text{W}$  beam illuminates the both investigated OC-FETs (DTG and SG) with  $5 \text{nm}$  gate oxide,  $V_g = 0.6\text{V}$  and  $5 \times 10^{17} \text{cm}^{-3}$  Silicon channel doping concentration ( $N_{ch}$ ). The optical gain is calculated from an inverter gate, where the OC-FET is used as active load. In this

context, the optical gain can be calculated from:  $G = g_m/R_d$ , where  $R_d$  represents the drain resistance [16]. Moreover, the investigated inverter gate is excited by an input optical signal varied between  $1 \text{nW}$  and  $10 \mu\text{W}$ . In such conditions, the optical inverter gate provides an optimal gain value ( $G = 4.3$ ) for  $N_2 = 5.10^{18} \text{cm}^{-3}$  with an applied optical signal of  $10 \mu\text{W}$ . From Fig. 3, the device exhibits best performance when Ge doping is increased, where the optical gain reaches its optimal value,  $G = 4.3$ , for  $N_2 = 5.10^{18} \text{cm}^{-3}$ . Moreover, the proposed DTG OC-FET design exhibits better performance in comparison to the conventional SG OC-FET devices for wide range of  $N_2$ , thanks to the inclusion of the aspect of both gate engineering and gate surface texturization within MOS-based phototransistor.

Figure 4 plots the variation of the  $I_{ON}/I_{OFF}$  ratio (light/dark ratio) against the Ge doping concentration of the gate near the drain side ( $N_2$ ) at fixed first region doping concentration,  $N_1 = 5.10^{16} \text{cm}^{-3}$ , for:  $V_{gs} = 0.6\text{V}$ ,  $V_{ds} = 0.5\text{V}$ ,  $L_1 = 0.1$  and  $L_2 = 0.08 \mu\text{m}$ . In order to improve the OC-FET performance, the electric field at the drain side should be decreased. In this context, the high doping of the second gate region leads to decrease the electric field at the drain side, and therefore, the  $I_{ON}$  will be increased as it is shown in Fig. 4. Moreover, A Ge doping concentration lower than channel doping decreases the potential drop in the Ge gate decreasing the charge separation and providing a smaller voltage drop on the gate oxide. An optimal  $I_{ON}/I_{OFF}$  ratio value is recorded (82 dB) for  $N_2 = 10^{19} \text{cm}^{-3}$  with an applied optical signal of  $10 \mu\text{W}$ . A high  $I_{ON}/I_{OFF}$  ratio leads to increase the device sensitivity and decrease the device power consumption. Thus, the proposed design provides an optoelectronic device with high optical sensitivity and better power consumption behavior in comparison to that



**Fig. 5** Variation of the (a) responsivity and (b) signal to noise ratio as function of the applied optical powers, c Comparison between photoresponsivity obtained in low and high optical power regimes for both designs (SG and DTG OC-FETs) (Color figure online)

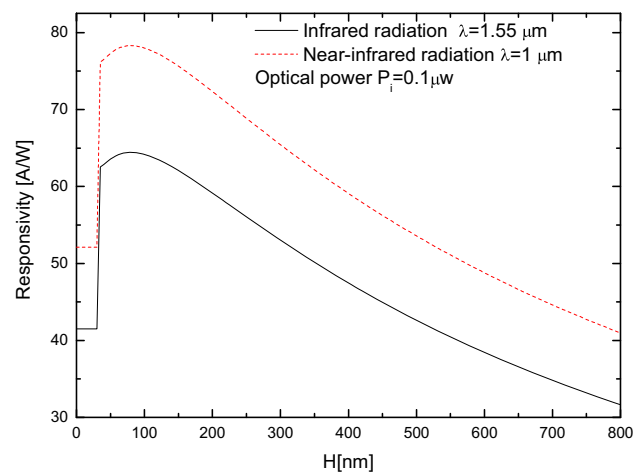
provided by the conventional SG OC-FET. For a phototransistor device, the responsivity  $R_{ph}$  and signal to noise ratio (SN) are two key parameters to characterize the device performance [14, 17].  $R_{ph}$  is defined by:

$$R_{ph} = \frac{I_{ON}(light) - I_{OFF}(dark)}{P} \tag{7a}$$

The signal to noise ratio (SN) is expressed by the following equation:

$$SN = \frac{I_{ON}(light) - I_{OFF}(dark)}{I_{OFF}(dark)} \tag{7b}$$

Based on the Eqs. (7a) and (7b), we calculated  $R_{ph}$  and SN of the proposed phototransistor design for power range of 1 nW – 10 μW with a monochromatic light at 1.55 μm, and they are plotted in Fig. 5. From Fig. 5, a high improvement is recorded for both factors of merit, where a high responsivity value is obtained for the proposed design at  $P = 10$  nW. The responsivity becomes more stable, when the applied optical power reaches 1 μW. Moreover, the signal to noise ratio is increased substantially when compared with that of the conventional SG OC-FET for full optical power range, where the optimal value of this factor of merit is recorded for optical power more than 1 μW. Contrary, the conventional SG OC-FET design exhibits low responsivity and signal to noise ratio values for the entire power range. In order to investigate the impact of our design on the photoresponsivity behavior, we propose to study the relative improvement of this figure of merit for high and low applied optical power as it is shown in Fig. 5c. From this figure, it is clearly shown that our design exhibits better photoresponsivity behavior for low applied optical power ( $P = 10$  nW) in comparison to that provided for high optical power value,  $P = 10$  μW. Therefore, the proposed design can be considered as potential candidate for low power communication systems, in which low optical power is required. Figure 6 plots the variation of the responsivity against the texture height values at fixed applied optical power,  $P = 0.1$  μW, for different



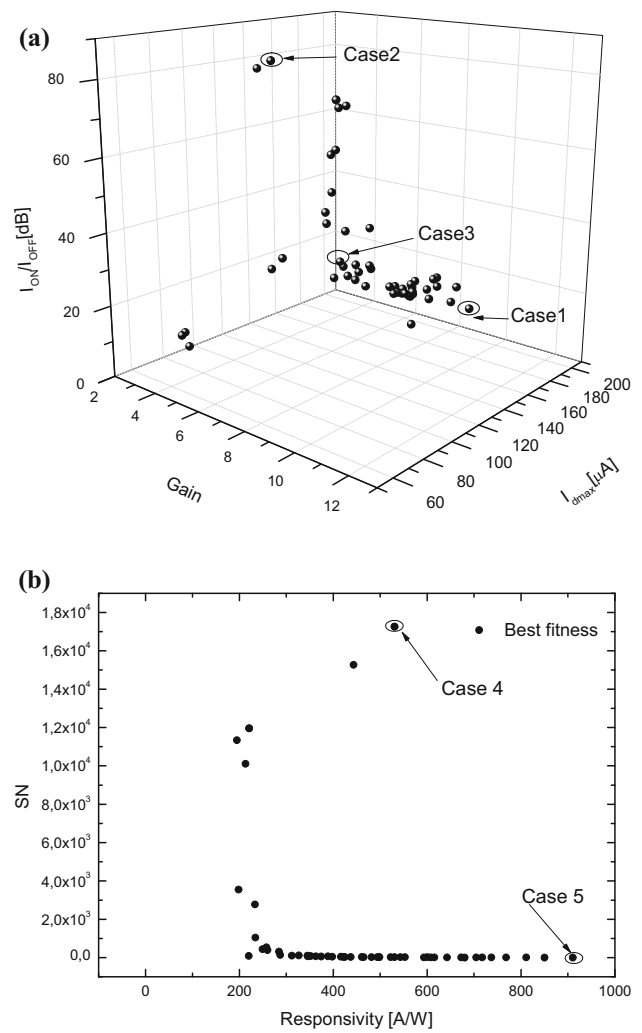
**Fig. 6** Variation of the responsivity as function of the texture height, H, for different applied radiation wavelengths (infrared and near-infrared radiations,  $\lambda = 1.55$  and 1 μm)

wavelength radiation values (near-infrared and infrared radiations). From this figure, it is clear shown that maximum responsivity values are recorded for both cases, where the maximum responsivity values are recorded at  $H = 80$  and  $90$  nm for  $\lambda = 1$  and  $1.55 \mu\text{m}$ , respectively. Moreover, phototransistor with surface texturization exhibits a significant performance enhancement over flat devices ( $H = 0$  nm) for both wavelength radiation values. At shorter wave lengths (near-infrared), optical absorption is high, leading to rapid decay of the incoming wave, as ti is plotted in Fig. 6. The enhancement observed at  $\lambda = 1 \mu\text{m}$  for responsivity of phototransistor with surface texturization is then primarily related to improved transmission of the front side in phototransistor device. The texturization morphology on the top side of the device thus acts as an anti-reflection layer. The comparison of phototransistors with surface texturization of varying texture height shows the complex dependence behavior of responsivity on texturization morphology. Therefore, the use of an adequate tool is crucial to optimize the device performance, taking into account the impact of surface texturization morphology.

The obtained result is strong signature of superior conversion of photons to electrons, thanks to the inclusion of gate surface texturization within MOS-based phototransistor design. The high performance provided by the proposed design can be explained by two mechanisms: (1) illumination that generates electron-hole pairs both within Ge gate, where the light is confined because of the gate surface texturization, and the Si channel. (2) enhanced photoconductive and photovoltaic effects by the presence of high doping gate region.

### 3.1 MOGA-based optimization of DTG OC-FET design

Recently, the MOGA-based optimization techniques are widely used in several engineering applications to investigate and optimize complex nonlinear and systems [18–22]. The MOGA-based computation is defined as such when the aim is to find acceptable values for all objective functions satisfying required constraints. The MOGAs differ from most optimization techniques because of their global searching offered by one population of solutions instead of one single solution. In MOGA-based computation, the objective functions (fitness) are required to be maximized and/ or minimized simultaneously. So, the aim of multi-objective optimization procedure is to find some optimal solutions corresponding to multiple objectives considered in research space. In this way, the designer can choose the most suitable solution by using higher level information. Due to the simple implementation and high versatility provided by MOGA-based approach for multi-objective global optimization, MOGA can be applied to investigate and optimize the DTG OC-FET performances.



**Fig. 7** Pareto-optimal solutions of the investigated DTG OC-FET

In our work, five objective functions, which affect the phototransistor performance, are considered in this study, i.e. Photoresponsivity ( $R_{ph}$ ), optical gain ( $G$ ),  $I_{ON}/I_{OFF}$  ratio, drain current driving capability ( $I_{D_{MAX}}$ ) and high signal to noise ratio (SN). Pareto approach has been considered a suitable choice for our design. Pareto approach searches non-dominant solutions called Pareto optimal solutions in the objective space. The main objective of this investigation is to find the optimal design of the proposed DTG OC-FET device. Therefore, the DTG OC-FET will be optimized with respect to the following criteria:

- Maximization of the Photoresponsivity,  $R_{ph}(X)$ .
- Maximization of the optical gain,  $G(X)$ .
- Maximization of the  $I_{ON}/I_{OFF}$  ratio,  $I_{ON}/I_{OFF}(X)$ .
- Maximization of the derived drain current,  $I_{D_{MAX}}(X)$ .
- Maximization of the signal to noise ratio,  $SN(X)$ .

where  $X$  represents the design variables vector, which is given by:  $X=(\psi, H, h, N_1, N_2, L_1, L_2, N_{ch}, t_{ox}, V_{gs}, V_{ds})$ .

**Table 1** Optimized DTG OC-FET design

Symbol	Case 1	Case 2	Case 3	Case 4	Case 5
Objective functions					
Optical gain ( $G$ )	11.26	6.0	7.85	6.2	4.6
Drain current Ratio ( $I_{ON}/I_{OFF}$ )(dB)	33.49	84.74	17.85	83.68	11.81
Derived drain current $I_{D_{MAX}}$ ( $\mu$ A)	104	99.2	190	83.68	64.4
Responsivity ( $A/W$ )	46.3	443.24	6.80	530.79	2.89
SN	397.66	15260	811.19	17276	911.25

**Table 2** Comparison between the optimized DTG OC-FET and conventional OC-FET design parameters for different texture numbers (m)

Symbol	Conventional SG OC-FET design [1, 4]	Optimized DTG OC-FET with (m = 5)	Optimized DTG OC-FET with (m = 3)
Design variables			
Channel length $L$ (nm)	180	138	138
Channel length for first region $L_1$ (nm)	–	75.2	75.2
Channel length for second region $L_2$ (nm)	–	62.77	62.77
Oxide thickness $t_{ox}$ (nm)	4	4	4
Ge doping concentration $N_d$ ( $\text{cm}^{-3}$ )	$2.10^{17}$	–	–
Channel doping concentration $N_{ch}$ ( $\text{cm}^{-3}$ )	$2.10^{17}$	$2.2.10^{16}$	$2.2.10^{16}$
First region Ge doping concentration $N_1$ ( $\text{cm}^{-3}$ )	–	$5.10^{16}$	$5.10^{16}$
Second region Ge doping concentration $N_2$ ( $\text{cm}^{-3}$ )	–	$1.10^{18}$	$1.10^{18}$
Drain voltage $V_{ds}$ (V)	0.5	0.15	0.15
Gate voltage $V_{gs}$ (V)	0.6	0.3	0.3
Angle of texturation ( $^\circ$ )	–	$47.3^\circ$	$47.3^\circ$
Texturation thickness (nm)	–	68	105
Gate Ge thickness $d$ (nm)	200	260	260
Objective functions			
Optical gain ( $G$ )	2.9	8.70	8.70
Drain current ratio ( $I_{ON}/I_{OFF}$ ) (dB)	70	83	83
Derived drain current $I_{D_{MAX}}$ ( $\mu$ A)	13	71.60	71.60
Responsivity ( $A/W$ )	–	221	221
SN	–	12,625	12,625

The constraints to be satisfied are:

- $g_1(x) : x \in [x_{i \min}, x_{i \max}]$ ,  $x_i \in X$  (each design variable should be confined within a given range).
- $g_2(x) : N_2 > N_1$ .
- $g_3(x) : L_1 + L_2 = L$ .

For the implementation of the MOGA-based computation, tournament selection is employed to select the best individual out of that set to be a parent. Scattered crossover creates a random binary vector, it then selects the genes where the vector is unity from the first parent, and the genes where the vector is zero from the second parent, and combines the genes to form the child. An optimization process was performed for 20 population size and maximum number of generations equals to 1000, for which stabilization of

the objective functions was recorded. The MOGA parameters were varied and the associated optimization error was recorded. For our MOGA-based computation, the optimum solutions are given as 'Pareto Front'. These solutions correspond to the non-dominated individuals, which present the best solutions of the objective functions simultaneously. Figure 7 shows the surface representing the Pareto Front, in this Figure each point represents the value of the objective function provided by a given design parameter, DTG OC-FET configuration. Five selected points are shown in Fig. 7 and the corresponding DTG OC-FET design parameters are given in Table 1. It is clearly shown that the presented possible solutions in the Pareto Front can be considered as an important guideline tool for the designer. Furthermore, we can notice that these optimal solutions present the advantage of having the better device performance, for which the



five objective functions are maximized. Table 1 illustrates the five extreme cases in the design space. Each case is associated to the maximum objective function (device performance). For example, in case 1, there is the optimal value of the photoresponsivity,  $R_{ph}(X) = 530$ , but other objective functions acquire the worst values. Therefore, we can notice that a high improvement in the photoresponsivity can be obtained with sacrificing at least one parameter. Moreover, the results obtained from Pareto Front region enable to the designer to obtain a comprehensive summary of the design tradeoffs, with respect of the different device figures of merit.

It is to note that if the five objective functions have the same required performance weight by the device designer, the multiobjective problem should be transferred to a mono-objective-based optimization. In this case, the overall mono-objective function is obtained by a given weightage based on the “weighted sum approach method” as follows:

$$F(X) = w_1G + w_2(I_{ON}/I_{OFF}) + w_3I_{DMAX} + w_4R_{ph} + w_5SN \quad (8)$$

where  $w_i (i = 1-5)$  can be assigned equal values as  $1/5$ .

The final optimized DTG OC-FET parameters are summarized in Table 2 for two different number of triangular texturization values ( $m = 5$  and  $3$ ), which is the number of triangles provided by the textured surface (Fig. 1a). From this table, it is clearly demonstrated that our optimized device provides better performance in comparison to the conventional SG OC-FET structures, in terms of electrical and optical performances.

## 4 Conclusion

In this paper, a new high-performance DTG OC-FET phototransistor design has been proposed in a CMOS compatible technology. The proposed DTG OC-FET phototransistor exhibits a significant improvement in photocurrent, in power consumption and in high photoresponsivity behavior, thanks to the improved channel electric field and to the light confinement at the texturized gate surface based on both photovoltaic and photoconductive effects. In addition, new MOGA-based technique is proposed to optimize and improve the optical and electrical performance of the proposed DTG OC-FET. The proposed technique has successfully searched the better possible performance and the design parameters that can yield this specific performance. The obtained results demonstrate that the proposed approach is very useful in developing high-performance CMOS-based optoelectronic devices for future optical interconnection applications.

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