J Comput Electron (2016) 15:45–52
DOI 10.1007/s10825-015-0723-z

A surface-potential based drain current model for short-channel symmetric double-gate junctionless transistor

Ratul Kumar Baruah[1,2] · **Roy P. Paily**[1,3]

Published online: 19 July 2015

Abstract Junctionless transistors, which do not have any pn junction in the source-channel-drain path have become an attractive candidate in sub-20 nm regime. They have homogeneous and uniform doping in source-channel-drain region. Despite some similarities with conventional MOSFETs, the charge-potential relationship is quite different in a junctionless transistor, due to its different operational principle. In this report, models for potential and drain current are formulated for shorter channel symmetric double-gate junctionless transistor (DGJLT). The potential model is derived from two dimensional Poisson's equation using "variable separation technique". The developed model captures the physics in all regions of device operation i.e., depletion to accumulation region without any fitting parameter. The model is valid for a range of channel doping concentrations, channel thickness and channel length. Threshold voltage and drain-induced barrier lowering values are extracted from the potential model. The model is in good agreement with professional TCAD simulation results.

Keywords Analytical model · Double-gate junctionless transistor (DGJLT) · Drain current · Surface potential · Short channel effect (SCE)

✉ Ratul Kumar Baruah
r.baruah@iitg.ernet.in; ratulkr@tezu.ernet.in

[1] Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati, Guwahati 781039, India

[2] Department of Electronics and Communication Engineering, Tezpur University, Assam 784028, India

[3] Centre for Nanotechnology, Indian Institute of Technology Guwahati, Guwahati 781039, India

1 Introduction

Junctionless transistors (JLT) avoid the ultrahigh doping concentration gradients at the junctions and high thermal budgets, and hence their fabrication steps are comparatively easier than junction-based metal oxide field-oxide transistors (JB MOSFETs). They offer low OFF-state currents and hence can be scaled to lower channel lengths compared to JB MOSFETs. JLT has near ideal subthreshold slope (SS ∼60 mV/dec), high ON-state to OFF-state current ratio ($I_{ON}/I_{OFF} > 10^7$), low drain induced barrier lowering etc. There is less degradation of mobility with gate voltage and temperature in JLT than classical transistors [1]. The transconductance in junctionless (JL) transistor is however lesser compared to JB transistor. Device variability and the parasitic source/drain resistances are acknowledged as important limitations of the JL nanowire field-effect transistors [2].

The working physics of a DGJLT is different from JB MOSFET counterpart. A cross-sectional view of symmetric n-channel DGJLT is shown in Fig. 1. JLT has highly doped ($\sim 8 \times 10^{18} - 8 \times 10^{19}$ cm^{-3}) channel to have desirable threshold voltage (V_T). Also, to have full depletion in the subthreshold region, channel should be adequately thin. For gate voltage $V_{GS} < V_T$, the channel of a DGJLT is fully depleted. When V_{GS} exceeds V_T, the channel becomes partially depleted. When V_{GS} = flat band voltage (V_{FB}), bulk current flows and on further increasing V_{GS}, surface current dominates in the channel current [3].

Looking at the low leakage currents and many advantages as mentioned above, a JLT can be a prospective candidate for low power circuit design applications in future technology nodes, and therefore, an analytical compact model of junctionless transistor is sought after. Since the device physics of DGJLT is fundamentally different than the JB

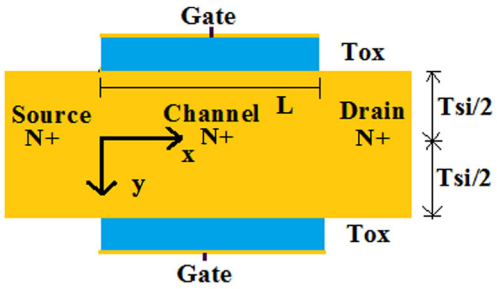

Fig. 1 Cross-sectional view of symmetric n-channel double-gate junctionless transistor (DGJLT)

MOSFETs [1], the existing models for DG JB MOSFETs do not directly apply. There are many reports on analytical/semi-analytical modelling for potential and drain current either for long-channel or short-channel length junctionless transistor in double-gate, trigate or gate-all-around architecture till date [2–27]. Some of them are valid only in subthreshold region and some are applicable from subthreshold to accumulation region. There are few potential models for shorter channel length double-gate junctionless transistors which are valid in subthreshold region only. Jiang et al. proposed a physics-based analytical model of electrostatic potential for short-channel junctionless double-gate MOSFETs (JLDGMTs) operated in the subthreshold regime only, by solving 2D Poisson's equation in channel region using method of series expansion similar to Green's function. Jin et al. derived potential model by solving 2-D Poisson's equation using "variable separation technique" for deep nanoscale short channel asymmetric junctionless double-gate MOSFETs valid in the subthreshold region. Holtij et al. reported analytical 2D potential model within ultra-scaled junctionless double-gate MOSFETs valid in the subthreshold regime using the Schwarz–Christoffel transformation. Also, some of the models are developed piecewise (region-wise) and some are non-piecewise. Accurate potential and drain current models, valid from depletion to accumulation regions of operation, for shorter channel length double-gate junctionless transistor, are still rare in literature. In this work, potential and drain current models, covering all regions of operation, are targeted for a shorter channel length double-gate junctionless transistor (DGJLT). A two-part approach, known as the "variable separation technique" is applied to derive the channel potential, in which the total potential is divided into long channel part and short channel part. Such a method gives quite accurate results in short channel regime, because, while deriving the short channel part of potential, one can include a large set of eigen values and details will be presented later in Sect. 2.2. In this work, we have obtained good accuracy with two eigen values, however, if more number of iterations are used, correspondingly, the simulation time may increase. Threshold voltage and drain induced barrier lowering (*DIBL*) parameters are extracted from the model. The potential model as well as the extracted parameters is then compared to professional TCAD simulation results.

2 Potential model derivation

The Poisson's equation considering both fixed and mobile charges in the silicon region can be written as

$$\frac{d^2\Psi(x,y)}{dx^2}+\frac{d^2\Psi(x,y)}{dy^2}=\frac{qN_D}{\varepsilon_{si}}\left(e^{(\Psi(x,y)-V)/U_T}-1\right) \tag{1}$$

where, $\Psi(x,y)$ is the channel potential, ε_{si} is the permittivity of silicon, V is electron quasi-Fermi potential, $U_T=kT/q$ is the thermal voltage, N_D is the channel doping concentration and q is the charge of electron. Hole density is neglected as compared to electron density. The coordinates, x and y are as shown in Fig 1. Equation (1) has no direct analytical solution. One way to solve (1) is variable separation technique, which states that the total potential can be divided into long channel part (1D) and short channel part (2D) *i.e.*,

$$\Psi(x,y)=\Psi_I(y)+\Psi_{II}(x,y) \tag{2}$$

where, $\Psi_I(y)$ is the potential which is related to only y direction (long channel part) and $\Psi_{II}(x,y)$ is the potential variation related to both x and y directions (short channel part) with boundary conditions, as stated below.

2.1 Expression for $\Psi_I(y)$

$\Psi_I(y)$ is expressed as

$$\frac{d^2\Psi_I}{dy^2}=\frac{qN_D}{\varepsilon_{si}}\left(e^{(\Psi(y)-V)/U_T}-1\right) \tag{3}$$

with boundary conditions

$$\left.\frac{\partial\Psi}{\partial y}\right|_{y=\pm\frac{T_{si}}{2}}=\Psi_S=\frac{C_{ox}}{\varepsilon_{si}}\left(V_{GS}-V_{FB}-\Psi\left(\frac{T_{si}}{2}\right)\right)$$
$$\left.\frac{\partial\Psi}{\partial y}\right|_{y=0}=0 \tag{4}$$

Equation (4) has no closed form solution even though it looks simple. Integrating (4), we obtain

$$E_S^2=\frac{2qN_DU_T}{\varepsilon_{si}}\left[e^{(\Psi_S-V)/U_T}-e^{(\Psi_0-V)/U_T}-\left(\frac{\Psi_S-\Psi_0}{U_T}\right)\right] \tag{5}$$

where, Ψ_S and Ψ_0 are the potentials at the surface and centre of the channel respectively. Thus, once the relation between Ψ_S and Ψ_0 is known, the potential at any point in the silicon body can be determined. The Gauss's law connects the surface potential with gate voltage as

$$Q_{SC} = -2\varepsilon_{si}\left.\frac{d\Psi}{dx}\right|_{x=\pm\frac{T_{si}}{2}} = -2C_{ox}(V_G - V_{FB} - \Psi_S) \quad (6)$$

Q_{SC} being the space charge density per unit area, $C_{ox} = \varepsilon_{ox}/T_{ox}$ is the oxide capacitance, V_{FB} is the flat band voltage. Combining (5) and (6)

$$(V_G - V_{FB} - \Psi_S)^2 = \frac{2qN_D\varepsilon_{si}U_T}{C_{ox}^2}\left[e^{(\Psi_S - V)/U_T} - e^{(\Psi_0 - V)/U_T} - \left(\frac{\Psi_S - \Psi_0}{U_T}\right)\right] \quad (7)$$

(a) For depletion region ($V_{FB} < V_G < V_{FB} + V_{DS}$) *with* $V_{DS} > 0$, after some mathematical reformulations, the Eq. (7) can be written as [4]

$$\psi_S = V_G - V_{TH} - \frac{qN_DT_{si}}{8C_{si}} - V_T Lambertw\left[\frac{qN_DT_{si}}{4C_{ox}U_T}e^{(V_G - V_{TH} - V)/U_T}\right] \quad (8)$$

where, Lambertw is the Lambert W-function, which is the inverse of the function $z = W(z) \times e^{W(z)}$. V_T is the threshold voltage and $(\Psi_0 - \Psi_S)$ is the difference between centre and surface potentials, given by,

$$V_T = V_{FB} - qN_DT_{si}/2C_{eff}$$
$$C_{eff}^{-1} = (4C_{si})^{-1} + (C_{ox})^{-1},\ C_{si} = \varepsilon_{si}/T_{si}$$
$$\Psi_0 - \Psi_S = qN_DT_{si}^2/8\varepsilon_{si} \quad (9)$$

The expression of V_T in (9) is valid when channel length is higher. The V_T for shorter-channel device is given in Sect. 2.3.

(b) For accumulation region ($V_G > V_{FB} + V_{DS}$)

The relation between centre and surface potentials $\{\Psi_S - \Psi_0\ (= \alpha, \text{say})\}$ is given by [5]

$$\Psi_S - \Psi_0 = \frac{qN_DT_{si}^2}{8\varepsilon_{si}}\left(e^{\frac{\Psi_0 - V}{U_T}} - 1\right) \quad (10)$$

Equation (10) can also be expressed as [17]

$$\Psi_S - \Psi_0 = -\frac{qN_DT_{si}}{8C_{si}} + U_T Lambertw\left[\frac{qN_DT_{si}}{8C_{si}U_T}e^{\frac{qN_DT_{si}}{8C_{si}U_T}}e^{\frac{\Psi_S - V}{U_T}}\right] \quad (11)$$

Now, using (7) and (11), the relation between surface potential with gate voltage can be obtained as [17]

$$(V_G - V_{FB} - \Psi_S)^2 = sign(\alpha)\left(\frac{q^2N_D^2T_{si}\varepsilon_{si}}{C_{ox}^3}\right) \times \left[e^{(\Psi_S - V)/U_T} - 1 - \left(1 + \frac{8C_{si}U_T}{qN_DT_{si}}\right) \times \left\{-\frac{qN_DT_{si}}{8C_{si}U_T} + Lambertw\left[\frac{qN_DT_{si}}{8C_{si}U_T}e^{\frac{qN_DT_{si}}{8C_{si}U_T}}e^{\frac{\Psi_S - V}{U_T}}\right]\right\}\right] \quad (12)$$

For accumulation region ($V_{GS} > V_{FB} + V_D$), $\alpha > 0$. Equation (12) can be solved numerically. The centre potential can be derived using Eqs. (8)–(12), as explained in [18].

2.2 Expression for $\Psi_{II}(x, y)$

$\Psi_{II}(x, y)$ is expressed as

$$\frac{d^2\Psi_{II}(x, y)}{dx^2} + \frac{d^2\Psi_{II}(x, y)}{dy^2} = 0 \quad (13)$$

with the boundary conditions

$$\Psi_{II}(0, y) = V_{bi} - \Psi_I(y)$$
$$\Psi_{II}(L, y) = V_{DS} + V_{bi} - \Psi_I(y)$$
$$\varepsilon_{si}\frac{\partial\Psi_{II}\,(T_{si}/2, x)}{\partial x} = -C_{ox}\Psi_{II}\left(\frac{T_{si}}{2}, x\right)$$
$$\left.\frac{\partial\Psi_{II}}{\partial y}\right|_{y=0} = 0 \quad (14)$$

Equation (13) is a mixed boundary value problem and it is already solved by many groups [28,29]. The final solution is

$$\Psi_{II}(x, y) = \left\{A_0e^{\frac{2\mu_n(x-L)}{T_{si}}} + A_1e^{-\frac{2\mu_nx}{T_{si}}}\right\} \times \cos(\mu_n y) \quad (15)$$

where,

$$A_0 = B_1\left[V_{DS} + V_{bi}\left(1 - e^{-\frac{2\mu_nL}{T_{si}}}\right)\right] - B_2\Psi_{S(\text{Long})}$$
$$A_1 = B_1\left[V_{bi}\left(1 - e^{-\frac{2\mu_nL}{T_{si}}}\right) - V_{DS}e^{-\frac{2\mu_nL}{T_{si}}}\right] - B_2\Psi_{S(\text{Long})} \quad (16)$$

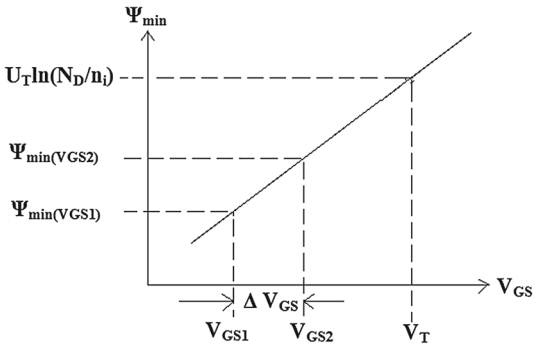

Fig. 2 Schematic plan for calculating the threshold voltage. Here, $V_T = V_{GS}$ at $U_T ln(N_D/n_i) = \Psi_{\min}$ and ΔV_{GS} is the difference between two voltages in the subthreshold region

$$B_1 = \frac{4 \times Sin(\mu_n)}{2\mu_n + Sin(2\mu_n)\left(1 - e^{-\frac{2\mu_n L}{T_{si}}}\right)},$$
$$B_2 = \frac{4\mu_n \times Cos\left(\frac{\mu_n}{2}\right)\left(1 - e^{-\frac{2\mu_n L}{T_{si}}}\right)}{2\mu_n + Sin(2\mu_n)\left(1 - e^{-\frac{2\mu_n L}{T_{si}}}\right)} \quad (17)$$

$\Psi_{S(\text{Long})}$ is the long channel surface potential. The eigenvalue μ_n is the periodic n$^{\text{th}}$ root of this equation and is determined using the permittivity and thickness values of both silicon and oxide. It can have infinite possible values for μ, however, first 1-2 iteration(s) give quite good result.

$$2\mu_n \tan(\mu_n) = \frac{\varepsilon_{ox} T_{si}}{T_{ox} \varepsilon_{si}} \quad (18)$$

Now, putting the expressions of $\Psi_I(y)$ and $\Psi_{II}(x, y)$ in Eq. (2), the total potential in the channel region of a shorter channel DGJLT can be determined.

2.3 Threshold voltage and DIBL value extraction

A schematic plan for calculating the threshold voltage (V_T) is given in Fig. 2. The threshold voltage is given by the following expression, and it is valid for longer as well as shorter channel length devices [30]

$$V_T = V_{GS} + \Delta V_{GS}\left(\frac{U_T \ln(N_D/n_i) - \Psi_{\min(V_{GS1})}}{\Psi_{\min(V_{GS2})} - \Psi_{\min(V_{GS1})}}\right) \quad (19)$$

$\Psi_{\min(V_{GS1})}$ and $\Psi_{\min(V_{GS1})}$ are the minimum potentials at two gate-to-source voltages V_{GS1} and V_{GS2}. Assuming a linear relationship between $\Psi_{\min}$ and V_{GS}, in the subthreshold region, threshold voltage can be extracted using (13).

Drain induced barrier lowering (*DIBL*) is defined as the change in threshold voltage when drain voltage changes from 50 mV to 1 V *i.e.*,

$$DIBL = V_T|_{V_{DS}=50mV} - V_T|_{V_{DS}=1V} \quad (20)$$

2.4 Discussion and verification of model

To validate the model results, they are compared with electrical characteristics of the devices simulated using 2D ATLAS device simulator with version 5.19.20.R [31]. Lombardi mobility model is employed, accounting for the dependence on the impurity concentrations as well as the transverse and longitudinal electric field values. Shockley-Read-Hall (SRH) recombination model is included in the simulation to account for leakage currents. Because of high channel doping concentration, Fermi-Dirac carrier statistics without impact ionization is utilized in the simulations. Band gap

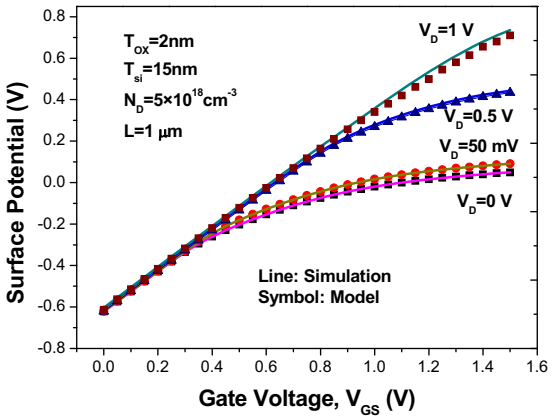

Fig. 3 Surface potential with respect to gate voltage near the drain side for $V_D = 0$ V, 50 mV, 0.5 V and 1 V. $L = 1$ μm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $N_D = 5 \times 10^{18}$ cm^{-3} and source/drain extension length = 50 nm. Flat band voltage (V_{FB}) considered is ~1.1 eV

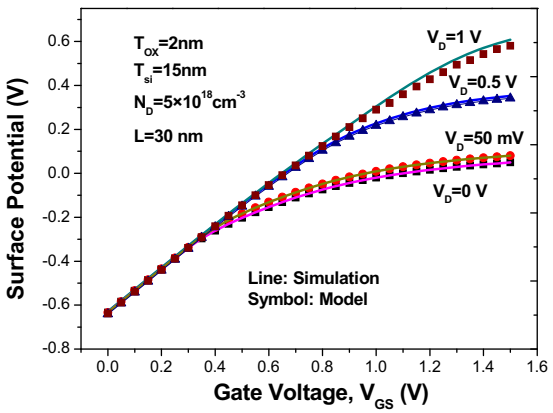

Fig. 4 Surface potential with respect to gate voltage near the drain side for $V_D = 0$ V, 50 mV, 0.5 V and 1 V. $L = 30$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $N_D = 5 \times 10^{18}$ cm^{-3} and source/drain extension length = 10 nm. Flat band voltage (V_{FB}) considered is ~1.1 eV

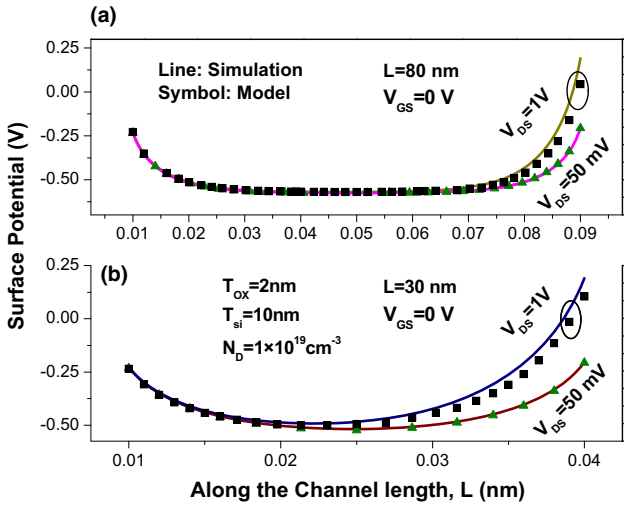

Fig. 5 Surface potential along the channel for **a** $L = 80$ nm (long channel) at $V_D = 50$ mV, 1 V, **b** $L = 30$ nm (short channel). $T_{si} = 10$ nm, $T_{ox} = 2$ nm, $N_D = 1 \times 10^{19}$ cm^{-3}, $V_{GS} = 0$ V and source/drain extension length=10 nm. Flat band voltage (V_{FB}) considered is ∼1.1 eV

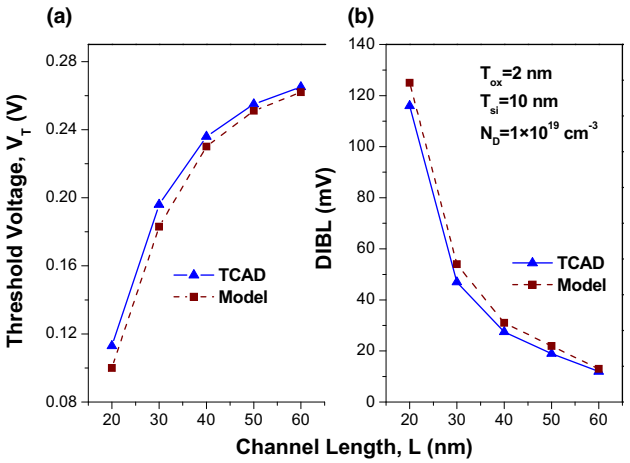

Fig. 6 **a** Threshold voltage (V_T) at $V_{DS} = 50$ mV for L = 20 to 60 nm, **b** drain induced barrier lowering (*DIBL*) for $L = 20$ to 60 nm. $T_{si} = 10$ nm, $T_{ox} = 2$ nm, $N_D = 1 \times 10^{19}$ cm^{-3}

narrowing model (BGN) is also incorporated to take care of the band gap narrowing effect which may arise due to highly doped channel regions. Quantum effect is not considered here. Channel doping concentration N_D of 5×10^{18} and 1×10^{19} cm^{-3}, equivalent gate oxide thickness (*EOT*) = 2 nm, silicon thickness (T_{si}) = 10, 15 nm are considered for TCAD simulation. Channel width (W) is 1μm. In addition, p-type polysilicon is used having doping concentration 10^{20} cm^{-3}. The interface charge concentration (N_{SS}) is considered as 5×10^{10} cm^{-3}. A constant mobility (μ_e) of 100 cm^2/V.s is assumed. For channel length of 1 μm, source/drain extension length (L_S/L_D) is taken as 50 nm; and for channel length of 30 nm-80 nm, L_S/L_D is taken as 10 nm to avoid parasitic resistance effect. Calculations are done on Mathematica computational software. Figure 3 shows the surface potential with respect to gate voltage, for different values of $V_D = 0$ V, 50 mV, 0.5 V and 1 V respectively for a channel length of 1 μm. The simulation and model curves are in close agreement. Figure 4 shows the surface potential with respect to gate voltage, for different values of $V_D = 0$ V, 50 mV, 0.5 V and 1 V respectively for a channel length of 30 nm. The marginal difference may be due to the inclusion of source and drain extension resistances in TCAD characteristics; and the exclusion of fringing electric fields in the model. Figure 5a, b shows the potential along the channel direction, 0.5 nm away from the Si-SiO_2 interface, at $V_{DS} = 50$ mV and 1 V respectively keeping $V_{GS} = 0$ V for gate lengths of 80 and 30 nm. Both the simulation and model plots are in close agreement. There is marginal difference of potential towards the drain side between model and simulation. For example, for L = 30 nm at $V_{DS} = 1$ V this difference are 86.4 mV. Figure 6a, b show the threshold voltage and drain induced barrier lowering characteristics extracted from model and simulation, for different gate lengths. The values obtained from model and simulations are in close agreement. The marginal difference of threshold voltage between model and TCAD results for say, L = 20 nm and L = 60 nm are 0.013 and 0.003 V respectively. The difference of DIBL between model and TCAD results are 9 mV and 1 mV for L = 20 nm and L = 60 nm respectively.

3 Drain current model

The mobile charge density Q_m can be written as

$$Q_m = Q_{SC} - Q_d \tag{21}$$

$Q_d = qN_DT_{si}$ is the fixed charge density. The drain current can be expressed as (using (7))

$$I_D = -\mu \frac{W}{L} \int_0^{V_{DS}} Q_m dV$$
$$= -\mu \frac{W}{L} \int_0^{V_{DS}} [2C_{ox}(V_G - V_{FB} - \Psi_S) + Q_d] dV \tag{22}$$

It is assumed that $V_S = 0$ and $V_D = V_{DS}$. W is the width of the device and Ψ_S (long-channel part + short-channel part) is the surface potential. Figure 7 shows the drain current with respect to gate voltage for different values of N_D i.e., 8×10^{18} cm^{-3} and 1×10^{19} cm^{-3} at a drain voltage of 1 V. Same current values are plotted in both logarithmic (left) and linear (right) scales. The model results (symbols) are in

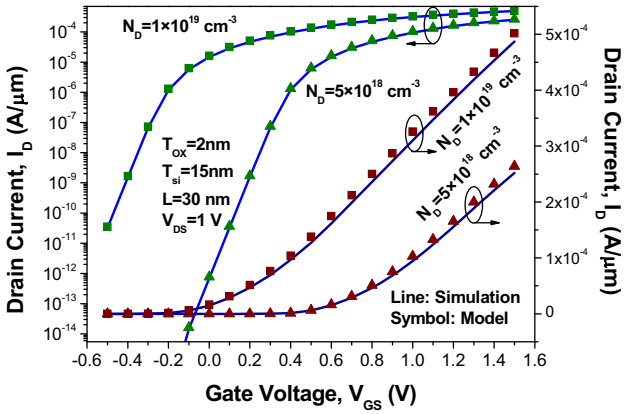

Fig. 7 Drain current with respect to gate voltage for $N_D = 5 \times 10^{18}$ cm^{-3} and 1×10^{19} cm^{-3}. $L = 30$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $V_{DS} = 1$ V and source/drain extension length = 10 nm. Flat band voltage (V_{FB}) considered is ~1.1 eV. *Lines* show the TCAD simulations and *symbols* shows model results

close agreement with TCAD simulation (lines) in all regions of device operation, *i.e.*, from subthreshold to accumulation regions. The subthreshold slope obtained from model is almost equal to TCAD results. As expected, current saturates at higher gate voltages. Also, saturation current increases with increase in channel doping concentration, as usual. The current in the accumulation region is obtained numerically. The subthreshold slope extracted from model and TCAD are in close agreement for long as well as short channel DGJLT. For example, for a DGJLT with $L = 30$nm, $T_{si} = 10$ nm, $T_{ox} = 2$ nm and $N_D = 1 \times 10^{19}$ cm^{-3}, the subthreshold slope is 63 mV/dec as extracted from TCAD, which is almost similar to the value extracted from model. Figure 8 shows the transfer characteristic for *Tsi*=10 nm, *L*=30nm, $T_{ox} = 2$ nm and $N_D = 1 \times 10^{19}$ cm^{-3} at gate voltages V_{GS} of 50 mV and 1 V. Both TCAD (solid line) and model results (symbols)

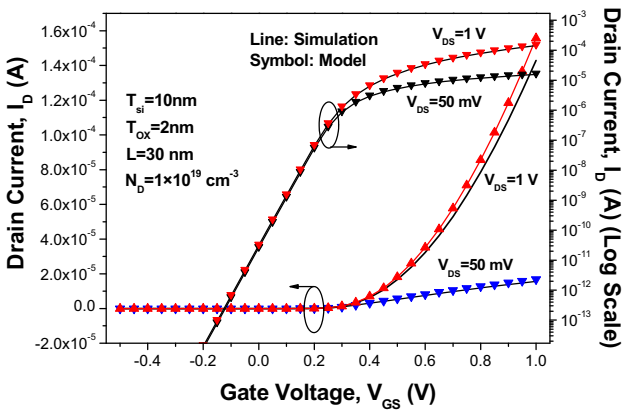

Fig. 8 Drain current with respect to gate voltage for $T_{si} = 10$ nm, $L = 30$ nm, $T_{ox} = 2$ $N_D = 1 \times 10^{19}$ cm^{-3} and source/drain extension length = 10 nm at $V_{DS} = 50$ mV and 1 V. *Lines* show the TCAD simulations and *symbols* shows model results

are in close agreement. Figure 9 shows the drain current with respect to gate voltage for $L = 80$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $N_D = 1 \times 10^{19}$ cm^{-3} at $V_{DS} = 1$ V. Lines show the TCAD simulations and symbols shows model results. TCAD (solid line) and model results (symbols) are in good agreement. Figure 10 presents the drain current with respect to drain voltage for different values of N_D *i.e.*, 8×10^{18} cm^{-3} and 1×10^{19} cm^{-3} at a gate voltage of 1 V. The models (symbols) are in close accord with TCAD simulation (lines). The transconductance with respect to gate voltage for L=30 nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $N_D = 1 \times 10^{19}$ cm^{-3} at $V_{DS} = 1$ V is shown in Fig. 11. TCAD simulations (symbols) and model results (lines) are not in close match at higher gate voltages. Figure 12 shows the output conductance with respect to drain voltage for $L = 30$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$

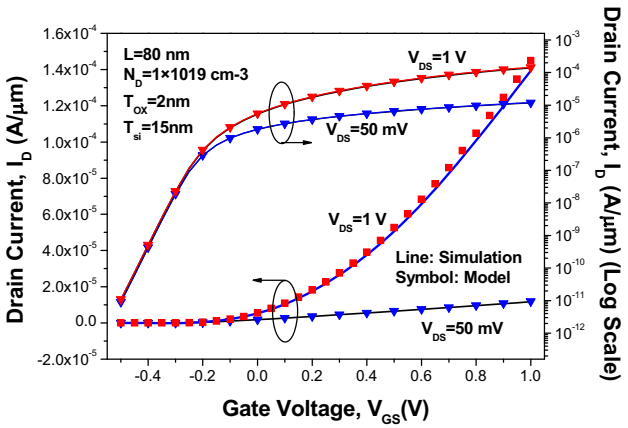

Fig. 9 Drain current with respect to gate voltage for $L = 80$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $N_D = 1 \times 10^{19}$ cm^{-3} and source/drain extension length=10 nm at $V_{DS} = 50$ mV and 1 V. *Lines* show the TCAD simulations and *symbols* shows model results

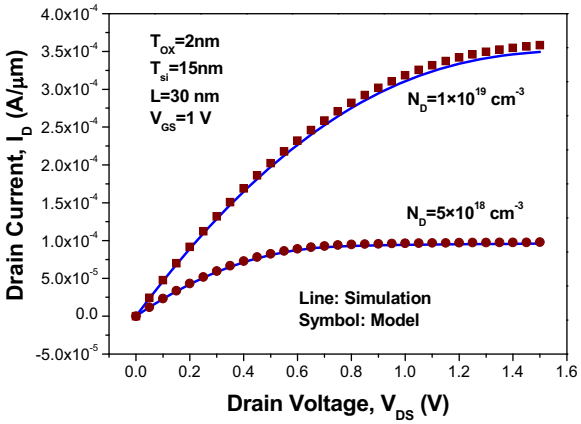

Fig. 10 Drain current with respect to drain voltage for $N_D = 5 \times 10^{18}$ cm^{-3} and 1×10^{19} cm^{-3}. $L = 30$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $V_{GS} = 1$ V and source/drain extension length = 10 nm. Flat band voltage (V_{FB}) considered is ~1.1 eV. *Lines* show the TCAD simulations and *symbols* shows model results

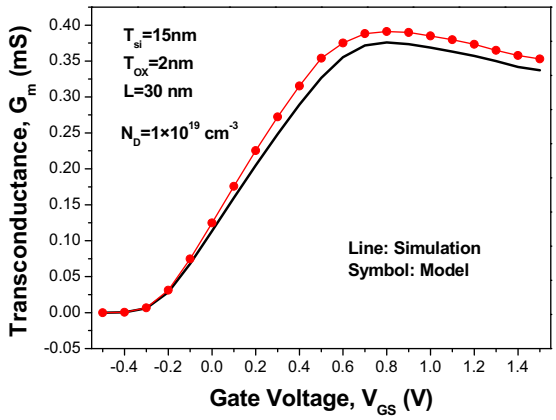

Fig. 11 Transconductance with respect to gate voltage for $L = 30$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $N_D = 1 \times 10^{19}$ cm^{-3} at $V_{DS} = 1$ V and source/drain extension length = 10 nm. *Lines* show the TCAD simulations and *symbols* shows model results

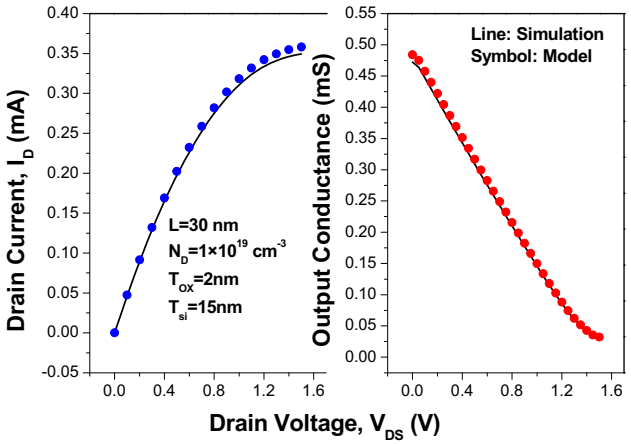

Fig. 12 Drain current and output conductance with respect to drain voltage for $L = 30$ nm, $T_{si} = 15$ nm, $T_{ox} = 2$ nm, $N_D = 1 \times 10^{19}$ cm^{-3} at $V_{GS} = 1$ V and source/drain extension length = 10 nm. *Lines* show the TCAD simulations and *symbols* shows model results

nm, $N_D = 1 \times 10^{19}$ cm^{-3} at $V_{GS} = 1$ V. Both TCAD and model results are in close agreement.

4 Conclusion

In this work, we have proposed a semi-analytical model to calculate the channel surface potential as well as drain current for shorter channel length symmetric double-gate junctionless transistor by a two parts approach. Carrier mobility is assumed to be constant and the quantum effects are not considered. The model is valid in depletion to accumulation regions of operation. Threshold voltage and drain induced barrier lowering parameters were extracted from model. Assessment of the model with TCAD simulations confirms its legitimacy. Consideration of short-channel and quantum effects in the model is another scope for future research.

Acknowledgments This work was partially supported by DST SERB, Government of India, under Grant No. SB/FTP/ETA-268/2012.

References

1. Colinge, J.-P., Lee, C.-W., Afzalian, A., Akhavan, N.D., Yan, R., Ferain, I., Razavi, P., O'Neill, B., Blake, A., White, M., Kelleher, A.-M., McCarthy, B., Murphy, R.: Nanowire transistors without junctions. Nat. Nanotechnol. **5**, 225–229 (2010)
2. Gnani, E., Gnudi, A., Reggiani, S., Baccarani, G.: Theory of the junctionless nanowire FET. IEEE Trans. Electron Devices **58**, 2903–2910 (2011)
3. Duarte, J.P., Choi, S.-J., Choi, Y.-K.: A full-range drain current model for double-gate junctionless transistors. IEEE Trans. Electron Devices **58**, 4219–4225 (2011)
4. Chen, Z., Xiao, Y., Tang, M., Xiong, Y., Huang, J., Li, J., Gu, X., Zhou, Y.: Surface-potential-based drain current model for long-channel junctionless double-gate MOSFETs. IEEE Trans. Electron Devices **59**, 3292–3298 (2012)
5. Sallese, J.-M., Chevillon, N., Lallement, C., Iñiguez, B., Prégaldiny, F.: Charge-based modeling of junctionless double-gate field-effect transistors. IEEE Trans. Electron Devices **58**, 2628–2637 (2011)
6. Lime, F., Santana, E., Iñiguez, B.: A simple compact model for long-channel junctionless double gate MOSFETs. Solid State Electron. **80**, 28–30 (2013)
7. Duarte, J.P., Choi, S.-J., Choi, Y.-K.: A full-range drain current model for double-gate junctionless transistors. IEEE Trans. Electron Devices **58**, 4219–4225 (2011)
8. Duarte, J.P., Choi, S.J., Moon, D.I., Choi, Y.K.: Simple analytical bulk current model for long-channel double-gate junctionless transistors. IEEE Trans. Electron Devices **32**, 704–706 (2011)
9. Duarte, J.P., Kim, M.-S., Choi, S.-J., Choi, Y.-K.: A compact model of quantum electron density at the subthreshold region for double-gate junctionless transistors. IEEE Trans. Electron Devices **59**, 1008–1012 (2012)
10. Duarte, J.P., Choi, S.-J., Moon, D.-I., Choi, Y.-K.: A nonpiecewise model for long-channel junctionless cylindrical nanowire FETs. IEEE Electron Device Lett. **33**, 155–157 (2012)
11. Chiang, T.-K.: A quasi-two-dimensional threshold voltage model for short-channel junctionless double-gate MOSFETs. IEEE Trans. Electron Devices **59**, 2284–2289 (2012)
12. Gnudi, A., Reggiani, S., Gnani, E., Baccarani, G.: Semianalytical model of the subthreshold current in short-channel junctionless symmetric double-gate field-effect transistors. IEEE Trans. Electron Devices **60**, 1342–1348 (2013)
13. Trevisoli, R.D., Doria, R.T., Souza, M., Pavanello, M.A.: A physically-based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors. Solid-State Electron. **90**, 12–17 (2013)
14. Trevisoli, R.D., Doria, R.T., Pavanelloc, M.A.: Analytical model for the threshold voltage in junctionless nanowire transistors of different geometries. ECS Trans. **39**, 147–154 (2011)
15. Trevisoli, R.D., Doria, R.T., de Souza, M., Pavanello, M.A.: Accounting for short channel effects in the drain current modeling of junctionless nanowire transistors. ECS Trans. **49**, 207–214 (2012)
16. Gnudi, A., Reggiani, S., Gnani, E., Baccarani, G.: Analytical model for the threshold voltage variability due to random dopant fluctuations in junctionless FETs, pp. 5–7. SISPAD, Denver (2012)

17. Cerdeira, A., Estrada, M., Iniguez, B., Trevisoli, R.D., Doria, R.T., Souza, M., de, M., Pavanello, A.: Charge-based continuous model for long-channel symmetric double-gate junctionless transistors. Solid-State Electron **85**, 59–63 (2013)
18. Cerdeira, A., Estrada, M., Trevisoli, R.D., Doria, R.T., de Souza, M., Pavanello, M.A.: Analytical model for potential in double-gate juntionless transistors. Symposium on Microelectronics Technology and Devices (2013)
19. Jin, X., Liu, X., Wu, M., Chuai, R., Lee, J.-H., Lee, J.-H.: Modelling of the nanoscale channel length effect on the subthreshold characteristcs of junctionless field-effect transistors with a symmetric double-gate structure. J. Phys. D **45**, 375102–375107 (2012)
20. Yesayan, A., Prégaldiny, F., Sallese, J.-M.: Explicit drain current model of junctionless double-gate field-effect transistors. Solid-State Electron. **89**, 134–138 (2013)
21. Hu, G., Xiang, P., Ding, Z., Liu, R., Wang, L., Tang, T.-A.: Analytical models for electric potential, threshold voltage, and subthreshold swing of junctionless surrounding-gate transistors. IEEE Trans. Electron Devices **61**, 688–695 (2014)
22. Woo, J.-H., Choi, J.-M., Choi, Y.-K.: Analytical threshold voltage model of junctionless double-gate MOSFETs with localized charges. IEEE Trans. Electron Devices **60**, 2951–2955 (2013)
23. Li, C., Zhuang, Y., Di, S., Han, R.: Subthreshold behavior models for nanoscale short-channel junctionless cylindrical surrounding-gate MOSFETs. IEEE Trans. Electron Devices **60**, 3655–3662 (2013)
24. Trevisoli, R.D., Doria, R.T., Souza, M., Das, S., Ferain, I., Pavanello, M.A.: Surface-potential-based drain current analytical model for triple-gate junctionless nanowire transistors. IEEE Trans. Electron Devices **59**, 3510–3518 (2012)
25. Jiang, C., Liang, R., Wang, J., Xu, J.: A two-dimensional analytical model for short channel junctionless double-gate MOSFETs. AIP Adv. **5**, 057122 (2015)
26. Xi, L., Kwon, H., Lee, J., Lee, J.: A subthreshold current model for nanoscale short channel junctionless MOSFETs applicable to symmetric and asymmetric double-gate structure. Solid-State Electron. **82**, 77–81 (2013)
27. Holtij, T., Schwarz, M., Kloes, A., Iñíguez, B.: Threshold voltage, and 2D potential modeling within short-channel junctionless DG MOSFETs in subthreshold region. Solid-State Electron. **90**, 107–115 (2013)
28. Hamid, H.A.E., Guitart, J.R., Iniguez, B.: Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric double-gate MOSFETs. IEEE Trans. Electron Devices **54**, 1402–1408 (2007)
29. Liang, X., Taur, Y.: 2-D analytical solution for SCEs in DG MOSFETs. IEEE Trans. Electron Devices **51**, 1385–1391 (2004)
30. Holtij, T., Schwarz, M., Kloes A., Iniguez, B.: 2D analytical potential modeling of junctionless DG MOSFETs in subthreshold region including proposal for calculating the threshold voltage. 13th International Conference on Ultimate Integration on Silicon (ULIS), pp. 81– 84 (2012)
31. Atlas User's Manual: Device Simulation Software (2008)